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Comparative Analysis of SEGR and SEB Susceptibility in Si and SiC MOSFETs Using TCAD Modeling

C.M. Marques, A. Michez, T. Labau, R. C. Germanicus, F. Wrobel, V. Chazal, G. Bascoul and K. Niskanen.

***Abstract*— This work covered two representative radiation environments: a moderate case using Al and Na ions, representative of low-LET atmospheric neutron-induced secondaries, and a worst-case scenario using high-LET Xe ions relevant to space conditions. Using TCAD simulations, sensitivities against Single-Event Gate Rupture (SEGR) and Single-Event Burnout (SEB) destruction are evaluated for Si and SiC VDMOSFETs under the heavy-ion irradiations. Results show that SiC MOSFET exhibit higher susceptibility to SEGR and SEB compared to their Si MOSFET counterparts, even under moderate conditions, due to their higher critical electric field and structural characteristics. Furthermore, the simulations reveal that once a failure is initiated, a dense plasma column propagates toward the drain, driving Joule heating, impact ionization, and extensive thermal damage across multiple transistors, in agreement with experimental post-irradiation observations. These findings demonstrate the importance of combining experimental evidence with physics-based TCAD modeling to achieve a comprehensive understanding of radiation-induced failure mechanisms in power MOSFETs for both SEGR and SEB.**

***Index Terms*—SiC, SEGR, SEB, TCAD, ECORCE.**

I. Introduction

SILICON carbide (SiC) power devices have emerged as strong candidates to replace conventional silicon (Si) components in high-performance applications. The wide bandgap, high critical electric field, and superior thermal conductivity of SiC enable high-voltage and high-frequency operation with reduced on-resistance [1, 2]. Consequently, SiC devices are often regarded as promising candidates for space, avionics, and nuclear applications [3-5].

Given these favorable material properties, SiC MOSFETs are generally expected to exhibit greater radiation robustness than their silicon counterparts. However, numerous studies challenge this assumption. Martinella et al. [6] conducted heavy-ion microbeam experiments on commercial SiC VDMOSFET identifying sensitive regions. They showed that bias conditions and device architecture strongly influence in the leakage-current related with SEE. In the same direction, Peng [7] investigated catastrophic failures in SiC MOSFETs under heavy-ion irradiation through a combination of experimental results and TCAD simulations. The study demonstrated that localized charge deposition and subsequent thermal feedback can escalate into Single-Event Burnout (SEB), sometimes leaving permanent melting features near the gate region. In complement of these previews works, Grome and Ji [8] reviewed SEB mechanisms across multiple experimental studies and proposed design tolerance guidelines. More recently, Germanicus et al. [9] reported destructive failures in COTS SiC MOSFETs caused by neutron-induced secondary ions under moderate operating conditions. Two distinct failure mechanisms were identified: Single-Event Gate Rupture (SEGR), resulting from ion strikes in the gate region, and (SEB), triggered by ion strikes beneath the source region. This finding is particularly relevant for space and avionics environments, as it suggests that catastrophic failures may occur under realistic conditions without requiring extreme bias or very high-LET ions.

These effects reveal a critical paradox: the same properties that make SiC attractive for power applications, such as a high critical electric field, can also enhance their vulnerability to radiation. Specifically, the ability to sustain high electric fields allows potential energy to accumulate within the device, which can drive strong thermal runaway once a failure process is initiated [10].

In contrast, Si-based power MOSFETs, despite their lower breakdown voltage and reduced thermal performance, tend to exhibit more predictable behavior under irradiation. This reliability is largely attributed to their more mature and optimized technological process. In Si power devices, SEGR is the dominant failure mechanism [11], while SEB, although possible, is less frequent and strongly dependent on design factors such as the gain of the parasitic BJT structure [12]. Titus [13] experimentally demonstrated the dependence of SEGR thresholds on gate bias and ion LET, whereas Kuboyama et al. [14] investigated the microscopic damage sites associated with SEGR in vertical Si MOSFETs. In addition, Huang et al. [15] analyzed the role of device geometry on SEGR and SEB thresholds in super-junction structures.

However, direct side-by-side evaluations of Si and SiC MOSFETs under equivalent irradiation environments remain limited in the literature. To address this gap, this work presents a comparative analysis of Si and SiC VDMOSFETs, focusing on their respective sensitivities to radiation-induced failure mechanisms. Using detailed TCAD simulations and data obtained from experimental results, the parameters triggering SEGRs at the SEB are being studied. The influence of ion LET, impact location, and material properties on the onset of SEGR and SEB are evaluate for both Si and SiC MOSFET. The

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objective is to assess not only which technology is more vulnerable under specific conditions, but also to provide physical insight into the mechanisms driving these vulnerabilities.

II. Si And SiC MOSFET Modeling

In order to compare radiation-induced failure mechanisms in Si and SiC power MOSFETs, both devices were modeled using the ECORCE (Étude du COmportement sous Radiation des Composants Électroniques) TCAD tool developed by Delphea [16]. ECORCE employs a drift–diffusion framework coupled with the heat equations, enabling thermodynamic simulations to resolve local temperature. A dynamic mesh generator optimizes the mesh distribution at each simulation step to capture steep gradients near critical regions. Simulations were carried out using state-of-the-art physical models [16, 17], including temperature-dependent specific heat and thermal conductivity, carrier lifetime as a function of doping, Shockley–Read–Hall recombination, carrier mobility as a function of electric field, temperature, and carrier concentration, bandgap narrowing with temperature, impact ionization, and band-to-band tunneling.

The device structure was based on a commercial vertical double-diffused MOSFET (VDMOSFET) [9]. Fig. 1 highlights the main layers of a representative VDMOSFET cross section, and Table I summarizes the structural parameters used in the simulations. Minor modifications were introduced between Si and SiC devices to maintain the maximum internal electric field below the critical value of each material. These modifications consists of a $1x10^{15}$ cm^{-3} n-doped 20 µm epilayer for Si and $1x10^{16}$ cm^{-3} n-doped 10 µm for SiC. The p-well doping is $2.5x10^{18}$ cm^{-3} for Si, while for SiC is $2.5x10^{18}$. Also, both devices were simulated under off-state condition (V_G = 0V), with the drain terminal at high voltage (V_{DS} = 200 V for Si and V_{DS} = 1000 V for SiC). It highlights the advantage of SiC properties, which allow devices with thinner epilayers, higher doping, and higher bias voltage in comparison with Si [1].

To analyze the influence of ionizing radiation, perpendicular (90°) ion strikes were simulated using Aluminum (Al, 27.6 MeV) and Xenon (Xe, 1.3 GeV) ions. The Al ions were chosen since they are representative of secondary products generated by atmospheric neutron interactions, providing a moderate LET (~10–15 MeV·cm²/mg) with an adequate range to cross the epitaxial layer of the SiC device. This makes them suitable for reproducing realistic ground-level and avionics conditions. In contrast, Xe ions were included to emulate a high-LET environment, representing severe conditions relevant to space applications and serving as a worst-case reference. Two injection sites were defined: beneath the gate region (x = 0.5 µm), targeting susceptibility to SEGR, and beneath the source region (x = 2.5 µm), targeting susceptibility to SEB [9]

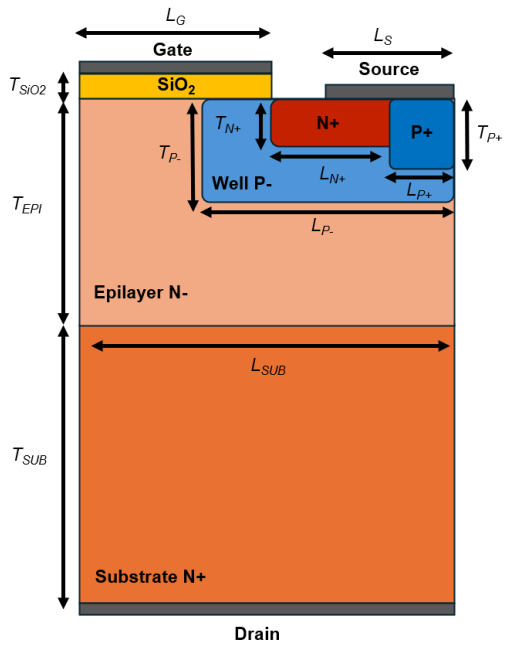

Fig. 1. Typical VDMOSFET geometry.

TABLE I

Main design parameters in the modeling [9].

Symbol	Description		Value
L_G	Gate terminal length (µm)		1.5
L_S	Source terminal length (µm)		0.8
L_{SUB}	Substrate length (µm)		2.9
L_{P-}	Well P- length (µm)		2.0
L_{N+}	N+ length (µm)		0.9
L_{P+}	P+ length (µm)		0.6
T_{SiO2}	Oxide thickness (µm)		0.03
T_{P-}	Well P- thickness (µm)		1.0
T_{N+}	N+ thickness (µm)		0.3
T_{P+}	P+ thickness (µm)		0.39
-	Substrate doping (cm^{-3})		3.0×10^{18}
-	P+ doping (cm^{-3})		2.0×10^{19}
-	N+ doping (cm^{-3})		1.0×10^{19}
T_{EPI}	Epilayer N- thickness (µm)	Si	20
		SiC	10
T_{SUB}	Substrate thickness (µm)	Si	170
		SiC	180
-	Epilayer N- doping (cm^{-3})	Si	1.0×10^{15}
		SiC	1.0×10^{16}
-	P- doping (cm^{-3})	Si	1.0×10^{17}
		SiC	2.5×10^{18}

III. Ion Injection Results

A. Ion injection beneath the Gate

When ions were injected beneath the gate oxide, both Si and SiC VDMOSFETs showed vulnerability to SEGR. However, significant differences in electric field dynamics and sensitivity to ion LET were observed. Fig. 2(a) and 2(b) present the spatial electric field distribution along the vertical axis of the devices for Xe and Al ion strikes, respectively. In both devices, the oxide interface is located at 190 µm. In the Si device, the substrate/epilayer interface is located deeper at 170 µm whereas in the SiC device it is at 180 µm.

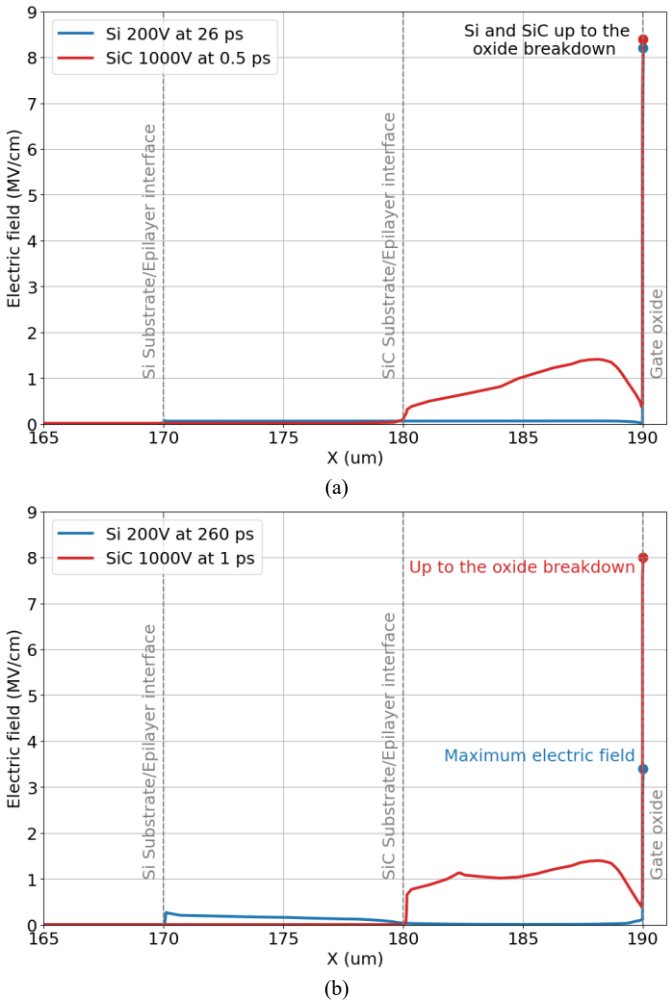

Fig. 2. Spatial distribution of the electric field for ion injection below the gate: (a) Xe 1.3 GeV and (b) Al 27.6 MeV.

Under high-LET conditions (Xe ion), both devices exceeded the critical breakdown field of SiO_2 (typically ~5–7 MV/cm). TCAD modeling indicates that the maximum electric field in the oxide reaches a much higher value than the breakdown value (SiC: 55 MV/cm, Si: 16 MV/cm). However, for a better understanding of both material behavior, we show the electric field distribution along the ion track when the electric field goes up to 8 MV/cm. This occurs at 26 ps for the Si device, whereas this value is exceeded at 0.5 ps for the SiC device. The faster onset in SiC is explained by its higher background electric fields, thinner/high-doped epilayer, which together accelerate the build-up of the critical conditions for failure.

In contrast, under low-LET conditions (Al ion), only the SiC device exceeded the breakdown field, reaching 8 MV/cm at 260 ps. The Si device remained well below the critical threshold, with a peak electric field of only 3.4 MV/cm. These results clearly indicate that SiC devices are more sensitive to SEGR, even under low-LET environment. This increased sensitivity can be attributed to a combination of material and structural factors. SiC devices operate with higher internal electric fields due to their ability to sustain breakdown levels approximately 10x higher than Si [10], resulting in elevated background fields near the oxide.

B. Ion injection beneath the Source

When ions were injected in the source region, SEB is the dominant failure mechanism. A notable divergence in behavior between Si and SiC devices was observed, particularly under high-LET conditions. Figures 3(a) and 3(b) show the electric field distribution along the device structure for Xe and Al ion strikes, respectively. In addition, Fig. 4 presents the maximum temperature distribution along the device structure for Xe and Al ions.

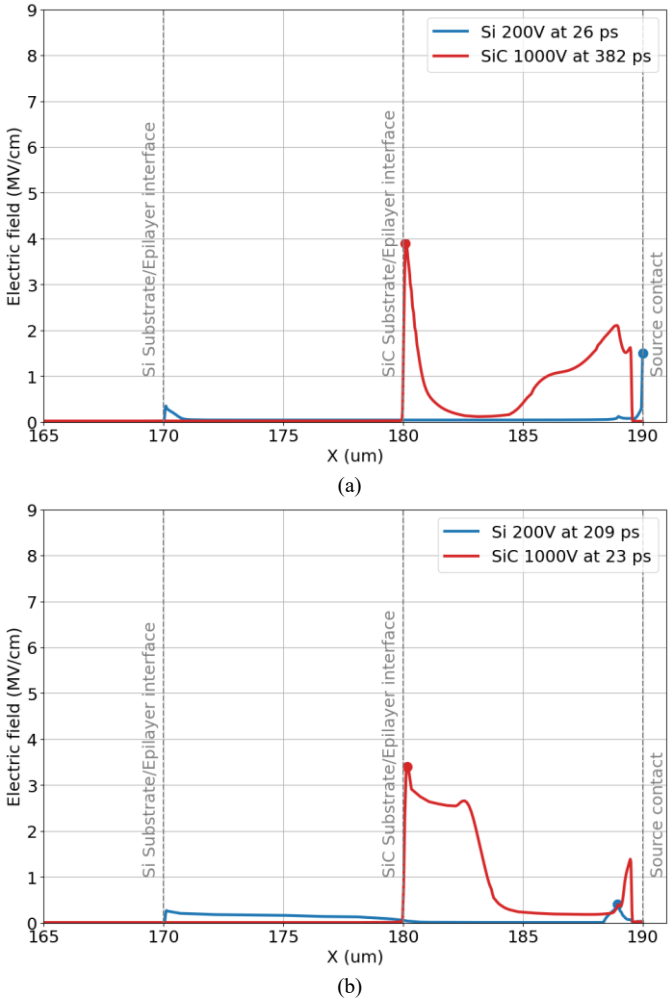

Fig. 3. Spatial distribution of the electric field for ion injection below the source: (a) Xe 1.3 GeV and (b) Al 27.6 MeV.

Under high-LET conditions, the SiC device exhibited a peak electric field of approximately 4 MV/cm at the epilayer/substrate junction. This value exceeds the critical electric field for 4H-SiC (typically ~3.0–3.5 MV/cm), triggering impact ionization and band-to-band tunneling. These processes initiate a feedback loop between current and heat, ultimately leading to thermal runaway. The corresponding temperature distribution shown in Fig. 4 confirms this burnout condition, with the lattice temperature rising above 3000 K. This value is well beyond the material's sublimation threshold (~2700 K) [18]. These findings are consistent with previously reported results in [9]. In contrast, the Si device remained stable under the same conditions, with no indication of burnout. Fig. 5 also shows the maximum lattice temperature in the Si device, remained below 500 K, which is not sufficient to cause thermal runaway. However, depending on the metal contact used (e.g., aluminum , with a melting point of 660 K), such temperatures could approach the melting range of metal leading to contact degradation [7, 10].

Under low-LET conditions, neither device experienced SEB. The Si device exhibited a nearly uniform temperature profile around 318 K and electric fields under 0.5 MV/cm. For the SiC device, temperatures peaked near 450 K and the field approached 3 MV/cm, which is high, and very close to the critical value. These results confirm that the SiC structure is significantly more susceptible to burnout, even under similar ion energy deposition conditions than Si.

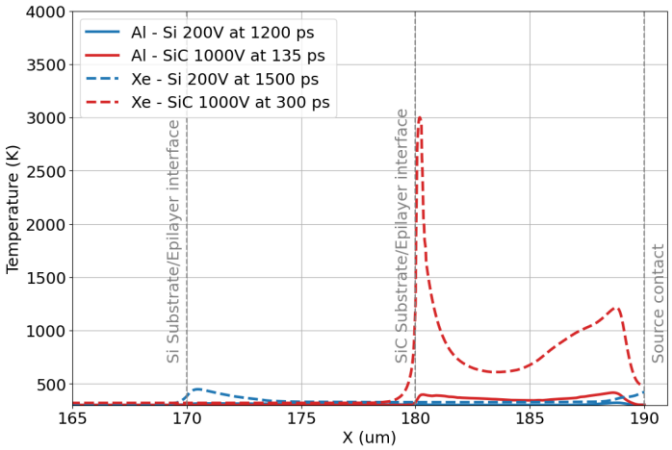

Fig. 4. Spatial distribution of the temperature after ion injection below the source for Xe 1.3 GeV and Al 27.6 MeV.

C. *Failure risk-mapping: SiC versus Si*

Risk mapping has recently been proposed as an effective approach to visualize the spatial dependence of failure susceptibility in SiC MOSFETs, considering all positions inside the device and all secondary ion directions. Germanicus et al. [9] applied this methodology using 27 MeV Al ions, simulating a grid of impact positions and incident angles, and identifying sensitive regions by monitoring both the maximum electric field in the gate oxide (SEGR) and the maximum temperature at the epi–substrate junction (SEB). Their results revealed a strong susceptibility to SEGR under gate-side strikes, while burnout thresholds were not exceeded for Al ions under their operating conditions, emphasizing that ion range is as critical as LET in determining failure sensitivity.

Fig. 5 shows the extension of this analysis to both SiC and Si devices under Al ion irradiation. The SiC map confirms the strong SEGR susceptibility reported in [9], with gate-side cells showing localized fields above the SiO_2 breakdown threshold (dark purple, purple, and pink regions). In contrast, the Si device does not exhibit critical responses under the same conditions, with both electric fields and junction temperatures remaining below failure thresholds. This apparent robustness, however, is primarily the result of the limited range of the Al ion, which prevents significant energy deposition at the epi-layer in Si. Therefore, although Al ion is well suited to reveal SEGR sensitivity in SiC, it is not adequate for a fair comparison of Si and SiC, since the epi-layer is thicker in Si (20 µm) and remains largely unaffected.

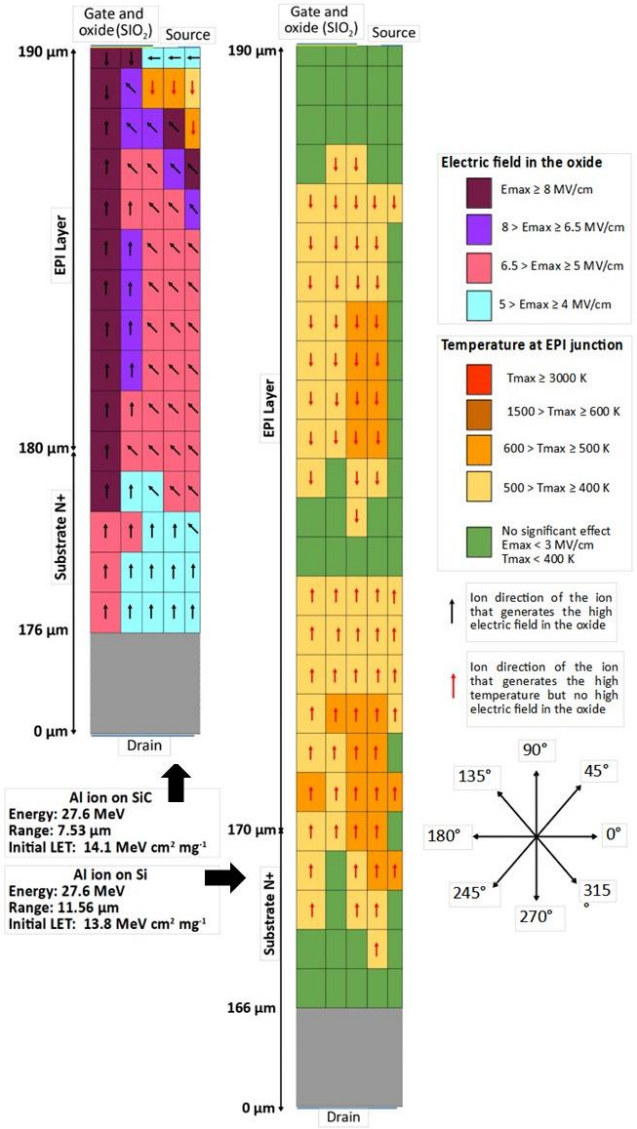

Fig. 5. Risk mapping of SEGR and SEB for 27.6 MeV Al ion in SiC (left) and Si (right) VDMOSFETs under off-state bias (Si = 200V and SiC = 1000V). For each position the electric field in the oxide and temperature at the epi-substrate junction are evaluated for all injection directions.

To address this limitation, we replaced Al with Na ion, keeping comparable energy and LET, but with a longer range. Although Na is not a dominant secondary (like Si or C) product from neutron interactions in Si/SiC, it choice isolates the role of ion range, enabling a direct comparison with the results reported in [9]. Fig. 6 presents the corresponding risk map for the Na ion. For SiC, the results confirm those of [9], showing a pronounced SEGR-sensitive region beneath the gate oxide. In contrast, the injection near the epi-substrate interface showed a lower increase of the electric field and temperature, probably an effect of the lower LET ion. For Si mapping, while the initial analysis with Al ions indicated that the device remained robust, the use of Na ions (longer range) allows the energy deposition track to reach closer to the epi–substrate interface, producing localized heating above 500 K (orange cells). This demonstrates that Si, although generally less vulnerable to SEGR due to its lower background electric fields, can still undergo SEGR if longer-range ions are considered, even at relatively low LET.

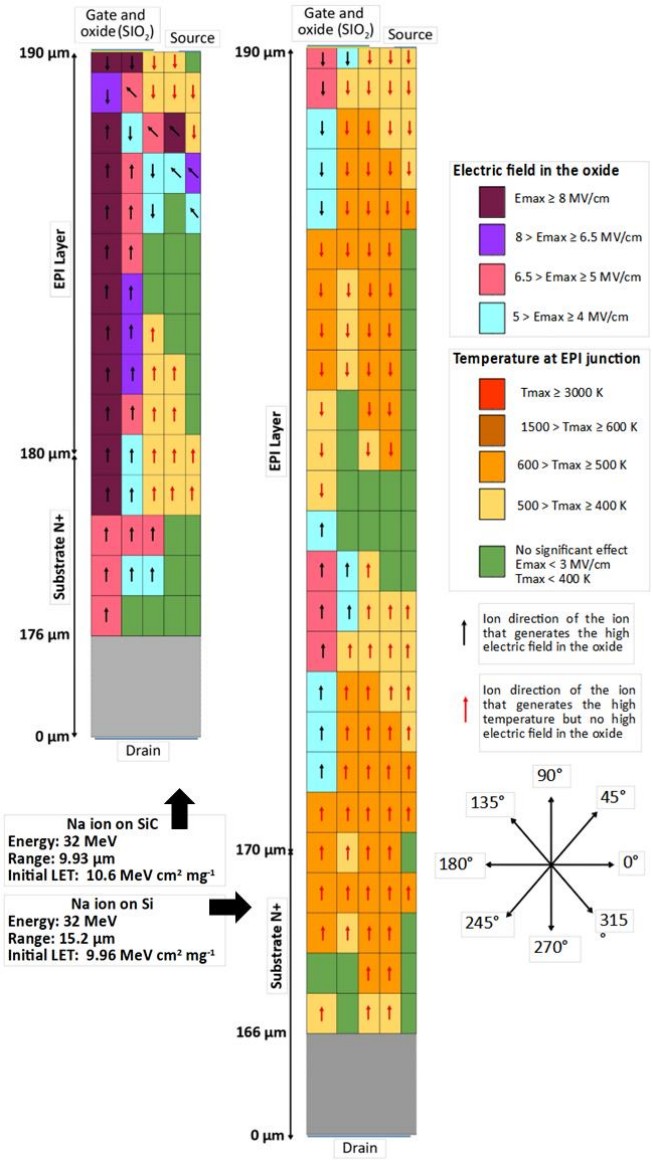

Fig. 6. Risk mapping of SEGR and SEB for 32 MeV Na ion in SiC (left) and Si (right) VDMOSFETs under off-state bias (Si = 200V and SiC = 1000V).

Taken together, these maps highlight two important conclusions. First, susceptibility is determined not only by LET but also by ion range and strike location, which jointly define whether the oxide or the epi–substrate junction becomes the dominant sensitive volume. Second, while SiC's higher breakdown field inherently raises its background fields and favors SEGR, Si devices are not intrinsically immune: under conditions where secondary ions penetrate deep enough, with a high enough LET, they can exhibit SEGR.

IV. Comparison with Experimental Data

In this section, the TCAD results presented in Section III were compared with experimental data available in the literature. Experimental results reported by Titus [13] and Kuboyama [14] showed that SEGR thresholds in vertical Si MOSFETs depend strongly on bias conditions, ion energy, and the position of the Bragg peak within the epitaxial layer. The most critical cases were observed when the ion deposited its maximum energy near the epi–substrate interface, where coupling of the drain potential to the gate oxide drives the local field above the dielectric breakdown strength. This behavior is consistent with our TCAD results, where SiC devices (operating with intrinsically higher background electric fields and thinner epi layer) reach the critical oxide electric field much earlier than their Si counterparts. Our TCAD results extend these findings to SiC devices, showing that due to their higher background fields and structural differences (epilayer thickness and doping concentration), the critical breakdown condition is reached much earlier and under lower LET compared to Si. These conclusions are also in line with recent experimental evidence by Germanicus et al. [9], who reported destructive SEGR events in COTS SiC MOSFETs caused by neutron-induced secondary ions under moderate operating conditions.

The SEB results for source-side strikes are also strongly supported by experimental evidence. In Si power MOSFETs, Liu et al. [12] demonstrated that SEB susceptibility is governed by avalanche dynamics and the gain of the parasitic BJT, while Huang et al. [15] highlighted the strong influence of device geometry on the burnout threshold. Extending these findings to wide-bandgap devices, Niskanen et al. [19] reported that the sensitive volume for SEB in SiC MOSFETs is located near the epi–substrate junction, consistent with our modeling results that reveal rapid avalanche onset in this region. Germanicus et al. [9] further confirmed, under neutron irradiation, that destructive burnout in COTS SiC devices originates from secondary ions reaching the substrate interface.

A. Importance of TCAD modeling

Post-irradiation analysis, such as the cross-sectional Scanning Electron Microscopy (SEM) image for a failed SiC MOSFET in Fig. 7 [9], reveal extensive thermal damage extending across multiple adjacent transistors. While such evidence clearly indicates catastrophic burnout, it does not allow identification of the primary trigger mechanism. The propagation of the failure across several cells makes it even more difficult to determine whether the initial event was a

SEGR or a SEB, since both mechanisms ultimately lead to similar large-scale structural damage.

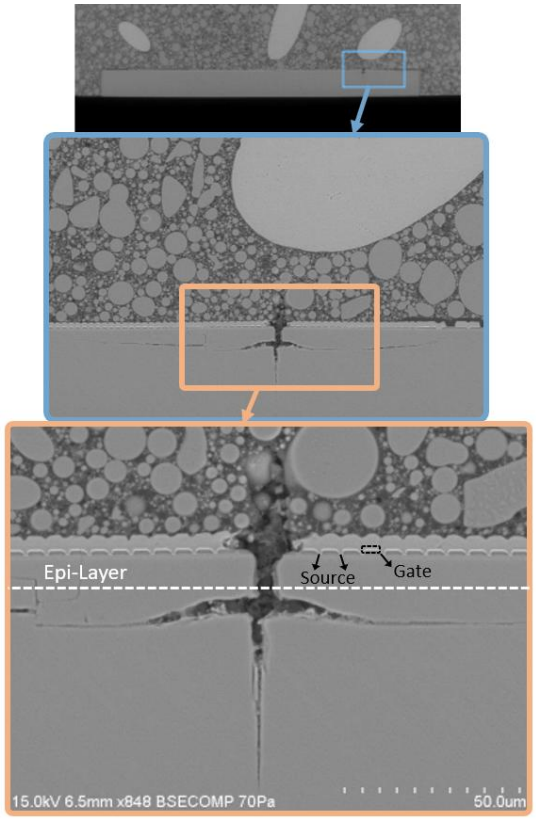

Fig. 7. Cross-sectional Scanning Electron Microscopy (SEM) images of a failed SiC MOSFET after neutron irradiation [14]. The SEM images show the post-irradiation damage extends for a large area in the device, through melting and micro-explosions. Despite the high-resolution imaging, it is not possible to determine whether the failure was initially triggered by SEGR at the gate oxide or by SEB at the source side.

In this context, TCAD modeling provides indispensable complementary insight by reproducing the evolution of electric fields, carrier dynamics, and thermal feedback, thus allowing the identification of the precise conditions that initiate failures. As demonstrated in this work, source-side strikes are associated with rapid avalanche buildup at the epi–substrate junction (SEB), whereas gate-side strikes correspond to oxide breakdown driven by localized electric-field enhancement (SEGR). Moreover, TCAD enables systematic variation of parameters such as ion LET, strike location, and device geometry under conditions that are difficult or impractical to achieve experimentally. Together with experimental evidence, these simulations establish a comprehensive framework: while experiments reveal the extent and morphology of device damage, TCAD links these observations to the underlying physical mechanisms.

B. Damage expansion after the failure

Usually, the post-irradiation cross section (Fig. 7) reveals intriguing characteristic that is often overlooked: regardless of whether the initiating event was SEGR at the gate oxide or SEB at the epi–substrate interface, the resulting damage extends several micrometers into the substrate and across multiple adjacent transistors. This observation indicates that radiation-induced failure is not confined to the initial breakdown site, but is strongly influenced by the subsequent evolution of the plasma generated within the device.

To our knowledge, once the initial rupture or avalanche occurs, a dense carrier plasma is formed in the impacted region. This plasma greatly increases the local conductivity, establishing a low-impedance path between source and drain. Under off-state conditions, the electric field in a vertical MOSFET is oriented from the drain (substrate) toward the source. As a result, the plasma column expands downward, following the direction of carrier drift. The combined effects of Joule heating and impact ionization during this transport process produce progressive material melting, which explains why the damaged area often extends deep into the substrate, far beyond the initial trigger point. The same mechanism also accounts for the lateral spread of the failure, as thermal runaway and micro-explosions propagate into neighboring transistors once the energy release becomes uncontrollable.

This behavior reconciles the apparent discrepancy between the localized initiation predicted by TCAD and the widespread destruction observed experimentally. While TCAD identifies the precise regions where failure is triggered, the subsequent plasma expansion follows the internal electric-field distribution and thermal gradients, producing catastrophic signatures that obscure the original failure site. These insights further clarify why post-irradiation microscopy alone cannot determine whether a given event was initiated by SEGR or SEB, since both mechanisms ultimately converge into an indistinguishable burnout morphology after plasma expansion.

V. Conclusion

This work presented a comparative analysis of Si and SiC vertical double-diffused MOSFETs under heavy-ion irradiation, focusing on the onset of SEGR and SEB through physics-based TCAD simulations with the ECORCE platform. Two radiation environments were considered: a moderate case with Al and Na ions, to represent low-LET secondary products of atmospheric neutrons, and a worst-case scenario with Xe ion, to represent high-LET for space applications. Following the concerns highlighted in the literature, both ions were injected at two critical locations: beneath the gate, to address SEGR, and beneath the source, to assess SEB. Despite their superior electrical and thermal performance under nominal operation, SiC devices exhibited a higher susceptibility to both SEGR and SEB when exposed to ionizing radiation.

When ions were injected beneath the gate, SiC devices exhibited oxide breakdown even under low-LET conditions, whereas Si devices remained below the critical electric field. This behavior was attributed to higher background electric fields in SiC, which promote charge accumulation at the oxide interface. Under high-LET exposure, both technologies exceeded the oxide breakdown threshold, but the onset was significantly faster in the SiC structure.

For source-side ion strikes, SiC devices again showed higher vulnerability for SEB. The electric field at the epilayer/substrate junction exceeded the critical value with Xe ion, initiating a cascade of impact ionization and band-to-band tunneling, ultimately leading to thermal runaway and burnout. In contrast, Si devices remained thermally stable, with electric fields and temperatures below critical thresholds, even under high-LET conditions. This was attributed to the deeper position of the substrate interface in Si, which allowed more energy dissipation before reaching the failure site.

We also extend the risk-mapping approach proposed in [9], demonstrating that longer-range ions such as Na can reveal SEGR-sensitive regions in Si devices that appear robust under Al irradiation. This highlights that ion range, in addition to LET and impact location, plays a decisive role in determining which failure mechanism dominates. These results provide a more complete analysis, comparing SiC with Si device. The SiC higher critical electric field inherently increases its sensitivity to SEGR, whereas Si, although less susceptible to oxide rupture, can still undergo SEGR if longer-range secondaries ions reach the epi–substrate junction.

Our TCAD results were compared with experimental data and confirmed that the simulated failure mechanisms are consistent with destructive events observed in irradiated COTS Si/SiC MOSFETs. It is important to highlight that cross-sectional microscopy obtained from [9] revealed widespread burnout and micro-explosions across multiple cells, masking the original trigger site. TCAD modeling proved essential to complement such experiments by understanding the underlying failure mechanisms.

Beyond the onset of failure, the simulations also revealed the mechanisms governing the subsequent damage expansion. Once a rupture or avalanche is initiated, a dense plasma column of carriers is formed along the ion track. Driven by the vertical electric field from drain to source, this plasma propagates into the substrate, creating a low-impedance path that enhances Joule heating and triggers further impact ionization. This explains why experimental post-irradiation images consistently show widespread thermal damage and micro-explosions extending across multiple adjacent transistors, regardless of whether the initiating event was SEGR or SEB. TCAD modeling thus provides indispensable insight by linking localized initiation sites to the large-scale burnout signatures observed experimentally.

In overall, although SiC offers distinct advantages for power applications, its radiation response must be carefully evaluated even in ground level.

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