A High Power SOI-CMOS WI-FI 6 Front-End Module with Reconfigurable Class-J Power Amplifier

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***Abstract*—This paper presents the design and experimental characterization of a high-power monolithic SOI-CMOS Front End-Module (FEM) supporting Wi-Fi 6 signals over the 5.1 to 5.9GHz frequency band. The FEM includes an SP3T antenna switch, a power amplifier (PA), a low noise amplifier (LNA) with bypass mode, and a digital controller. The LNA achieves 14dB of power gain with less than 2.1dB of noise figure (NF) with 25mW of power consumption. The reconfigurable differential Class-J PA delivers 32dBm of saturated output power (P_{sat}) with 34% of peak PAE. Without DPD, the reconfigurable PA achieves state-of-the art performance with 20/18dBm of linear output power (P_{out}) for an EVM of -34/-37.5dB with 80MHz MCS9/MCS11 signals.**

***Keywords*—Monolithic, SOI, CMOS, Wi-Fi 6, Front-End Module, Low Noise Amplifier, Power Amplifier.**

I. Introduction

The demand for wideband, high-power RF Front-End Modules (FEMs) operating above 5GHz is rapidly increasing, driven by emerging Wi-Fi applications such as augmented and virtual reality (AR/VR) and vehicular wireless access. However, designing wideband, high-power Wi-Fi FEMs for frequencies above 5GHz presents significant challenges, primarily due to stringent linearity requirements imposed by complex modulated signals with high peak-to-average power ratio (PAPR>10dB) and wide bandwidth (>80MHz). Specifically, power amplifiers (PAs) must deliver over 18dBm of average output power while maintaining an error vector magnitude (EVM) better than -38dB under 1024-QAM OFDM modulation. To achieve these demanding performances, power combining techniques, such as series combining transformers (SCTs) or parallel combining transformers (PCTs), are commonly employed [1]. However, achieving high linear transmit power with adequate efficiency and linearity in CMOS technology is particularly challenging.

In this work, we present a high-power monolithic SOI-CMOS FEM featuring a reconfigurable two-way SCT-based differential PA operating in Class-J [2]. The reconfigurable PA optimizes linearity and efficiency based on signal modulation and bandwidth across the 5.1 to 5.9GHz frequency band. To enhance efficiency and linearity over this band, second harmonic traps are integrated into the output transformer. Experimental results demonstrate that the proposed design enables a fully integrated SOI-CMOS FEM with watt-level transmit performance. The PA achieves a saturated output power of 32dBm, along with state-of-the-art linear output power and EVM levels under MCS9 and MCS11 modulation schemes, operating at a 3.8V supply voltage. Compared to state-of-the-art CMOS FEMs, the proposed FEM achieves superior output power and linearity.

II. FEM Description

A fully integrated Wi-Fi 6 FEM including a power amplifier, a low noise amplifier, an antenna switch and a digital control unit is designed and integrated in a 130nm SOI-CMOS process from STMicroelectronics®, Fig. 1. The SOI chip is assembled using flip-chip on a 4-Layer organic LGA package which is then assembled on a PCB for testing purpose. The SOI die size is 2.2x1.8mm^2.

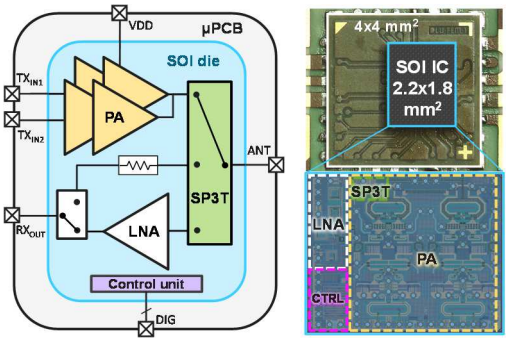
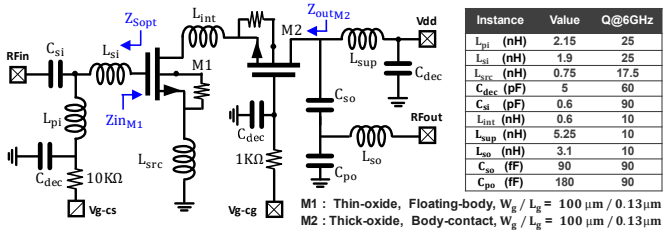


Fig. 1. Block diagram and die and package micrograph of the proposed FEM.

A. Low Noise Amplifier (LNA)

A broadband LNA is designed to cover the 5 to 7GHz frequency band under 2.5V supply voltage while drawing 10mA of DC current. The LNA is designed using the methodology proposed in [3]. The cascode topology, Fig. 2, uses a thin-oxide body-contacted transistor as a common-source (M1) device to achieve low noise-figure (NF) and high input-stage gain. The thick-oxide body-contact common-gate device (M2) boosts the overall gain and improves the reverse isolation and stability while satisfying reliability requirements at high voltage swing. The width of both M1 and M2 is set to 100µm considering the DC current (10mA) and the optimum current-density for minimum NF $J_{c,NF_{min}} \approx 0.1mA/\mu m$.



Instance	Value	Q@6GHz
L_{pi} (nH)	2.15	25
L_{si} (nH)	1.9	25
L_{src} (nH)	0.75	17.5
C_{dec} (pF)	5	60
C_{si} (pF)	0.6	90
L_{int} (nH)	0.6	10
L_{sup} (nH)	5.25	10
L_{so} (nH)	3.1	10
C_{so} (fF)	90	90
C_{po} (fF)	180	90

Fig. 2. Schematic of the proposed broadband WiFi-7 LNA.

The inductor L_{src} matches the input impedance of the common source transistor (Zin_{M1}) to the conjugate of the optimum noise-match source impedance Z^*_{Sopt}. The wideband

input matching use T-network (C_{si}, L_{pi}, L_{si}) matches Zin_{M1} to 50Ω. The two-section output matching-network (C_{so}, C_{po}, L_{so}) is a trade-off between output matching and linearity.

The RX path is measured under $V_{dd} = 2.5V$ and $I_{dc} = 10mA$. The measured and simulated small-signal and large-signal performances, extracted at the LNA output reference plane, are shown on Fig. 3. The simulated and measured results show excellent agreement. Over the 5 to 7GHz band, the LNA achieves a flat S21 with less than ±0.5dB variation around 14dB, a return loss lower than -13dB and a noise figure between 1.65 to 2.1dB. Moreover, the measured OCP_{1dB} is 5dBm around the center frequency and drops to 2dBm at high-band.

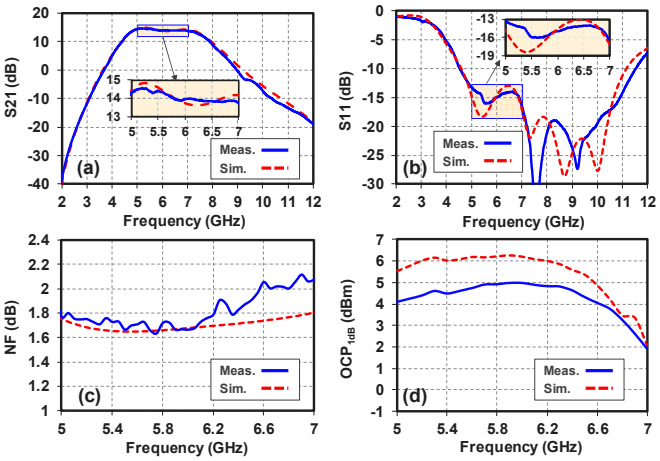
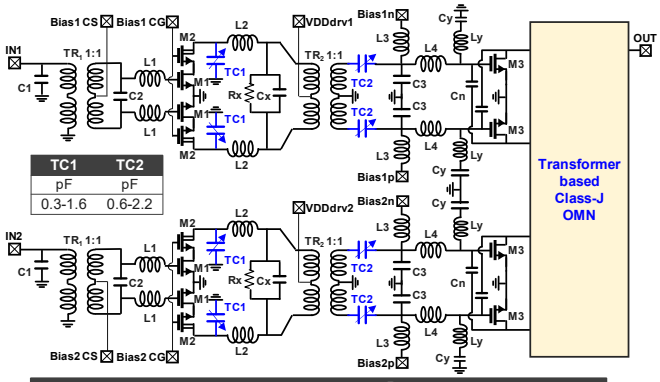


Fig. 3. Measured versus simulated LNA performances versus frequency under V=2.5V and Idc=10mA: (a) S21, (b) S11, (c) Noise Figure, (d) OCP_{1dB}.

B. *Class-J Power Amplifier (PA)*

A fully-integrated two-way differential SCT-based class-J reconfigurable PA is designed to cover the 5.1 to 5.9GHz frequency band (Fig. 1 and Fig. 4).



TC1	TC2
pF	pF
0.3-1.6	0.6-2.2

$W_{M1,2}$	$W_{M3,2}$	Cn	C1	C2	C3	Cy	Cx	Rx	L1	L2	L3	L4	Ly
µm	mm	pF	pF	fF	pF	fF	fF	Ω	pH	pH	nH	pH	pH
900	3	0.75	1.1	250	2.6	650	350	150	96	220	1.6	200	240

Fig. 4. Schematic of the reconfigurable PA.

The SCT power combining approach was preferred to the PCT approach since it offers broadband characteristics with low turn ratio and low loss transformer [1]. The design of the voltage-combined class-J output matching network (OMN) is based on the model presented on Fig. 5 where the primary inductance (L_i), the coupling coefficient (k), the optimal input impedance (Z_{opt}) and the parallel input notch (HT) frequency ($n_r = \omega_0/\omega_r$) are free design parameters.

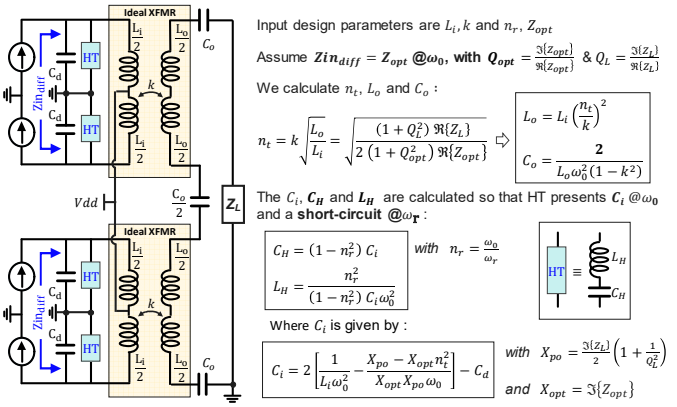


Fig. 5. Transformer-based class-J OMN model and design equations.

With the proposed analytical approach the transformer dimensioning is automatically calculated using the equations of Fig. 5 to present the optimal differential resistance R_{opt} at the internal drain reference plane of each output stage. Note that the output capacitance of each device (C_d) is taken into account in the design equations. As a reminder, for a class-J PA [2] the fundamental and second-harmonic optimal impedances that provide maximum efficiency and output power over frequency are given by the equations (1) to (3).

$$Z_{opt}@f_0 = (1 + j\alpha)R_{opt} \quad (1)$$

$$Z_{opt}@2f_0 = -\frac{j3\pi}{8}\alpha\, R_{opt} \quad (2)$$

$$R_{opt} = (V_{dd} - V_k)^2 / P_{out} \quad (3)$$

Fig. 6 shows the transformer parameters (C_i and L_o/L_i) as a function of L_i, α, k and V_{dd} or R_{opt} assuming that $V_{knee} = 0.63V$ and each differential power cell delivers 30dBm of output power. The knee voltage is calculated considering normalized current density ($J_c \approx 0.37A/mm$) and on-state resistance ($R_{onW} = 1.8\Omega.mm$) of the LDMOS (laterally-diffused MOS) device used for the output stage. As can be seen on Fig. 6-(a) and Fig. 6-(b) for high α and low V_{dd} the L_i value validity range is limited. The maximum value ($L_{i|_{max}}$) is given by the equation:

$$L_{i|_{max}} = X_{opt}X_{po}/\left(X_{po}\omega_0 - X_{opt}{n_t}^2\omega_0\right) \quad (4)$$

with

$$X_{opt}X_{po}\left(X_{po} - X_{opt}{n_t}^2\right) > 0 \quad (5)$$

We assume that the PA operates in class-B at its center frequency $f_c = 5.5\ GHz$ (i.e. $\alpha = 0$). Fig. 5-(c) shows that the inductance ratio L_o/L_i grow significantly when the k factor decrease, which can lead to physical implementation issue. Then, to stay in the $(L_o/L_i) < 5$ region k has to be higher than 0.5. Based on EM simulations of the broadside-couple transformer, the coupling coefficient is fixed to $k = 0.55$.

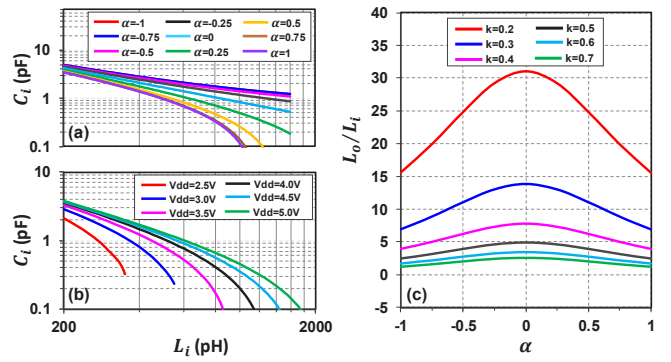


Fig. 6. C_i versus α (a), C_i versus Vdd with $\alpha = 1$ (b) and L_o/L_i inductance ratio versus α (c) for multiple k.

To achieve a continuous class-J operation over the targeted band, the load impedance seen at the internal drain plane of the output devices must satisfy the following conditions:

$$|\alpha(f)| = |\Im m(Z_{in}(f))/\Re e(Z_{in}(f))| \leq 1 \quad (6)$$

$$Z_{in_{H2}}(2f)/Z_{opt_{H2}}(2f) = 1 \quad (7)$$

Note that $Z_{opt,H2}(2f)$ represents the expected impedance at $2f$ considering the actual corresponding impedance at f:

$$Z_{opt_{H2}}(2f) = -j\frac{3\pi}{8}\alpha(f)\,\Re e(Z_{in}(f)) \quad (8)$$

To select the optimum value of L_i, we sweep L_i and the operating frequency f_0 while monitoring P_{out} and DE at 1dB compression as well as the class-J conditions stated in (6) and (7). Note that, n_r is set to 0.5 since we target class-B operation at f_0 (i.e. class-J with $\alpha = 0$). As shown on Fig. 7, for $L_i \approx 350pH$ both class-J conditions (6) and (7) are satisfied over wide frequency range which results in a more constant output power (P_{out} =33dBm +/-0.2dB) and efficiency (DE>68%) compared to other L_i values where condition (7) fails.

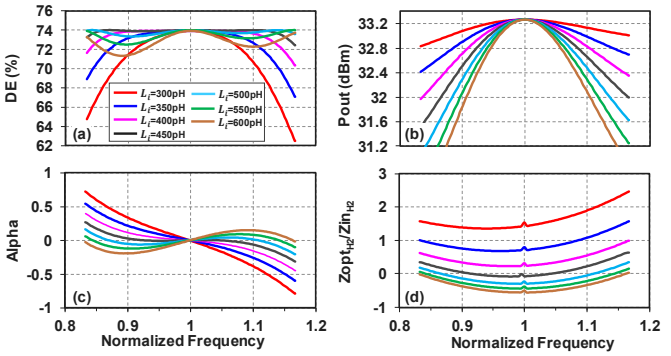


Fig. 7. Differential PA with Class-J OMN performances ($n_r = 0.5$): (a) drain efficiency, (b) P_{out} and (c) class-J conditions $\alpha(f)$ and (d) $Z_{opt_{H2}}(f)/Z_{in_{H2}}(f)$ versus normalized frequency for different L_i values.

The OMN is implemented based on the proposed methodology. The OMN is optimized using electromagnetic simulation. Due to the layout parasitic inductance between the two transformers and the capacitive parasitic of each transformer, the harmonic trap on the TR2 transformer has been removed during final optimization. Also, to overcome high sensitivity to the load imbalance of the SCT structure, careful attention was paid to the symmetry of the two output paths.

Moreover, the output stage uses LDMOS devices with 3mm gate width and a breakdown voltage (BVDSS) of 13.5V. It is important to highlight that the class-J operation leads to a maximum voltage swing that can go up to 2.7 x V_{dd} which requires the transistor to have higher breakdown voltage compared to conventional class-B design. The cross-coupling neutralization capacitances (C_n) of 750fF and the parallel RC network (R_x, C_x) are added to PA stability over the 5-6GHz frequency band. Note that the capacitance C_n is fine tuned in presence of the input harmonic trap ($L_Y - C_Y$) to optimize the AMAM and AMPM of the output stage. The driver stage uses a cascode topology made of a common-source body-contact NMOS device and a common-gate LDMOS device each with a 0.9mm gate width. The driver stage operates in class-AB and delivers 26dBm of saturated output power. A reconfigurable inter-stage matching-network is designed to transform the input impedance of the output stage into the optimum impedance of the driver stage. The reconfigurable capacitors TC_1 and TC_2 control the driver gain and phase profiles and help achieving low overall AMAM and AMPM over frequency, as it will be discussed next in the measurement section.

Finally, a wideband input matching-network is designed to match the drivers input of each PA path to 50Ω over the targeted frequency band. The FEM IC, package and PCB are co-designed using RFPro EM simulator from Keysight. The TX path is measured on-board under V_{dd} = 3.8V and I_{dc} = 150mA. Note that, all the subsequent measurements are extracted at the output plane of the PA and include the insertion loss of the external in-phase power splitter connected to IN_1 and IN_2. The S-parameters and CW characteristics are shown in Fig. 8. On the 5-6GHz frequency range the input/output return loss is lower than -10/-4dB respectively and the PA achieves a saturated output power (P_{sat}) and output-referred 1dB compression power (OP_{1dB}) of 32dBm and 30dBm respectively with a power gain (Gp) between 22.5dB and 24.8dB and a peak PAE between 28.4% and 34%.

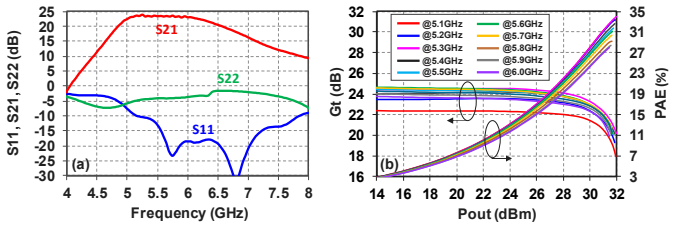


Fig. 8. (a) S-Parameter and (b) CW measurement: Gain and PAE versus Pout from 5.1 to 6GHz frequency.

The PA is characterized using NI™ VST PXIe-5842 under 3.8V supply voltage. To demonstrate the effectiveness of the re-configurability, the PA is measured with 80MHz MCS9 256QAM and MCS11 1024QAM signals without DPD over 5.1 to 5.9GHz while tuning the PA with emphasis on linearity optimization so as to get the lowest EVM for a given targeted output power under a specified EVM level. The resulting EVM and operating current (I_{dd}) are extracted as a function of frequency for two different targeted Pout and three different PA settings (LB, MB, HB) as shown in Fig. 9 The proposed PA supports the 80MHz MCS9 256QAM and MCS11 1024QAM

Table 1. Performance comparison with state-of-the-art 5-6-GHz band CMOS PA for WiFi 6 applications.

Reference	[4] ISSCC17	[5] RFIC18	[6] TMTT19	[7] TMTT19	[8] MWCL23	[9] TCAS24	This Work	
Feature	Two-chip FEM w. Doherty PA	Fully integrated Differential PA	Fully integrated Doherty PA	Fully integrated Reconfigurable PA	Fully integrated Differential PA	Fully integrated Reconfigurable PA	**Fully integrated FEM w. Reconfigurable PA**	
Technology	55nm CMOS / 180nm SOI	55nm CMOS	55nm CMOS	40nm CMOS	180nm CMOS	40nm CMOS	**130nm SOI**	
Chip size (mm)	2.0x0.58 / 1.9x0.76	1.26x0.76	2x3	1x0.2 (wo Bump)	2.3x1.3	1.43x0.8	**1.8x2.2**	
Freq. (GHz)	4.9-5.9	4.9-5.9	5.8	4.9-5.9	5.1-6.1	5.2-5.8	**5.1-5.9**	
Supply (V)	3.3	5.0	5.5	3.3	3.3	2.5	**3.8**	
Psat (dBm)	29	27.6	27.2	27.1	30.1	24.4-24.8	**32**	
Peak PAE (%)	*N.A*	*N.A*	24.5	32.2	18	20.8-27.3	**28-34**	
Modulation BW (MHz)	MCS9 160	MCS9 80	MCS9 80	MCS7 40	MCS9 80	MCS11 80	**MCS9 / 11 80**	**MCS11 80**
DPD	Yes	No	No	No	Yes	No	**No**	**Yes**
EVM (dB)	-38	-35	-35	-32	-32	-35	**-34 / -37.5**	**-42**
Pout (dBm)	18	17.6 @5.53GHz	17 @5.8GHz	<18.8	18.8 @5.3GHz	12.8 @5.53GHz	**20 / 18**	**20.5 – 22.4**
Idd (mA)	191	252	172	189	384	123	**315 / 275**	**310 – 395**

requirement with an EVM of −34/−37.5dB at 20/18dBm Pout with less than 310/275mA I_{dd} respectively without DPD.

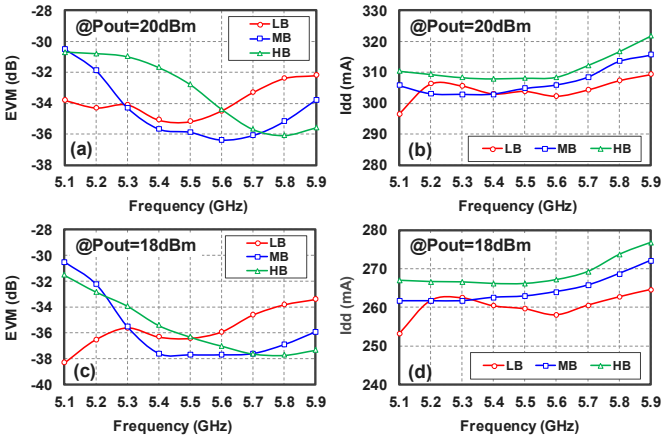


Fig. 9. Measured (left) EVM and (right) I_{dd} versus Pout for 80MHz (top) MCS9 and (bottom) MCS11 signals without DPD.

When applying DPD on a 80MHz MCS11 1024QAM signal, the PAs achieves 20.5-22.4dBm of linear P_{out} for an EVM of −42dB and 310-395mA of I_{dd} as shown in Fig. 10.

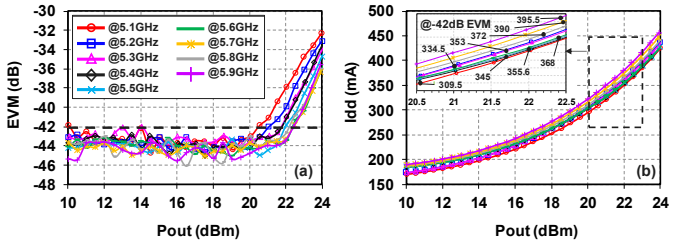


Fig. 10. Measured (a) EVM and (b) I_{dd} versus Pout for 80MHz MCS11 signal over 5.1-5.9GHz with DPD.

Table 1 provides a performance comparison with state-of-the-art 5-6GHz CMOS PA/FEM for Wi-Fi 6 applications. The proposed FEM is the first monolithic high-power FEM with a reconfigurable PA that demonstrates the highest linear Pout without DPD compared to other CMOS-based 802.11ac/ax Wi-Fi PAs operating above 5GHz.

III. Conclusion

This paper presents a high power SOI-CMOS monolithic FEM for Wi-Fi 6 applications in the 5-6GHz frequency range. The LNA achieves 14dB of gain and less than 2.1dB of NF. A new design methodology for the design of differential Class-J PA is proposed. Without DPD, the reconfigurable PA delivers more than 18dBm of average output power under 3.8V supply voltage while satisfying an EVM of -37.5dB in the 5.1GHz to 5.9GHz band under 80-MHz 1024-QAM signal. Compared to state-of-the-art CMOS Wi-Fi 6 PAs, the proposed PA achieves superior output power and linearity. Further optimization of DTC's range and device sizing can help reaching the 5-7GHz.

Acknowledgment

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