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A 22-nm FDSOI 35-41 GHz Frequency Synthesizer

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Abstract — This paper proposes a 35 to 41 GHz frequency synthesizer based on programmable integer- N frequency multiplication offering perfect synchronization with the input reference signal and precise phase control of the output signal. A prototype fabricated in a 22-nm FDSOI technology is presented with phase noise at 1 MHz offset frequency of -97 dBc/Hz, state of the art power and tuning range figures of merit of 174 dBc/Hz and 177 dBc/Hz, respectively, and a power consumption of 32 mW.

Keywords — 5G FR2, Ka-band, frequency synthesizer, injection locked oscillators, phase shifter.

I. INTRODUCTION

For 5G communication systems, the FR2 band (24.25 – 71 GHz) offers a path to overcome the actual crowding of the FR1 frequency range (410 MHz – 7.125 GHz), in addition to enable lower-latency and higher data rate links [1]. The n260 band (37.0 - 40.0 GHz) is likely one of the first bands to be commercially exploited. At these frequencies, beamforming using Massive MIMO (Multiple Input Multiple Output) is proposed to compensate the limitations of operating in the mmW frequencies (e.g. increased path loss and shadowing). The directivity brought by a K antenna array improves the budget link by a factor $10 \cdot \log(K)$ on each end of the link. Furthermore, if the MIMO signals can be phase shifted in a controllable way, beam steering can be implemented enabling spatial selectivity to track users and to reconfigure the links to point to different directions [2]. Other applications using that same frequency range include high-resolution, close-range targeting radars, military aircraft, space telescopes, vehicle speed detection systems, and satellite communications. For most of these applications, it is crucial to use low phase noise oscillator. The transmitted signal phase control is also required in some of them. This can be implemented with a phase shifter in the local oscillator (LO) signal path.

This paper proposes an innovative and agile LO synthesizer based on integer- N frequency multiplication that displays interesting properties such as perfect synchronization with the input reference and precise phase control of the output signal. A prototype fabricated using 22-nm FDSOI technology is presented, showing a 35 to 41 GHz frequency generation range with phase noise at 1 MHz offset frequency of -97 dBc/Hz and state of art figures of merit.

II. FREQUENCY GENERATION ARCHITECTURE AND CIRCUITS

A. High-integer N frequency multiplication architecture

The frequency synthesizer circuit proposed in this paper implements synchronized frequency multiplication by a large integer number N . The basic idea behind this technique is illustrated in Fig. 1 and is based in [3]. An external sinusoidal

reference of much lower frequency than the desired output signal is used at the circuit input (REF IN). This signal is conformed into a square waveform (REF) with controllable duty cycle using a duty cycle controller circuit (DCC) such as the one described in [4]. This circuit generates also a couple of waveforms (C_{OFF} and C_i), both with the same period as the input reference $T_{REF}=1/F_{REF}$, whose function will be clear later. The REF signal is used to switch on and off a pulsed oscillator (P-OSC) designed to have a free-running oscillation frequency inside the frequency band of interest (35-40 GHz). When the oscillator is started exactly in the same way at the beginning of each cycle of the REF signal, it gets synchronized with this signal, and its output results in a periodically repeated oscillation train (PROT) signal. This signal has interesting spectral properties. Firstly, it is composed of several discrete spectral terms that are exact integer multiples of F_{REF} . Secondly, the multiple spectral terms are shaped by a cardinal sine envelope that is centered on the free-running oscillation frequency of the P-OSC. The width of this envelope main lobe depends on the duty cycle of the REF signal. Tuning the P-OSC free-running frequency only results in a displacement of the envelope main lobe, but the spectral terms remain at the same integer multiples of F_{REF} frequency, only its amplitude is changed. In order to extract a single tone from the PROT multi-harmonic output signal, an injection locked oscillator (ILO) is used. This ILO is tuned to center its locking range around the desired integer multiple of the F_{REF} signal, resulting in a output signal with frequency: $F_{out} = N F_{REF}$. Indeed, for a better rejection of the spectral terms laying at adjacent integer multiples (i.e. $(N \pm 1) F_{REF}$) a second ILO can be used in cascade.

B. Circuit description

The above described circuit idea is implemented in a 22-nm FDSOI technology as shown in Fig. 2. The P-OSC is based in a cross-coupled CMOS LC oscillator that is turned on and off by switching its tail current source using the REF signal. The

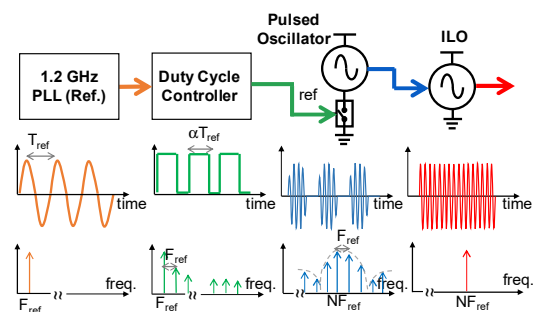


Fig. 1. Frequency synthesizer architecture and basic operation.

signal C_1 is used to start the oscillator always in the same way [5]. The signal C_{OFF} is used to discharge the tank after each oscillator train pulse, so that at the next REF cycle the oscillator starts with the same initial conditions. A differential varactor is used to tune the P-OSC free-running frequency. The output of the P-OSC is coupled to a following buffer using a transformer implemented with the two copper upper thick metal layers of the technology. The buffer is an NMOS common source pseudo-differential amplifier with neutralization capacitors. A controllable bias voltage is used to tune its gain and therefore to modify the amplitude of the signal used to inject the ILO. The output of the buffer is used to drive a first ILO (ILO1) that is implemented using again a cross-coupled CMOS LC topology, this time with a combination of fine, continuous-tuning, and coarse, digital-tuning varactors. The ILO1 is followed by a buffer identical to the P-OSC buffer. A second ILO (ILO2) followed by a third identical buffer is added next. The circuit is completed with an output buffer implemented using a cascode pseudo-differential amplifier. The singled ended output is obtained with a balun and a matching LC circuit to drive an external 50 Ohms load. Figure 3 shows the photograph of the chip ($1.6 \times 0.6 \text{ mm}^2$). The circuit includes on-chip bias and tuning voltage generation using 6 bit digital to analog converters (DAC) and LDO supply regulator [6] controlled by an SPI interface.

III. EXPERIMENTAL RESULTS

A. Free-run operation

In this section, the REF IN input signal is switched off in order to characterize the P-OSC, and the two ILOs (ILO1, ILO2) in free-running operation. Note that all the signals are observed at the output of the circuit. First, the P-OSC and ILO1

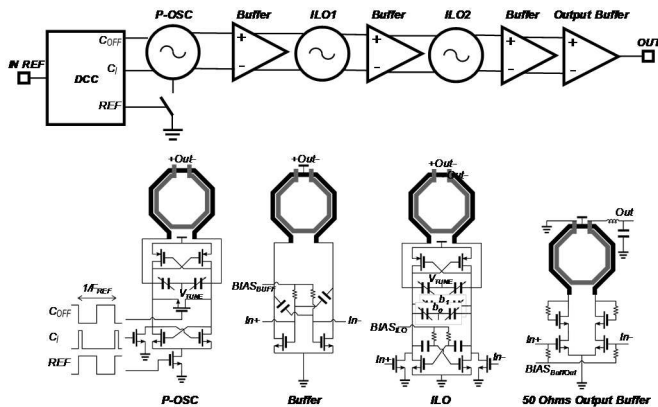


Fig. 2. Frequency synthesizer block diagram and circuit schematics.

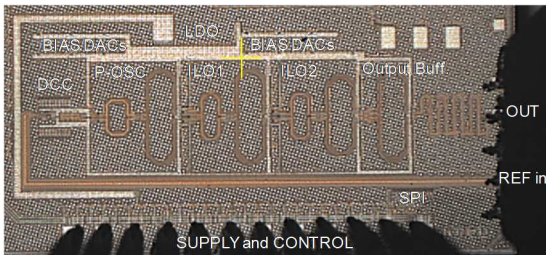


Fig. 3. Fabricated integrated circuit.

oscillators are switched off by setting their bias voltages to 0. In this configuration the ILO2 operates as a free-running oscillator and its frequency can be characterized as a function of the fine tuning voltage and the coarse tuning code (from 00 to 11). The results are shown in Fig. 4 in colored solid lines. Next the ILO1 is turned on and the injection signal to ILO2 is set to the maximum so that the ILO2 can lock on any ILO1 frequency. In this way the free-running oscillation frequency of ILO1 is characterized through ILO2. The results are shown in Fig. 4 as colored dashed lines. Finally the injected signal amplitudes of ILO1 and ILO2 are set to the maximum so that the P-OSC can drive both ILO1 and ILO2 and its free-running frequency can be observed at the output. It is shown in Fig. 4 with a black dashed line. The figure also shows a comparison with post-layout simulation results, indicated with a different symbol for each oscillator. The agreement with the measurements is excellent (better than 1%) and the error are likely due to underestimation of some parasitic capacitances. The right panel of Fig.4 shows the measured output power as a function of the oscillation frequency. Note that the probes and cable insertion losses are not de-embedded in this measurement.

The results of Fig. 4 demonstrate an overall frequency synthesis range from 35 up to 41 GHz (~15.8 % tuning range). The P-OSC circuit does not include a coarse tuning mechanisms and the higher parasitic capacitance of the synchronization circuitry prevents to cover the full frequency range of ILO1 and ILO2 with a single varactor. However this is not an issue since the P-OSC produces a multi-harmonic spectrum when the REF IN signal is activated, and the ILO1 can lock in one of the higher harmonics of P-OSC that falls inside its locking range.

The locking range of the two ILOs is measured next, as shown in Fig. 5, as a function of the injection signal strength. For ILO1 this is done by tuning the free-run frequency of the P-OSC. The injection signal level is adjusted by varying the bias of the P-OSC output buffer. Similarly, the ILO2 locking range is measured by varying the ILO1 free-running frequency and its output buffer bias to control the injection signal strength. The

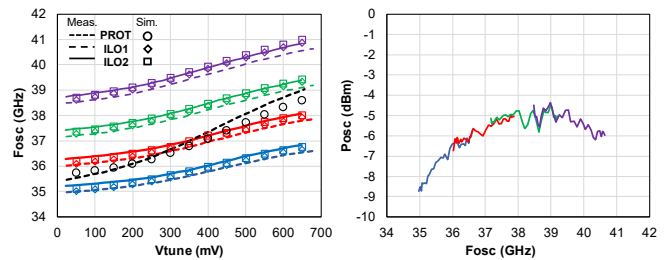


Fig. 4. Free-run oscillation frequencies (left) and output power (right).

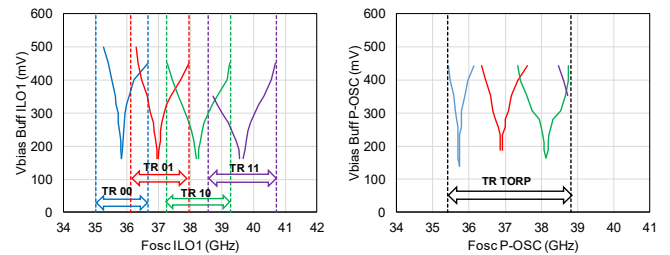


Fig. 5. Locking curves & tuning range (TR) for ILO2 (left) and ILO1 (right).

vertical dashed lines indicate the tuning range of the preceding oscillator. The ILO1 LR observation is limited by the maximum free-running frequency of the P-OSC.

B. Synchronized operation

The proposed frequency synthesizer operates in its normal mode when the REF IN is activated. The frequency of this signal sets the seed for the integer-N multiplication factor that produces the desired output frequency. In order to synthesize a few frequencies covering the full operating range of the ILOs, two different REF IN frequencies are used in this work: 1.2 and 1.25 GHz. The later value allows to synthesize tones at 35, 36.25 and 37.5 GHz (i.e. $N = 28, 29$ and 30 , respectively), as shown in Fig. 6. With 1.2 GHz of REF IN signal, other tones are synthesized using $N = 31, 32, 33$ and 34 , resulting in output frequencies of 37.2, 38.4, 39.6 and 40.8 GHz, respectively. Note that these are the aimed channels (n260), but any frequency between 35 and 41 GHz can be synthesized by choosing the appropriate integer N and REF IN signal frequency values. Due to the multi-harmonic nature of the P-OSC spectrum, some remaining spurs are still present at the output around the desired single tone frequency with more than 50 dBc rejection. However, for the highest frequency tones of Fig. 6 in which the ILO1 has to lock to a harmonic away from the main lobe of the P-OSC spectrum (because of the limited tuning range of the P-OSC), the adjacent spurs are only 34 dBc lower.

The phase noise measured for all the synthesized tones shown in Fig. 7 is better or equal to -97 dBc/Hz at 1 MHz offset and the RMS jitter integrated from 1 KHz to 1 GHz is better than 450 fs, which is a significant achievement. Figure 8 shows the impact on the RMS jitter and on the phase noise of detuning the ILO1 and ILO2 with respect to the position of the desired output tone at 37.2 GHz. Similar results are obtained for the other tone frequencies. As the ILOs approach the boundaries of its locking range, the synchronization mechanism degrades and the jitter and phase noise are impacted. The ILO1 is much more sensitive since the injection strength from the P-OSC is smaller due to its multi-harmonic spectrum, where the energy spreads among the different harmonic terms. The output signal of ILO1 is stronger and the locking range of the ILO2 is therefore larger. Accordingly, the ILO2 can be detuned across a large span without significantly impacting the phase noise and the jitter of the output signal. This is an important feature, as will be seen in the next section where ILO2 tuning is varied to implement phase shifting.

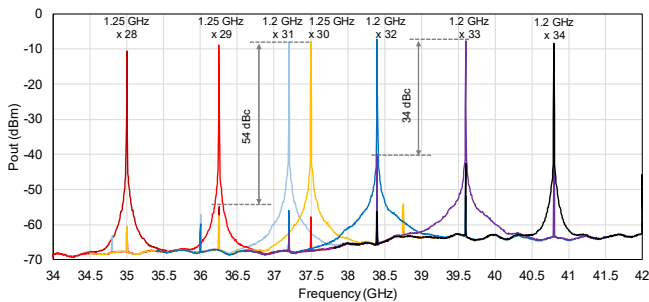


Fig. 6. Some examples of single tone frequencies generated

IV. FREQUENCY SYNTHESIZER AS PHASE SHIFTER

One of the possible approaches for phased arrays implementations is based on introducing the phase shift functionality in the LO chain. In its original paper [11], Adler showed that an oscillator under locking conditions displays a phase difference α between the locking signal (input) and its output such that:

$$\sin \alpha = 2Q \frac{E}{E_{inj}} \frac{\Delta\omega_0}{\omega_0}, \quad (1)$$

where Q is the quality factor of the injected oscillator, E/E_{inj} is the ratio of the oscillator current and the injected current, ω_0 is the injected oscillator free-running frequency and $\Delta\omega_0$ is the difference between the injected signal frequency and ω_0 . This expression indicates that by varying ω_0 , i.e. by changing the tuning voltage of the injected oscillator, the phase difference between the input and the output can be tuned between -90° and $+90^\circ$ within the locking range. This mechanism can be used to implement a phase shift operation using the second ILO2 in the proposed circuit and noting that the first ILO1, which provides the input to ILO2, is perfectly synchronized with the reference input REF IN.

In order to demonstrate this feature, the following experiment is performed: the REF IN signal is split to feed the proposed frequency multiplier and also to trig a high-speed sampling scope. The tone at 38.4 GHz with REF IN at 1.2 GHz and $N = 32$ has been used in this experiment. First, the tuning code of the ILO2 free-running frequency corresponding to the synchronized output signal is selected so that $\Delta\omega_0 = 0$, and a reference waveform is captured by the scope. Next, the tuning code of ILO2 is swept and the phase difference between the reference waveform and the actual output signal is measured on the scope. An average of 1200 samples is used to eliminate the random jitter of the scope converters. An example of the scope waveforms is shown in Fig. 9, left. Since the phase shift

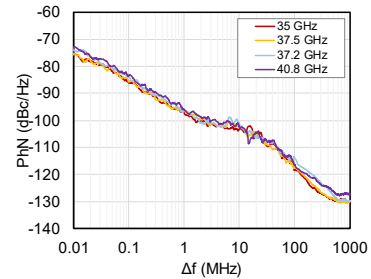


Fig. 7. Phase Noise profiles for several synthesized tones.

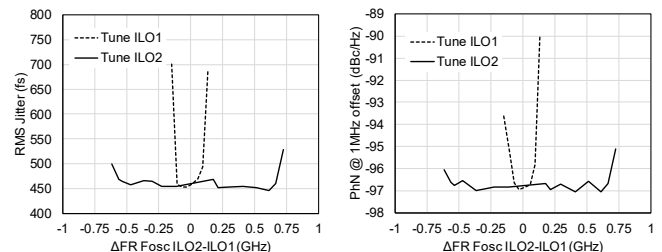


Fig. 8. Impact of ILO1 and ILO2 detuning on phase noise and jitter for the 37.2 GHz tone generated from 1.2 GHz of REF in and $N = 31$.

Table 1. Comparison of the proposed frequency synthesizer with previous works operating in the same frequency range.

	This work	[7]	[8]	[9]	[10]
Topology	Pulsed-oscillator+ ILOs	LC VCO	LC VCO	PLL Push-Push LC VCO	Colpits VCO
Technology	22-nm FDSOI	SiGe	65-nm CMOS	65-nm CMOS	45-nm RFSOI
Frequency (GHz)	35-40.8	35.2-37.6	35.1-40.9	35-41.9	41.1-42.9
PhN @ 1MHz (dBc/Hz)	-97	-99	-94	-97.5	-81
RMS Jitter 1kHz-1GHz (fs)	450	-	-	-	-
P _{DC} (mW)	32.4	84	60	80	25.8
FoM* (dBc/Hz)	174	171	168	171	160
FoM _T * (dBc/Hz)	177	167	172	176	152
FoM _J * (dB)	232	-	-	-	-

$$*FoM = -PhN - 10 \log \left(\left(\frac{1MHz}{Freq.} \right) \left(\frac{P_{DC}}{1mW} \right) \right), FoM_T = FOM + 10 \log \left(\left(\frac{TR\%}{10} \right) \right), FoM_J = -10 \log \left(\left(\frac{Jitter_{rms}}{1s} \right)^2 \left(\frac{P_{DC}}{1mW} \right) \right)$$

depends also on the injection signal strength through the term E/E_{inj} , a couple of measurements are done for two different injection strengths. For the first case (ILO1 Buff Bias code 25), the peak-to-peak phase spans for most of ILO2 tuning range (see Fig. 9, right), but for the lower value (ILO1 Buff Bias code 20), only the center values of the ILO2 tuning range can be used. Outside this range, the ILO2 is not locked by its input, but the ILO1 signal stays synchronized to the REF input. Since the phase noise is not varying significantly across the ILO2 tuning range, this technique can be used to generate a controlled phase shift in the range -90° and $+90^\circ$ with an accuracy of $\pm 3^\circ$ on the signal generated by the proposed frequency synthesizer without affecting its phase noise and jitter performances.

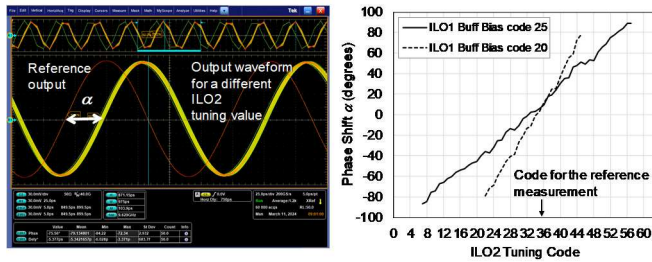


Fig. 9. Impact of ILO1 and ILO2 detuning on phase noise and jitter for the 37.2 GHz tone generated from 1.2 GHz of REF in and N = 31.

V. DISCUSSION AND CONCLUSIONS

This work has presented and demonstrated a frequency synthesizer operating at mmW that covers the 5G FR2 n260 band. Compared with previous works operating in the same band (see Table 1), the proposed circuit achieves one of the lowest phase noise, excellent jitter and a very low power consumption (including the 50 Ohms output buffer), resulting in state-of-art figures of merit.

The proposed frequency synthesizer uses a large integer-N frequency multiplication technique based on a synchronized pulsed oscillator and a couple of injection locked oscillators. It covers a frequency span from 35 up to 40.8 GHz with RMS jitter equal or better than 450 fs integrated over 1kHz – 1GHz band. The phase noise at 1 MHz offset is -97 dBc/Hz and it consumes 32.4 mW including the 50 Ohms output buffer. Realized in 22-nm FDSOI technology it occupies $1.6 \times 0.6 \text{ mm}^2$,

and features integrated LDOs and digital programmability through a standard SPI interface. Thanks to the excellent phase coherence between the input reference and the synthesized output tone the circuit can be used in MIMO architectures either for communications or for radar or localization applications. It offers the additional feature of introducing a fine tuning phase shift on the synthesized signal with respect to the reference, which makes it also a very interesting building block for phased array transceivers based on local-oscillator phase shifting.

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