



**HAL**  
open science

## Wafer-level testing of inverse-designed and adjoint-inspired vertical grating coupler designs compatible with DUV lithography

Thomas van Vaerenbergh, Peng Sun, Sean Hooten, Mudit Jain, Quentin Wilmart, Ashkan Seyedi, Zhihong Huang, Marco Fiorentino, Ray Beausoleil

► **To cite this version:**

Thomas van Vaerenbergh, Peng Sun, Sean Hooten, Mudit Jain, Quentin Wilmart, et al.. Wafer-level testing of inverse-designed and adjoint-inspired vertical grating coupler designs compatible with DUV lithography. *Optics Express*, 2021, 29 (23), pp.37021. 10.1364/oe.433744 . cea-04951392

**HAL Id: cea-04951392**

**<https://cea.hal.science/cea-04951392v1>**

Submitted on 17 Feb 2025

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.




L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution 4.0 International License



# Wafer-level testing of inverse-designed and adjoint-inspired vertical grating coupler designs compatible with DUV lithography

THOMAS VAN VAERENBERGH,<sup>1,\*</sup>  PENG SUN,<sup>2</sup> SEAN HOOTEN,<sup>2</sup>   
MUDIT JAIN,<sup>2</sup> QUENTIN WILMART,<sup>3</sup> ASHKAN SEYEDI,<sup>2</sup> ZHIHONG  
HUANG,<sup>2</sup> MARCO FIORENTINO,<sup>2</sup>  AND RAY BEAUSOLEIL<sup>2</sup>

<sup>1</sup>LSIP Lab, Hewlett Packard Labs, HPE Belgium, B- 1831 Diegem, Belgium

<sup>2</sup>LSIP Lab, Hewlett Packard Labs, Hewlett Packard Enterprise, CA 95035, USA

<sup>3</sup>Univ. Grenoble Alpes, CEA, LETI, F38000 Grenoble, France

\*thomas.van-vaerenbergh@hpe.com

**Abstract:** Perfectly vertical grating couplers have various applications in optical I/O such as connector design, coupling to multicore optical fibers and multilayer silicon photonics. However, it is challenging to achieve perfectly vertical coupling without simultaneously increasing reflection. In this paper, we use the adjoint method as well as an adjoint-inspired methodology to design devices that can be fabricated using only a single-etch step in a c-Si 193 nm DUV immersion lithography process, while maintaining good coupling and low reflection. Wafer-level testing of devices fabricated by a pilot line foundry confirms that both design paradigms result in state-of-the-art experimental insertion loss (<2 dB) and bandwidths (~20 nm) while having only moderate in-band reflection (<-10 dB). Our best design has a (median) 1.82 dB insertion loss and 21.3 nm 1 dB-bandwidth.

© 2021 Optical Society of America under the terms of the [OSA Open Access Publishing Agreement](#)

## 1. Introduction

Grating couplers (GCs) are an appealing and scalable solution for optical I/O in large-scale integrated photonic circuits, because they allow for wafer-level testing. Traditional GC designs avoid coupling light from a waveguide to a fiber which is perfectly perpendicular to the surface of the chip, as it would result in large back-reflection into the waveguide. Instead, in most applications, GC designs are being used that couple to fibers which are tilted slightly off-axis. However, recent advances in automated inverse design techniques using, e.g., the adjoint method [1,2], have opened up new capabilities in photonic device design, resulting in a renewed interest in perfectly vertical GCs as perfect vertical coupling could simplify the design of connectors [3,4], or would allow for coupling to multi-core fibers [5]. Additional applications for perfectly vertical GCs can be expected in the reduction in alignment tolerance in grating coupled lasers [6], optical vias in multi-layer 3D photonics applications [7–9] or optical MRAM [10]. While many of the recently proposed vertical GC designs have appealing insertion loss (IL) and in-waveguide reflection numbers, either in theory [5,11–14] or experiment [5,15], they often have fabrication requirements which might make them less suitable for cost-efficient and scalable fabrication using deep UV (DUV)-lithography. For instance, these designs have critical dimensions which can only be achieved using e-beam lithography [5,11,15], or tight alignment constraints for the different etch steps in the same material layer [13,14] or in different material layers [12]. The manufacturability of vertical GCs can be taken into account either by incorporating design-constraints intrinsically in the inverse design procedure [1,12,16–18], or by avoiding less mature or too elaborate fabrication flows (at expense of higher losses, or higher reflectivity) all together (e.g., by restricting the optimizer to only work with a single etch-step [3,11]).

In this paper, we experimentally characterize the merits of two different design paradigms, hierarchical inverse-design (based on Ref. [1,3,12,19]) and adjoint-inspired design (based on Ref. [20]), for the use-case of perfectly vertical GCs which can be fabricated using a single etch step in a 193 nm DUV immersion lithography process (the foundry provides another deep etch step, but this one is not used for our GC devices). More specifically, extending our preliminary work in Ref. [19], our goal is to design low-loss perfectly vertical single-polarization GCs in the O-band, with moderate reflection. The GCs in this paper have been fabricated on 300 mm silicon-on-insulator (SOI) wafers in a pilot line fab (CEA Leti). For the first time ever, we perform extensive automated wafer-level testing of these fabricated vertical GC devices and, for both design paradigms, we find devices with state-of-the-art experimental IL ( $< 2$  dB), bandwidths ( $\sim 20$  nm) and moderate within-band reflection ( $< -10$  dB).

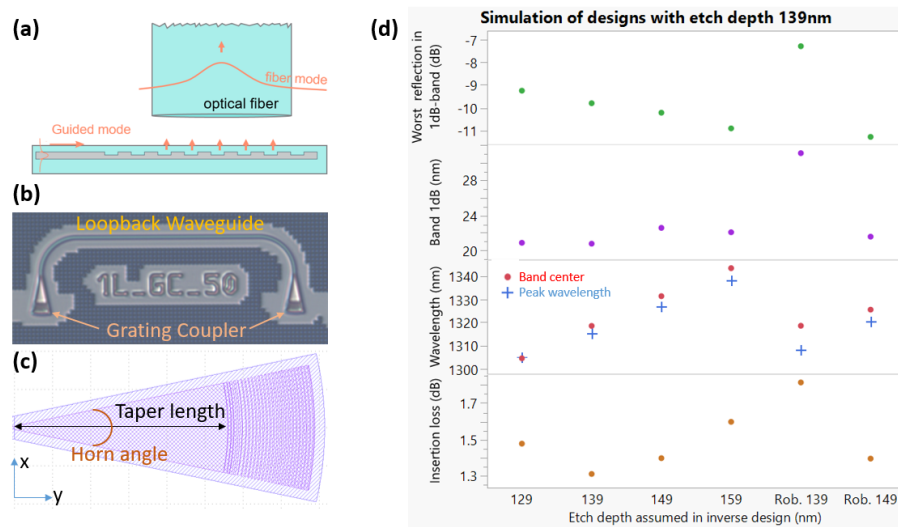
## 2. Rationale of the two types of design of experiments (DOE)

In emerging advanced design methodologies for silicon photonic devices, different paradigms have been proposed to incorporate fabrication constraints in the design flow. One common approach is to add penalties to the desired figure of merit whenever design parameters reach values which are known to be hard or impossible to fabricate. This approach is an alternative to or can be an extension of inverse design flows based on level-set methods [17,18] or pixel-based topology optimization [11], and has frequently been applied in the context of shape-based optimization [1,3,11,12] (in which a high-dimensional parameterization of the surface between different material regions in the devices is optimized, with the parameterization typically based on physics intuition for the given problem). Often, designs benefit from hierarchical design procedures, i.e., the automated design flow contains multiple steps in which, e.g., either different design paradigms are mixed [11] or the importance of the constraints penalties are gradually increased [1,12]. Alternatively, in recent work [20], we have explored the possibility to use the outcome of an unconstrained inverse design optimization as a guideline to formulate parameterized designs with a reduced number of free design variables, such that forward optimization using traditional design of experiments (DOEs) techniques such as factorial experiments of the design variables are feasible within the footprint of a silicon photonic die. Interestingly, in its aim to devise well-performing device parameterizations that only require a very limited number of design variables, the latter design paradigm has some similarities with recently proposed design methodologies inspired by machine learning (ML) techniques such as principal component analysis [13,14]. While a thorough comparison between the adjoint-inspired and ML-inspired techniques is outside the scope of this paper, we expect that these approaches can be complementary, and it is worth noting that both techniques allow for multi-objective optimization [20,21]. Importantly, for optimal robustness against fabrication deviations, we believe that the DOEs generated as part of the adjoint-inspired design methodology should not just be used to select the best device(s) within a simulated DOE, but these DOEs should instead be fabricated. In other words, well-designed DOEs for adjoint-inspired devices should provision for fabrication imperfections in such a way that optimal performance can still be obtained within the *fabricated* DOE, as it is expected that the best performing device(s) in the fabricated DOE will typically be different from the best performing device(s) in the simulated version of the DOE.

In this paper, we will compare the performance of vertical GC devices designed either using hierarchical shape-based inverse design using the adjoint method (DOE explained in Sec. 2.1) or by using an adjoint-inspired design flow (DOEs explained in Sec. 2.2). We use Lumerical FDTD for the 2D FDTD simulation results reported in this section, where a typical simulation takes  $\sim 2$  s on 4 CPU cores (Intel Xeon CPU E7-8890 v3 @ 2.50GHz, on a HP Proliant DL580 Gen9 server with 72 cores). Moreover, IL values are calculated based on an overlap integral with the fiber mode positioned  $2 \mu\text{m}$  above the GC (assuming oxide cladding).

### 2.1. Inverse designed GCs using the adjoint method

In Ref. [3], we obtained a theoretical 1.0 dB IL and 20 nm 1 dB-bandwidth for a perfectly vertical single-layer, single-etch GC (Fig. 1(a)) in SOI for the O-band when assuming a 65 nm minimal feature size (compatible with a 193 nm DUV immersion lithography process), a 159 nm partial etch depth and a 304 nm Si height. In the current work, we designed 0 degree GCs targeting several etch depths (129 nm, 139 nm, 149 nm, 159 nm), assuming the same waveguide height and minimal feature size. We also included two "robust" (Rob.) designs where the figure of merit during optimization included not only the target etch depth, but also two neighboring etch depths (i.e., target etch  $\pm 10$  nm). For this, we used the same hierarchical inverse-design procedures as outlined in Ref. [3], implemented in the open source python package EMopt [22]. Subsequently, a series of loopback test structures optimized for measurements using a fiber array containing these (focusing [23]) GCs (Figs. 1(b)-1(c)) were fabricated in 193 nm DUV immersion lithography by CEA LETI on a 300 mm wafer [24,25], targeting a 139 nm partial etch depth.



**Fig. 1.** (a) Vertical grating couplers (GCs) couple light between a waveguide and a fiber orthogonal to the die surface; (b) Loopback test structures which are compatible with wafer-level testing using fiber arrays; (c) Example GDSII for focused grating; (d) Simulation results of the inverse designed GCs assuming a 139 nm etch depth (Rob.=Robust).

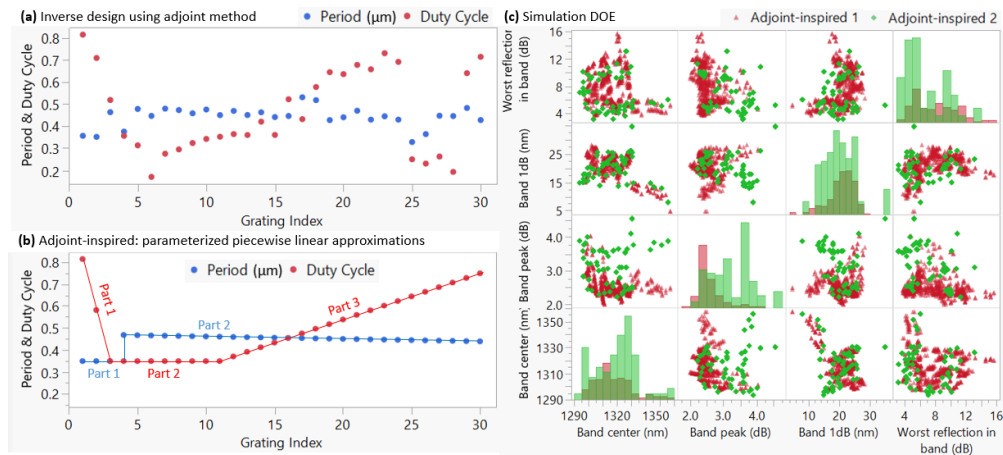
2D Lumerical FDTD-simulations of all the different designs assuming they have been fabricated with this 139 nm etch have  $< 2$  dB IL and  $\geq 20$  nm 1 dB-bandwidth, while only the "Rob. 139 nm" (having a larger 1 dB-BW) compromises on the in-band reflection (Fig. 1(d)). Not surprisingly, the best insertion loss (1.31 dB) is obtained for the device which assumed a 139 nm etch depth in its design.

### 2.2. Adjoint-inspired GCs

The single-etch vertical GC designs generated by the adjoint method tend to have regions with different functionality. More specifically, as has been observed in Ref. [3] by calculating an effective local scattering angle, a first section of the GC will scatter light into a negative (backward) slightly off-axis angle, whereas the remaining part tends to scatter light in a slightly positive off-axis angle. The combination of the different sections results in an effective perfectly vertical scattering over a  $\sim 20$  nm bandwidth. In Ref. [20], when designing 8 degree GCs with wide

(>70 nm) 1 dB-bandwidths for coarse-wavelength division multiplexing (CWDM) applications, we were able to identify sections with distinct functionality as well. Indeed, different sections of the CWDM GC enable wideband operation of the adjoint optimized gratings by stagger tuning two beams with approximately  $5^\circ$  spacing in between. For these CWDM GCs, insight into the physics governing the designs generated by the adjoint method allowed us to come up with simplified multi-section designs which can be easily parameterized and adapted to the fabrication constraints of a given foundry.

In this paper, to test this adjoint-method inspired design methodology proposed in Ref. [20] for another application than CWDM GCs, we have analyzed a set of example geometries by selecting the best performing (in terms of IL and reflection) inverse designed devices for vertical GCs obtained in Sec. 2.1, and we have subsequently developed an (ad hoc) parameterizable piecewise linear approximation scheme that can generate some of the most representative geometric features seen in these example devices (Figs. 2(a)-2(b)). Here, we made the intrinsic assumption that a similar geometry leads to a similar performance. When parameterizing such an adjoint-inspired design DOE, a careful balance needs to be reached between the number of free design variables and the required complexity of the geometry to mimic the physics present in the design generated by the adjoint method. Indeed, more design variables would result in a larger required footprint for the corresponding DOE, whereas the dimensions of more complicated geometries might be harder to monitor during process development. For this work, we have settled on a piecewise linear approximation with 9 design variables, in which the GC's duty cycle (5 variables) contains three continuously connected regions, with the middle region being constant, whereas the period (4 variables) has two regions, of which the first one is constant with a discontinuous jump to the second region. Using this piecewise linear approximation scheme, we have created two adjoint-inspired DOEs. These DOEs differ from each other as they were originally optimized for different dielectric stacks, but both DOEs contain working devices for the wafer studied in this paper. Their parameters were chosen by trial-and-error in simulation, where we swept a representative and fabrication-constrained set of discrete values of the variables describing the piecewise linear parametrization. A first DOE has a factorial of  $1^1 \times 2^6 \times 3^2 = 576$  GC designs (keeping one out of 9 design variables fixed), whereas a second smaller DOE has a factorial of  $1^5 \times 3^4 = 81$  GC designs (keeping 5 out of 9 design variables fixed). In Fig. 2(c), based on FDTD simulations of the corresponding GC designs for the nominal dielectric stack of the fabricated wafer, we have calculated some of the GC's most important performance metrics and have represented the results in a graph matrix. The correlations between these different performance metrics are rather limited. Clearly, in simulation, both DOEs cover a broad range of performance metrics, but the more extensive DOE 1 contains devices with lower loss values (min. 2.0 dB) than DOE 2 (min. 2.2 dB). On the wafer measured in this paper, we have fabricated one GC for every single device in DOE 1, whereas we have included multiple replicas for the devices included in DOE 2 (one third of the devices has been replicated 18 $\times$ , the other devices have been replicated 9 $\times$ , resulting in 976 fabricated devices for DOE 2). The minimal feature size encountered in DOE 1 and DOE 2 are 65 nm and 63 nm, respectively. As a reliable model of possible fabrication deviations was not yet available at the time of design, it was a priori impossible to perform a meaningful variability analysis of these DOEs. This would be useful to improve yield [26] and hence reduce the required size of the DOE. However, we aimed to obtain a broad range of device metrics (e.g., wavelength, IL), expecting this would increase the robustness of the DOEs.



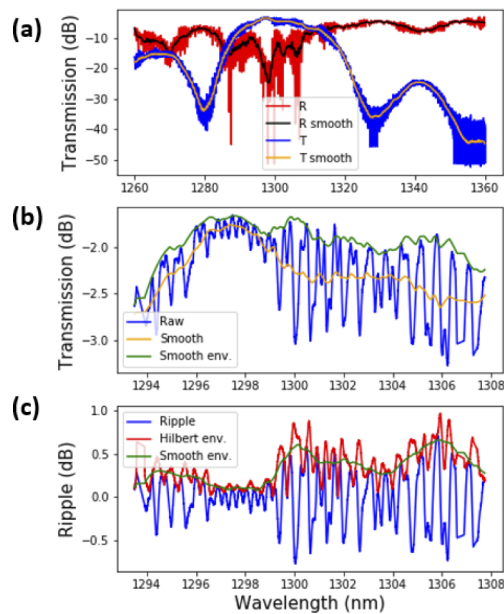
**Fig. 2.** Concept of adjoint-inspired design and corresponding simulation results. (a) Example inverse designed GC using the adjoint method (respecting fabrication constraints). (b) Adjoint-inspired design: parameterized GC with piecewise linear period and duty cycle geometry. (c) Graph matrix with simulation results for two different adjoint-inspired DOEs: adjoint-inspired DOE 1 (red, 576 designs) and DOE 2 (green, 81 designs). For each device we calculate the worst in-band in-waveguide reflection, 1 dB-bandwidth, band center and band peak for vertical GCs. Graphs on the diagonal represent the histograms of the x-axis variable.

### 3. Wafer-level testing and data analysis procedure

Using a 300 mm probe station for automated testing, unless otherwise indicated, we experimentally characterized the fabricated devices using a flat polished fiber array ( $250\ \mu\text{m}$  spacing between fibers) without anti-reflection (AR) coating positioned at  $25\ \mu\text{m}$  above the wafer's top oxide surface. Consequently, in our current experimental set-up reflections at the interfaces between the  $25\ \mu\text{m}$  of air and the top oxide of the wafer and the input/output fibers, respectively, are forming a cavity which depends on the exact position of the fiber array, complicating the repeatability of our measurements. To determine the gauge repeatability and reproducibility (gauge R&R) of our setup, we reloaded our wafer three times, realigned for every wafer load three times to a representative GC design on five different dies, measured each device for each alignment three times, and extracted the insertion loss from the corresponding 27 spectra for each die. From these measurements we extracted the  $6\sigma$  R&R of our setup to be 0.3 dB for 0 degree GCs, which is higher than the 0.1 dB reference value we obtain when measuring 8 degree GCs with angle-polished fibers using the same set-up. Importantly, in eventual applications, such as connectors for optical I/O [4], index-matching epoxy will be deposited in between the fiber and the wafer.

During our measurements, we recorded both the transmission through the loopback test structure, as well as the reflection from the wafer back into the input fiber (Fig. 3(a)). For the latter reflection measurement, as our current fiber array does not contain AR coating, the reflection at the glass-air interface of the fiber facet ( $\sim -16\ \text{dB}$ ) has to be considered when interpreting the results. Moreover, due to an additional GC-GC cavity caused by in-waveguide reflection at the GC, our spectra contain Fabry-Perot fringes with a short  $\sim 0.6\ \text{nm}$  free-spectral range (FSR). To obtain the envelope that corresponds with the transmission spectrum of an isolated GC, we first smoothen the ripples using a Savitzky-Golay filter with 2 nm window (which is wider than the FSR of the GC-GC cavity) and third order polynomials (Fig. 3(b)). Subsequently,

we extract this smoothed spectrum of the raw data to obtain a reflection ripple (Fig. 3(c)). A Hilbert transform [27] on this ripple can be used to extract the envelope of the reflection. We use another Savitzky-Golay filter to smoothen the extracted ripple envelope, which we then add back to the smoothed transmission spectrum to obtain an approximation of the GC transmission envelope (Fig. 3(b)). Additionally, we will use the amplitude of the Fabry-Perot fringes to estimate the magnitude of the in-waveguide reflection of the devices. However, these reflection estimates should be interpreted with caution as this procedure is less reliable than what could be obtained using dedicated reflection test structures based on, e.g., Michelson interferometers [28]. Nevertheless, the general trends and order of magnitudes should remain valid. Note that in Ref. [19], we reported the IL based on the smoothed spectrum of the raw data, in contrast to the current paper, in which the smoothed envelope of the spectrum has been used to calculate the IL. For representative devices, we see a  $\sim 0.1$  dB difference in IL between both methods.



**Fig. 3.** Processing of measured spectra. (a) Recorded raw data for the GC transmission and reflection (back into the input fiber); (b) Zoom of transmission spectra showing both raw data, the smoothed spectra and the envelope obtained using a (smoothed) Hilbert transform. (c) Raw Fabry-Perot ripple (raw data - smoothed spectra) and raw and smoothed Hilbert transform.

We have chosen to characterize our GCs with a fiber array using loopback test structures (Fig. 1(b)), as this leads to higher measurement throughput (only one alignment required per device instead of one for each GC) and, by combining this with a capacitive sensor, also improved measurement reproducibility. Given the small  $250 \mu\text{m}$  spacing between both GCs, changes in etch depth inside the test structure are negligible, and we have verified that the misalignment effect for the worst-case core eccentricity of the fiber array is smaller than 0.1 dB (which is smaller than our gauge R&R). The  $25 \mu\text{m}$  fiber height is chosen to reduce the risk to damage the fiber array during the measurements, while still maintaining a moderate excess loss given the fiber's  $\sim 50 \mu\text{m}$  Rayleigh length. The biggest contribution to the excess loss due to this non-zero fiber height is the curvature in phase front, which leads to a 0.26 dB loss penalty compared to the  $2 \mu\text{m}$  fiber height used in our simulations [29].

## 4. Analysis of the full DOE

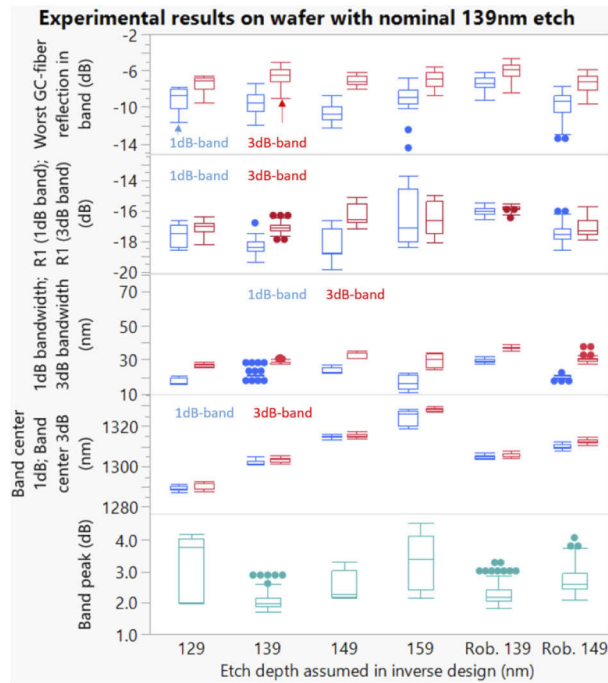
In this section, we analyze the respective DOEs introduced in Sec. 2 by performing measurements of all 1608 vertical GCs included in the different DOEs on five different dies of the same wafer.

### 4.1. Five-die measurement of inverse designed DOE

To compare the different GC designs introduced in Fig. 1, for GCs on five different dies, we have extracted the band peak (i.e., peak IL), band center (this metric is less sensitive to reflection ripples), 1 dB-/3 dB-bandwidths (BW<sub>s</sub>), an estimate of the in-waveguide reflection (R<sub>1</sub>, averaged over the 1 dB-/3 dB-band), and the maximum 1 dB/3 dB in-band GC-fiber reflection (Fig. 4). Here, as higher reflection in some designs might result in Fabry-Perot ripples in the transmission spectrum that could potentially make the 1 dB-based metrics less reliable, we choose to report metrics for both the 1 dB-band (which is generally reported for GCs [3,11,12,20]) and 3 dB-band (sometimes used for vertical GCs [5,15]). In principle, it is up to the system designer to determine which metric (1 dB- or 3 dB-band) is relevant for a certain application. The box plots in Fig. 4 represent the performance distributions for a given adjoint design by combining the measurement results of five different dies, three alignment attempts (at 1300 nm, 1310 nm and 1320 nm, respectively), which amounts to 15 measurements per device design. For these designs, we used a horn angle of 24° and a taper length of 28 μm. For design target etch depths 139 nm, Rob. 139 nm and Rob. 149 nm, we additionally included 5-die measurements of a DOE which takes the factorial of three different choices of horn angle (20°, 24° and 28°) and four different choices of taper length (20 μm, 24 μm, 28 μm and 32 μm), which, combined with the previous set of measurements, leads to 180 + 15 = 195 measurements for these design etch depths. Similarly to our simulation results, the best performing device for the band peak is the GC that has been designed for a nominal 139 nm etch depth. For this grating corrugation design, the corresponding focusing GCs have a 21.2 nm median 1 dB-BW, and while the measured GC-fiber reflection is undesirably high due to the lack of index-matching epoxy or oxide between the fiber and the wafer in our set-up, the in-waveguide reflection estimate R<sub>1</sub> is well below -10 dB. As for the taper design, we noticed best performance for long taper lengths (28 μm and 32 μm) and a horn angle of 24°.

While this paper focuses on automated measurement methodologies that are compatible with wafer-level testing of vertical GC DOEs, we have also performed an initial test of the design of record (DOR) device (i.e., the best device of our DOE, more details in Sec. 5) on a representative die using deionized (DI) water ( $n = 1.32$ ) as index matching fluid between the fibers and the wafer's top oxide. For this measurement series, we aligned the fiber array to our best GC on a representative die, and obtained a new gauge R&R estimate by performing three repeat measurements for three XY-realignments both before and after manually adding the DI water droplets. Whereas the gauge R&R for this single die measurement does not improve (~ 0.2 dB for both measurement series), our data indicates that the reduction in reflection in the GC-fiber cavity due to adding DI water reduces the coupling loss compared to the air interface by 0.1 dB. As expected, we obtained no significant changes in our in-waveguide reflection estimates, as adding DI water has negligible influence on the amplitude of the corresponding GC-GC cavity reflection ripples. In principle, an approach to avoid measurement parasitics due to the top oxide-air interface which is compatible with wafer-scale automated testing would be to process an anti-reflection coating at the top oxide [30,31]. However, such an AR coating might not be compatible with further processing steps required to embed the vertical GCs inside connector designs, in which this spurious reflection issue is most likely already solved as connector designs often incorporate an index-matching epoxy in between the top oxide and the fiber [4]. A more straight forward improvement of our measurement procedure would be to include an AR-coated fiber array. Unfortunately, we did not have access to such a fiber array during the measurements reported in this paper.





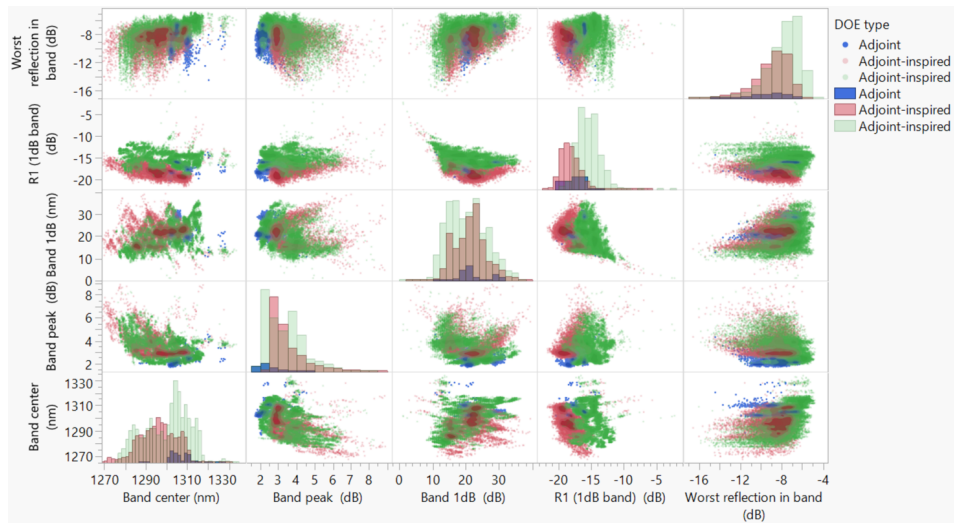
**Fig. 4.** Experimental characterization of the devices simulated in Fig. 1 fabricated on an SOI wafer with 139 nm partial etch. Worst in-band GC-fiber reflection, estimate of in-waveguide GC-GC reflection (integrated over 1 dB-/3 dB-band), 1 dB-/3 dB-bandwidth, band center and band peak for vertical GCs. Measurement results obtained using wafer-level testing on five different dies. Dots represent outliers, and we show 15 data points for target design etch depths 129 nm, 149 nm and 159 nm, while 195 data points are included for the other design etch depths.

#### 4.2. Five-die measurement of adjoint-inspired DOEs

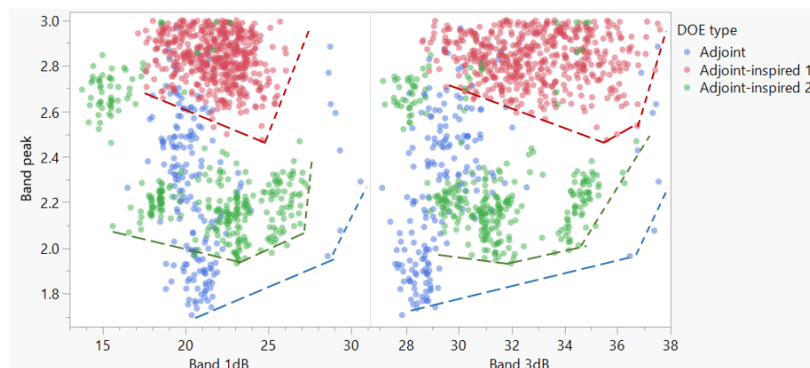
In Fig. 5, we summarize some of the most important GC specs for a five-die measurement of the two adjoint-inspired DOEs discussed in Sec. 2.2 in a graph matrix (only for the 1 dB-band, as 3 dB-band figures result in similar trends). As a reference, we have also included the corresponding measurement results from devices designed using the adjoint method. In this ensemble of measurements, which contains three alignment attempts (using either 1300, 1310 or 1320 nm) for five dies with each 1608 devices, we have excluded 5 outlier measurements with a peak loss larger than 10 dB. As can be expected, the two adjoint-inspired device DOEs cover a wider range in insertion loss, center wavelength, bandwidths and reflection metrics than the inverse-designed DOE. In contrast to the 2D FDTD simulations (Sec. 2.2), adjoint-inspired (AI) DOE 2 (min. 1.83 dB, median 3.18 dB) has a better minimal band peak measurement than AI DOE 1 (min. 2.35 dB, median 3.10 dB). In agreement with simulation results, both parameterized DOEs have a worse minimal IL than the inverse-designed (ID) DOE (min. 1.71 dB, median 2.28 dB). Surprisingly, the best IL measurement for DOE 2 is  $\sim 0.4$  dB better than expected based on simulation results, whereas we have a  $\sim 0.5$  dB increase in loss for the inverse-designed DOE. When comparing the median (out of 5 dies) measured IL for the specific devices that gave the best experimental IL measurement within each DOE, using the optimal alignment wavelength, we obtain experimentally (versus simulated IL for this design): 1.77 dB (1.31 dB) for ID DOE, 2.50 dB (2.27 dB) for AI DOE 1 and 2.11 dB (2.79 dB) for AI DOE 2. Interestingly, when contrasting the experimentally obtained median IL of the best devices of each DOE with

the simulated prediction for minimal IL reported in Sec. 2.1 (1.31 dB for ID DOE, 2.00 dB for AI DOE 1 and 2.22 dB for AI DOE 2), AI DOE 2 suffers less from the expected performance hit due to fabrication imperfections than the DOE for the inverse-designed devices (in fact, it performs even better than simulations). While this is just one data point for a certain device type given the foundry's specific fabrication process, this suggests that in some cases the adjoint-inspired design methodology might generate DOEs that are more robust against fabrication deviations than DOEs consisting of a limited set of devices directly designed using inverse design. For the wafer studied in this paper, this mismatch between simulation and experiment might be caused due to a lack of adaptation of the used optimal-proximity correction (OPC) algorithm to the specific GC design of interest [24]. Whereas adaptation of the OPC algorithm might improve the losses for the inverse designed devices, it risks to reduce the performance of the adjoint-inspired devices. Alternatively, a study of micrographs of the fabricated adjoint-inspired devices might result in new parameter schemes that maintain decent performance while applying more advanced OPC.

Despite this slight increase in experimental loss compared to the inverse-design DOE, the parameterized DOEs still have their value as they can be used for selection of devices that need to satisfy multiple constraints or, alternatively, in the context of multi-objective optimization. For instance, in Fig. 6, for devices with insertion loss smaller than 3 dB, we have tracked the trends of the band peak versus the 1 dB- and 3 dB-band, respectively. As an example of multi-objective constraints, we have excluded all the measurements which do not satisfy the following constraints: (a) 1310 nm alignment wavelength, (b) center band  $\in [1300 \text{ nm}, 1320 \text{ nm}]$ , (c) Maximum in-band GC-fiber reflection  $\leq -8 \text{ dB}$ , (d) R1 (for the 1 dB-band)  $\leq -10 \text{ dB}$ . While the measurements seem to suggest that the convex hull of the inverse designed devices might still perform slightly better in the loss versus bandwidth trade-off, for the 1 dB-band, we are lacking measurements in the 22 – 28 nm 1 dB-bandwidth range that confirm our convex hull assumption. Dedicated adjoint-optimization runs with altered figure of merits for the desired loss vs bandwidth trade-off would be needed to produce a more densely populated convex hull. In contrast, the bigger DOEs of the parameterized devices have as an advantage that they cover their respective convex hulls in a more dense way, and as long as the set of devices is sufficiently large and the individual parameter ranges are well-centered, no compute-intensive optimization runs are required to boost performance of individual devices inside these DOEs. In other words, when sufficient mask space is available to allow for large DOEs, the larger parameterized DOEs allow one to generate devices that cover a sufficiently broad range of specs such that system engineers can easily post-select their desired devices from an experimental DOE given the specs corresponding to their specific applications (specs which might not always be known a priori). In contrast, the pure adjoint-method inverse designed devices require more design effort upfront (an effort which in some applications might be well justified if mask space is small, or when significantly better convex hulls can be obtained).



**Fig. 5.** Experimental characterization of the devices from adjoint-inspired DOE 1 (red, 576 devices) and DOE 2 (green, 976 devices) simulated in Fig. 2, with the inverse designs discussed in Sec. 4.1 as a reference in blue (56 devices, including the 42 designs analyzed in Fig. 4 and 14 additional designs, part of an eccentricity sweep for 139 nm and Rob. 149 nm). Worst in-band GC-fiber reflection, R1 estimate of in-waveguide GC-GC reflection (integrated over 1 dB-band), 1 dB-bandwidth, band center and band peak for vertical GCs. Measurement results obtained using wafer-level testing on five different dies. Similar trends can be obtained for metrics related to the 3 dB-band.



**Fig. 6.** Band peak versus 1 dB- and 3 dB-band of measurements satisfying certain constraints: (a) 1310 nm alignment wavelength, (b) center band  $\in [1300 \text{ nm}, 1320 \text{ nm}]$ , (c) Maximum in-band reflection  $\leq -8 \text{ dB}$ , (d) R1 (1 dB-band)  $\leq -10 \text{ dB}$ . Dashed lines suggest relevant convex hulls for the respective DOEs.

## 5. Full wafer-level testing of design of record (DOR)

In addition to the previous five-die measurements, we performed measurements of our DOR on 67 wafer dies. As the devices based on adjoint optimization with nominal 139 nm etch depth performed best, we picked the best design in this category as DOR. This design has optimal horn angle (24 degree), taper length (28  $\mu\text{m}$ ) and 0 eccentricity.

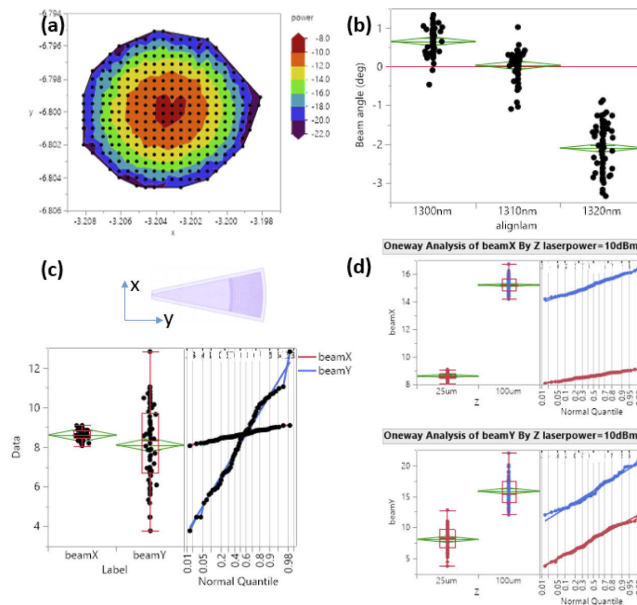
### 5.1. Performance metrics of DOR

The full wafer-level testing of the DOR results in a (median) IL of 1.82 dB and a 20.5 nm 1 dB-BW (28.1 nm 3 dB-BW) and 1 dB in-band R1 reflectivity of  $-16.5$  dB. The peak loss is 0.51 dB higher than our corresponding 2D FDTD simulation (see Sec. 2.1), which can be attributed due to several reasons: a) 0.26 dB excess loss due to phase front curvature (Sec. 3); b) a 0.1 dB penalty as the actual Si height was 299.3 nm instead of 304 nm assumed in simulations (the foundry adapted the etch depth correspondingly, such that the remaining Si thickness  $304 \text{ nm} - 139 \text{ nm} = 165 \text{ nm}$  was still on spec); c) while we used optical proximity correction (OPC) for our GCs, the OPC process was not optimized for these specific devices resulting in slight deviations in the grating dimensions (observed deviations were more significant for smaller feature sizes: 13% for 60 nm, with a  $3\sigma$  of 2.1 nm, versus 6.5% for 400 nm, with a  $3\sigma$  of 3.9 nm); d) in the current process the actual depth of the partial etch of different grating lines is width dependent (in narrow trenches, close to 60 nm width, there will be +5 to +15 nm more remaining Si left), which has a priori not been taken into account in our device design; e) limitations due to intrinsic reflections in our current measurement setup (due to the air gap instead of oxide cladding, see Sec. 3). Importantly, in this paper, when reporting GC metrics, we apply the data processing procedure based on the Hilbert transform introduced in Sec. 3. Omitting the envelope extraction provided by the Hilbert transform in the data analysis would typically result in an overestimate of the loss (e.g., IL estimate of 1.91 dB for the DOR), and underestimate of the band widths (e.g., 18.9 nm 1 dB-BW and 26.9 nm 3 dB-BW estimates for the DOR).

To put these numbers in perspective, for the default O-band 8 degree GC in the foundry's PDK, we obtained an IL of 2.4 dB with a 20.8 nm 1 dB-bandwidth. By taking full advantage of a similar (single-etch) 193 nm DUV dry lithography process and targeted OPC, a 1.35 dB IL can be obtained for 8 degree GCs (reported in Ref. [24], design not included on our immersion lithography wafer). As an alternative data point, for a different layer stack and targeting the C-band, an experimental dual-etch apodized perfectly vertical GC fabricated using e-beam lithography was reported to have an experimental IL of 1.5 dB (0.6 dB in simulation) and 49 nm 3 dB-bandwidth, with a minimal feature size of 30 nm [5]. The 30 nm critical dimension is incompatible with DUV lithography. In contrast to our measurement procedure, these numbers were obtained with a single fiber-in and single fiber-out measurement setup by measuring a single device. The difference in measurement procedure, layer stack and target wavelength complicate a direct comparison with our own results. Theoretic work reported in Refs. [13,14,21] indicates that inserting subwavelength features increases the required minimal feature sizes, opening up the way towards fabrication using DUV lithography. This suggest that for certain layer stacks a dual etch vertical GC *might* eventually obtain better performance metrics than the single-etch vertical GC reported in this paper, as long as the foundry choice and cost constraints for a certain application are compatible with the etch-step alignment specifications required to obtain sufficiently high yield.

### 5.2. Mode profile and beam angle of DOR

The data shown in Fig. 4 was extracted from measurements obtained at the same fiber height (25  $\mu\text{m}$ ), with the fiber array's XY-fiber position determined by an automated alignment routine at one of three different alignment wavelengths (1300 nm, 1310 nm or 1320 nm). As an additional

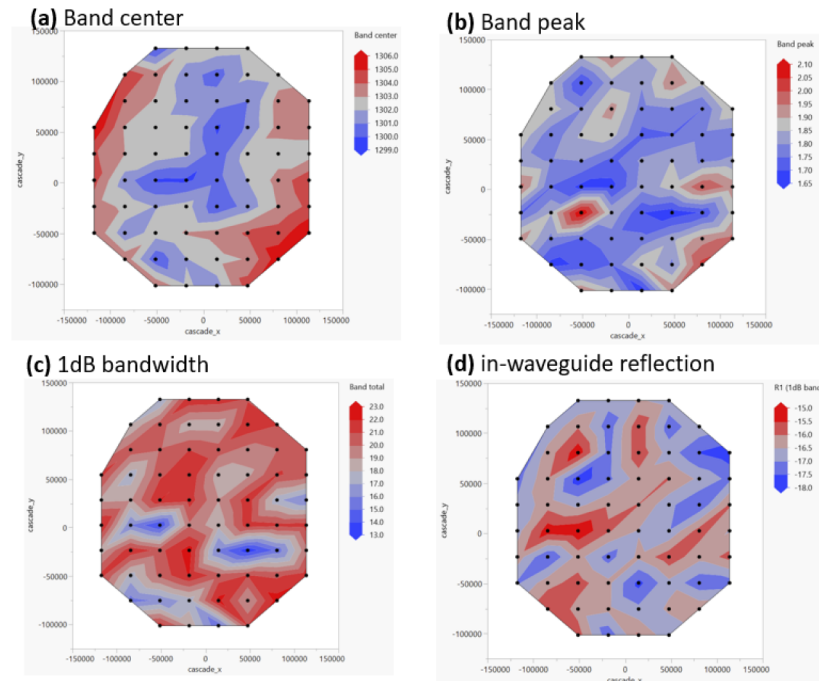


**Fig. 7.** (a) Power map for design of record (DOR) on one of the wafer dies; (b) DOR angles for different alignment wavelengths; (c) Beam width distributions at fiber array height  $h = 25 \mu\text{m}$  in the X and Y dimension; (d) Beam width expansion between heights  $25 \mu\text{m}$  and  $100 \mu\text{m}$ .

characterization of the DOR, we determined a power map for the DOR in one of the dies (Fig. 7(a)), which corresponds to the convolution of the fiber modes with the DOR's mode profile. As expected, we obtain a smooth, uni-modal power distribution. Subsequently, we have tracked the fiber array alignment positions at different alignment wavelengths at four different heights:  $25 \mu\text{m}$ ,  $45 \mu\text{m}$ ,  $65 \mu\text{m}$  and  $85 \mu\text{m}$  (Fig. 7(b)). This measurement allows us to estimate the beam angle of the GC at these different wavelengths, and we obtain the desired 0 degree coupling at 1310 nm (the GC's band center is 1305 nm). Furthermore, we have expanded the analysis of Fig. 7(a) to all dies and we extracted an estimate for the GC beam width by fitting a parabola to the logarithmic power maps for the DOR obtained for all dies at heights  $25 \mu\text{m}$  and  $100 \mu\text{m}$ . In this calculation, we assumed a Mode Field Diameter (MFD) of the fiber to be  $9.2 \mu\text{m}$ . However, we have not independently verified this MFD, and for the polarization maintaining fibers used in our setup, the spec provided by the vendor is  $10.3 \mu\text{m}$ . Consequently, the obtained values of the beam widths should be considered to be estimates of the real beam widths. Nevertheless, the trends in these numbers are still meaningful. For instance, the extracted data allows us to observe that the spread in beam widths is wider for the Y-dimension than for the X-dimension (Fig. 7(c)). This is in agreement with expectations as the beam width in the X-dimension is determined by taper length and horn angle whereas it is not affected by lithography and the etch depth, so the spread is very tight. In contrast, the beam width in the Y-dimension is determined by the grating apodization along the longitudinal axis, and it is significantly affected by lithography and etch, making the spread larger. In addition, by comparing the respective beam widths at height  $25 \mu\text{m}$  and  $100 \mu\text{m}$  (Fig. 7(d)), we obtain an expected increase in beam width of  $\sim 2\times$ , which is in line with what can be obtained using a Rayleigh length of  $\approx 50 \mu\text{m}$ .

### 5.3. Wafer maps of DOR

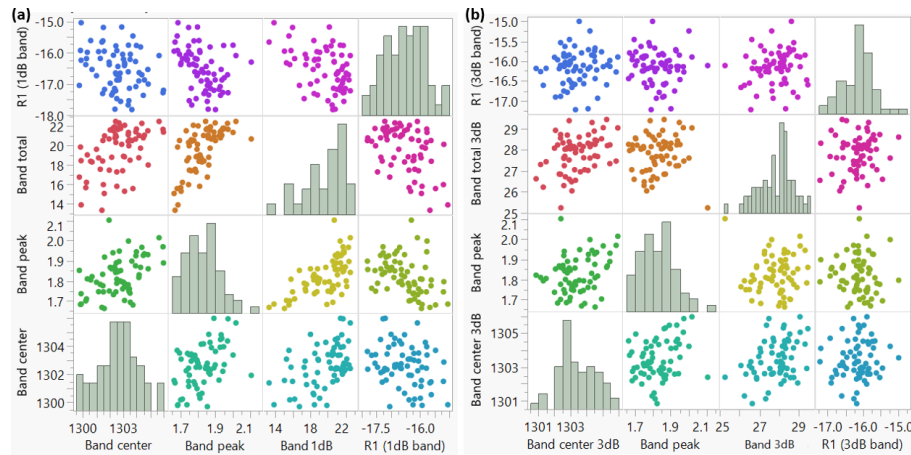
Additionally, we have made wafer maps of the DOR measurements at  $25\ \mu\text{m}$  height for four important wafer metrics: (a) band center wavelength; (b) band peak; (c) 1 dB-bandwidth; (d) in-waveguide reflection (Fig. 8). We observe lower band center wavelengths in the center of the wafer, compared to the east and west sided edges of the wafer. The magnitude and type of pattern is consistent with etch depth variations over the wafer surface [24]. Specifically, for the wafer of interest, using inline metrology, we extracted a maximum of 4 nm etch depth variation between center and edge. Assuming constant etch depths over the whole GC, for this etch depth range, our 2D FDTD simulations predict a 4.5 nm range for the band center. So, the observed band center spread is indeed mainly driven by etch depth variations. The other three GC specs we have tracked in these wafer maps do not have such a direct correlation with the etch depth variations (e.g., FDTD simulations would only predict a 0.1 dB spread in IL), and their spatial patterns contain less structure. As the correlations between process and device performance are non-trivial, we consider these vertical GCs to be too complicated to act as reliable proxies for fabrication bias. Consequently, to obtain more insight in how the fabrication process precisely affects our devices, additional DOEs containing less complicated photonic devices such as ring resonators, directional couplers or multi-mode interferometers would be required [26,32].



**Fig. 8.** Wafer-Level Testing (WLT) of DOR (a) Band center; (b) Band peak; (c) 1 dB-bandwidth; (d) In-waveguide reflection.

Finally, we have also assembled graph matrices which track the correlations and distributions of the DOR's WLT data (Fig. 9). We have assembled graph matrices both for wafer specs calculated for a 1 dB-band and for a 3 dB-band. Consequently, only the band peak values are identical between the two graphs, whereas all other numbers are adapted to the respective band choice. Interestingly, for the 1 dB-band version, we obtain a stronger correlation between the band peak and the bandwidth than for the 3 dB-band. This is to be expected, as the calculation of the 1 dB-bandwidth is more sensitive to the spectrum's reflection ripples. Furthermore, the

calculated in-waveguide reflection values seem robust with respect to the bandwidth choice as the range of R1 values for both bands are comparable.



**Fig. 9.** Graph matrix showing correlations and distributions of Band center, Band peak, bandwidth, In-waveguide reflection obtained during WLT of the DOR: (a) 1 dB-band, (b) 3 dB-band.

## 6. Conclusion

Perfectly vertical GCs might have applications in coupling to multi-core fibers or might simplify connector designs for optical I/O. We used both inverse design techniques and adjoint-inspired design techniques to design single-layer, single-polarization, and single-etch vertical GCs in SOI. Wafer-level testing with a 0.3 dB R&R gauge was performed on the resulting devices. Five-die measurements indicate that the best inverse designed devices outperform the best adjoint-inspired designed devices. However, both design paradigms result in devices with state-of-the-art experimental IL ( $< 2$  dB) and bandwidths ( $\sim 20$  nm) and moderate within-band reflection ( $< -10$  dB). Specifically, when testing our best design on all 67 dies, we obtain a (median) 1.82 dB IL, 21.3 nm 1 dB-BW with  $< -10$  dB in-waveguide reflection. As an alternative to increasing the etch depth [3], we expect that our single-etch GC could be improved by using an effective blazing functionality by leveraging subwavelength techniques, similar to recent proposals for dual-etch designs [5,13,14]. In addition, as previously proposed [3], alignment-tolerant multi-layer designs in a SiN-on-silicon platform [33,34] might allow for further improvement in vertical GC performance as well.

**Funding.** Hewlett Packard Enterprise.

**Acknowledgments.** The authors thank D. Fowler for help in calibrating our wafer probe station, the clean room staff of CEA-LETI for assistance in device fabrication and G. Kurczveil and S. Srinivasan for insightful discussions on AR-coatings for wafers and reflection test structures.

**Disclosures.** S. Hooten, T. Van Vaerenbergh, P. Sun, R. G. Beausoleil have a related granted patent (US10884192B1) on single-etch wideband GCs. The authors declare no further conflicts of interest.

**Data availability.** Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

## References

1. A. Michaels, M. C. Wu, and E. Yablonovitch, "Hierarchical Design and Optimization of Silicon Photonics," *IEEE J. Sel. Top. Quantum Electron.* **26**(2), 1–12 (2020).
2. S. Molesky, Z. Lin, A. Y. Piggott, W. Jin, J. Vucković, and A. W. Rodriguez, "Inverse design in nanophotonics," *Nat. Photonics* **12**(11), 659–670 (2018).

3. S. Hooten, T. Van Vaerenbergh, P. Sun, S. Mathai, Z. Huang, and R. G. Beausoleil, "Adjoint Optimization of Efficient CMOS-Compatible Si-SiN Vertical Grating Couplers for DWDM Applications," *J. Lightwave Technol.* **38**(13), 3422–3430 (2020).
4. S. Mathai, P. Rosenberg, G. Panotopoulos, D. Kurtz, D. Childers, T. Van Vaerenbergh, P. Sun, J. Hulme, J. Rhim, A. Seyedi, M. Tan, and M. Fiorentino, "Detachable 1x8 single mode optical interface for DWDM microring silicon photonic transceivers," *Proc. SPIE* **11286**, 112860A (2020).
5. T. Watanabe, M. Ayata, U. Koch, Y. Fedoryshyn, and J. Leuthold, "Perpendicular grating coupler based on a blazed antireflection structure," *J. Lightwave Technol.* **35**(21), 4663–4669 (2017).
6. S. Lin, D. Wang, F. Khan, J. Chen, A. Nickel, B. Kim, Y. Matsui, B. Young, M. Kwakernaak, G. Carey, and T. Sudo, "Grating coupled laser (GCL) for Si photonics," *Opt. InfoBase Conf. Pap. Part F174-OFC 2020*, 5–7 (2020).
7. A. Michaels and E. Yablonovitch, "High density multilayer optical circuit board for unprecedented connectivity at board scales," in *Proceedings of 2016 IEEE International Conference on Rebooting Computing, ICRC 2016*, (2016).
8. K. Shang, S. Pathak, B. Guan, G. Liu, and S. J. B. Yoo, "Low-loss compact multilayer silicon nitride platform for 3D photonic integrated circuits," *Opt. Express* **23**(16), 21334 (2015).
9. D. A. Miller, "Attojoule Optoelectronics for Low-Energy Information Processing and Communications," *J. Lightwave Technol.* **35**(3), 346–396 (2017).
10. H. Becker, C. Kruckel, D. Van Thourhout, and M. Heck, "Out-of-Plane Focusing Grating Couplers for Silicon Photonics Integration with Optical MRAM Technology," *IEEE J. Sel. Top. Quantum Electron.* **26**(2), 1–8 (2020).
11. L. Su, R. Trivedi, N. V. Sapra, A. Y. Piggott, D. Vercruyse, and J. Vučković, "Fully-automated optimization of grating couplers," *Opt. Express* **26**(4), 4023 (2018).
12. A. Michaels and E. Yablonovitch, "Inverse design of near unity efficiency perfectly vertical grating couplers," *Opt. Express* **26**(4), 4766–4779 (2018).
13. D. Melati, Y. Grinberg, M. Kamandar Dezfouli, S. Janz, P. Cheben, J. H. Schmid, A. Sánchez-Postigo, and D. X. Xu, "Mapping the global design space of nanophotonic components using machine learning pattern recognition," *Nat. Commun.* **10**(1), 4775–4779 (2019).
14. M. Kamandar Dezfouli, Y. Grinberg, D. Melati, P. Cheben, J. Schmid, A. Sánchez-Postigo, A. Ortega-Moñux, J. G. Wangüemert-Pérez, R. Cheriton, S. Janz, and D.-X. Xu, "Perfectly vertical surface grating couplers using subwavelength engineering for increased feature sizes," *Opt. Lett.* **45**(13), 3701–3704 (2020).
15. T. Watanabe, Y. Fedoryshyn, and J. Leuthold, "2-D Grating Couplers for Vertical Fiber Coupling in Two Polarizations," *IEEE Photonics J.* **11**(4), 1–9 (2019).
16. D. Vercruyse, N. V. Sapra, L. Su, R. Trivedi, and J. Vučković, "Analytical level set fabrication constraints for inverse design," *Sci. Rep.* **9**(1), 8999 (2019).
17. A. Y. Piggott, J. Petykiewicz, L. Su, and J. Vučković, "Fabrication-constrained nanophotonic inverse design," *Sci. Rep.* **7**(1), 1786 (2017).
18. A. Y. Piggott, E. Y. Ma, L. Su, G. H. Ahn, N. V. Sapra, D. Vercruyse, A. M. Netherton, A. S. Khope, J. E. Bowers, and J. Vučković, "Inverse-Designed Photonics for Semiconductor Foundries," *ACS Photonics* **7**(3), 569–575 (2020).
19. T. Van Vaerenbergh, S. Hooten, P. Sun, M. Jain, A. Seyedi, Z. Huang, M. Fiorentino, and R. Beausoleil, "Experimental characterization of Inverse-Designed Vertical Grating Couplers in the O-band," in *Proceedings of 2021 IEEE Photonics Conference*, (to be published).
20. P. Sun, T. Van Vaerenbergh, M. Fiorentino, and R. Beausoleil, "Adjoint-method-inspired grating couplers for CWDM O-band applications," *Opt. Express* **28**(3), 3756–3767 (2020).
21. D. Melati, M. Kamandar Dezfouli, Y. Grinberg, J. H. Schmid, R. Cheriton, S. Janz, P. Cheben, and D. X. Xu, "Design of Compact and Efficient Silicon Photonic Micro Antennas with Perfectly Vertical Emission," *IEEE J. Sel. Top. Quantum Electron.* **27**(1), 1–10 (2021).
22. A. Michaels, "Emopt: Electromagnetic optimization toolbox," <https://github.com/anstmichaels/emopt> (2021).
23. F. Van Laere, T. Claes, J. Schrauwen, S. Scheerlinck, W. Bogaerts, D. Taillaert, L. O'Faolain, D. Van Thourhout, and R. Baets, "Compact focusing grating couplers for silicon-on-insulator integrated circuits," *IEEE Photonics Technol. Lett.* **19**(23), 1919–1921 (2007).
24. D. Fowler, P. Grosse, F. Gays, B. Szlag, C. Baudot, N. Vuillet, J. Planchot, and F. Boeuf, "Fiber grating coupler development for Si-photonics process design kits at CEA-LETI," *Proc. SPIE* **10922**, 1092205 (2019).
25. R. L. Tiec, S. Levi, A. Kravtsov, O. Novak, C. Dupre, C. Vannuffel, T. Dewolf, S. Garcia, Q. Wilmart, and J. Faugier-Tovar, "Advanced roughness characterization for 300mm Si photonics patterning and optimization," *Proc. SPIE* **11690**, 116900K (2021).
26. W. Bogaerts, Y. Xing, and U. Khan, "Layout-Aware Variability Analysis, Yield Prediction, and Optimization in Photonic Integrated Circuits," *IEEE J. Sel. Top. Quantum Electron.* **25**(5), 1–13 (2019).
27. L. Cohen, "Time-frequency distributions-a review," *Proc. IEEE* **77**(7), 941–981 (1989).
28. E. Kleijn, M. K. Smit, and X. J. Leijtens, "Multimode interference reflectors: A new class of components for photonic integrated circuits," *J. Lightwave Technol.* **31**(18), 3055–3063 (2013).
29. W. B. Joyce and B. C. DeLoach, "Alignment of gaussian beams," *Appl. Opt.* **23**(23), 4187–4196 (1984).
30. E. E. Perl, W. E. McMahon, R. M. Farrell, S. P. Denbaars, J. S. Speck, and J. E. Bowers, "Surface structured optical coatings with near-perfect broadband and wide-angle antireflective properties," *Nano Lett.* **14**(10), 5960–5964 (2014).
31. E. E. Perl, C. T. Lin, W. E. McMahon, D. J. Friedman, and J. E. Bowers, "Ultrabroadband and wide-angle hybrid antireflection coatings with nanostructures," *IEEE J. Photovoltaics* **4**(3), 962–967 (2014).



32. P. Sun, J. Hulme, T. Van Vaerenbergh, J. Rhim, C. Baudot, F. Boeuf, N. Vulliet, A. Seyedi, M. Fiorentino, and R. G. Beausoleil, "Statistical behavioral models of silicon ring resonators at a commercial cmos foundry," *IEEE J. Sel. Top. Quantum Electron.* **26**(2), 1–10 (2020).
33. J. C. C. Mak, Q. Wilmart, S. Olivier, S. Menezo, and J. K. S. Poon, "Silicon nitride-on-silicon bi-layer grating couplers designed by a global optimization method," *Opt. Express* **26**(10), 13656 (2018).
34. Q. Wilmart, D. Fowler, C. Sciancalepore, K. Hassan, S. Plantier, L. Adelmini, S. Garcia, D. Robin-Brosse, S. Malhouitre, and S. Olivier, "A hybrid SOI/SiN photonic platform for high-speed and temperature-insensitive CWDM optical transceivers," *Proc. SPIE* **10537**, 1053709 (2018).