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# Project Ameliz: Patterning Techniques for Copper Electroplated Metallization on Heterojunction Solar Cells

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**Abstract.** For the current PV production about 2000 tons of silver are consumed per year, 10% of the entire world annual silver supply. The PV production is expected to grow significantly in the next decades in order to enable the energy transition to 100% renewables. Annual production volumes in the terawatt range are predicted already for 2030 and this may lead to higher silver price and put more pressure on the industry to replace silver by copper.

Within the Ameliz project several patterning approaches for copper electrodeposition on heterojunction cells are developed: firstly, patterning by printing a metal seed grid with a dielectric layer as plating mask and secondly masking by a monolayer of self-assembling molecules. These molecules consist of a phosphonic acid group and a hydrocarbon chain. They are bonded to the ITO surface and form a monolayer of well-ordered, densely packed hydrophobic chains, which protects the ITO surface against plating solutions. Furthermore, methods for selective formation of a copper seed layer by electrografting and for improved adhesion by ITO reduction are being investigated.

## INTRODUCTION

The PV production is expected to grow to terawatt levels in the next decades to enable energy transition to 100% renewables and to meet the climate goals. Two terawatt annual production are envisaged already for 2030! [1] [2] For today's annual production of around 100 GW more than 2000 metric tons of silver are consumed (assuming 100 mg silver consumption and 5 W per cell and 100 GW annual production) and in 2019 already 10% of the annual silver supply have been consumed for the PV sector [3]. Even considering a strong reduction in silver consumption per cell (to e.g. 50 mg in 2030) the silver demand for PV will be a considerable part of the entire silver supply. Beside silver, the replacement of other rare materials, like indium, will be crucial for PV production on terawatt scale. Aluminum zinc oxide is an alternative to the commonly used ITO and contains only abundant elements.

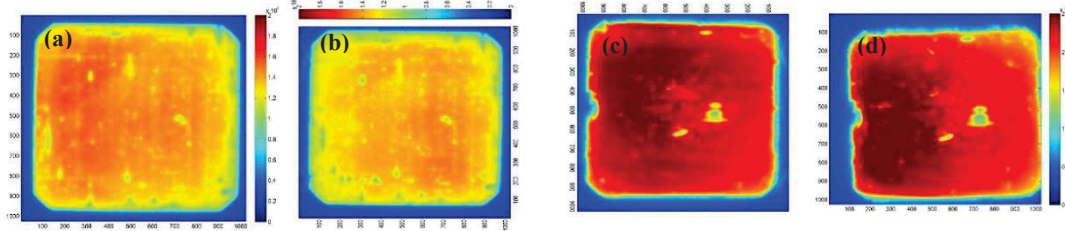
With our baseline copper plating sequence high efficiency above 24.7% has been demonstrated on industrial heterojunction cell precursors and excellent module stability has been confirmed in extended aging tests. The process offers already a cost advantage compared to screen printing, especially for the case of bifacial cells with busbars for interconnection with soldered ribbons, where the silver paste consumption is particularly high [4].

For processes utilizing a thick organic mask, a photoresist or hotmelt ink, the patterning has the highest cost share of the entire process sequence. Therefore, the focus of the Ameliz project is on the development of alternative patterning approaches and furthermore on the replacement of the commonly used PVD seed layer to reduce the upfront investment for cell production with copper electrodeposited metallization.

## COPPER METALLIZATION ON HETEROJUNCTION SOLAR CELLS

The heterojunction structure offers a huge advantage for copper plating: there is no direct contact between the metal and the silicon and thin conductive oxides are excellent barriers against copper diffusion [5] [6]. Therefore, the reliability concerns related to copper ingress into silicon on homojunction cells, where the metals are electrodeposited directly on the emitter [7], do not apply for heterojunction cells.

Heterojunction cell precursors annealed with a pure copper seed layer, sputtered directly on indium tin oxide (over the entire cell surface), do not show any degradation of the photoluminescence signal. This applies equally to precursors on which the TCO has been deposited with a mask and on which on the edges only amorphous silicon layers are present ( Figure 1).



**FIGURE 1.** Photoluminescence images of heterojunction cell precursors with ITO deposited on the n-side on the entire cell surface (on the left) and with mask on the p-side (on the right), before (a) and (c) and after annealing (b) and (d) with sputtered copper seed layer for 1 hour at 190°C.

## BASELINE COPPER PLATING PROCESS SEQUENCE

Our baseline process comprises a sputtered metal seed layer and patterning by hotmelt inkjet printing. After copper plating the hotmelt mask is removed, and the seed layer etched back in between the fingers. Line dimensions of 25  $\mu\text{m}$  width and 25  $\mu\text{m}$  height are reliably feasible with hotmelt inkjet patterning. The specific resistivity of lines deposited from our electrolytes is slightly higher than the resistivity of bulk copper (1.7  $\mu\Omega\cdot\text{cm}$ ) and the measured values vary between 1.8 and 2.6  $\mu\Omega\cdot\text{cm}$ . The used seed layer stack, consisting of a thin adhesion layer and a copper layer for sufficient lateral conductivity, allows for low contact resistivity in the range 0.05 to 0.5  $\text{m}\Omega\cdot\text{cm}^2$  on different TCOs, and for good adhesion. In a 180° peel test performed on cells with soldered ribbons force values above 4 N/mm have been measured. Good efficiency above 24.7% and 83.3% fill factor have been achieved on an industrial precursor, for a monofacial cell with four busbar layout.

Excellent stability of mini-modules made of heterojunction cells featuring copper plated metallization, fabricated according to the baseline process, has been confirmed for interconnection with wires (Smart Wire Connection Technology SWCT) as well as for interconnection with soldered ribbons, exceeding in both cases three times the requirement of the IEC 61215 norm. For the SWCT modules cells fabricated with pure copper seed layer have been used, for the modules with soldered ribbon an additional adhesion layer has been used.

Further details of the process are described in [8]

**TABLE 1.** Cell efficiency certified by ISFH CalTec

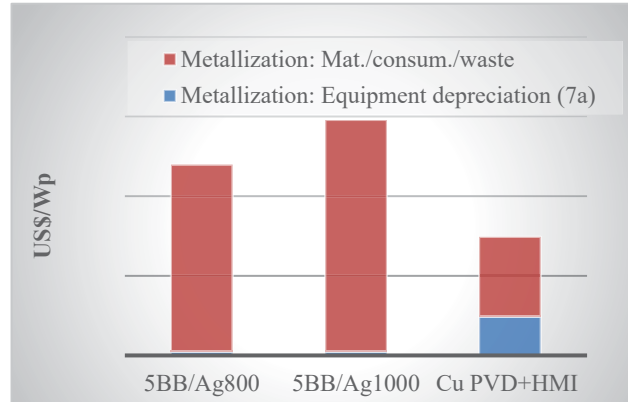
Heterojunction cell	Area [cm <sup>2</sup> ]	Jsc [mA/cm <sup>2</sup> ]	Voc [mV]	FF [%]	Efficiency [%]
4 busbars, monofacial	222.8	40.3	736.1	83.3	24.73

With slight modifications this process is applicable for heterojunction cells with aluminum zinc oxide (AZO), which is sensitive to alkaline and acidic processing solutions. The efficiency of first cells with AZO on both sides and with copper plated metallization is lower than the screen-printed reference, by 0.6 %abs., the main difference

coming from Jsc. There is remaining attack on AZO during processing and a part of the layer is dissolved. Further process improvement, particularly improvement of the seed layer etch-back, is required. [9]

The plating process offers a cost advantage compared to silver screen printing. The silver paste consumption for bifacial heterojunction cells with busbars, for interconnection with soldered ribbons is particularly high, at 300 mg per cell for 5-busbar-layout. With 9 busbars the silver consumption can be reduced to 180 mg per cell.

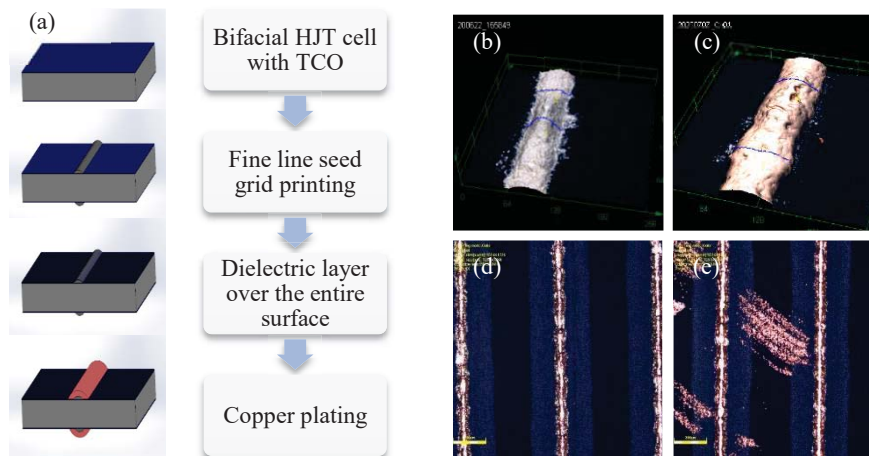
In Figure 2 the difference in metallization cost with silver screen printing and with copper plating is depicted, calculated for cells with 5 busbars, paste laydown 300 mg and for silver paste price 800 and 1000 US\$/kg. It is a simplified calculation: only equipment depreciation and materials and consumables are considered. Facility and labor related costs are not included.



**FIGURE 2.** Cost comparison between silver screen printing and copper plating (with sputtered seed layer and hotmelt inkjet patterning). Calculation for silver paste laydown 300 mg and paste price 800 or 1000 US\$/kg.

## PRINTED SEED GRID AND DIELECTRIC LAYER

Instead of an organic resist a dielectric layer can be used as plating mask, combined with printed seed-grid for patterning [10]. The dielectric layer such as silicon nitride, silicon oxide or aluminum oxide is less than 100 nm thick. The process sequence is visualized in Figure 3. At first a grid of lines and current collecting busbars is printed on both sides of the cell. Either screen printing or inkjet printing of a metal particle paste are applicable. Contrary to standard screen printing for heterojunction cells with busbar-layout the lines are very fine as the required conductivity will be provided by the subsequently electrodeposited copper. In the next step a dielectric layer is deposited over the entire surface. Since the surface of a printed seed line is rough and the dielectric layer not perfectly tight on top of the lines, electrons can pass through and copper can be deposited on top of the printed seed grid.



**FIGURE 3.** (a) Process sequence with printed seed grid and a dielectric layer as plating mask. (b) Screen-printed seed-grid and printed finger covered with electrodeposited copper (c). Cell area with selective copper deposition on the seed-grid (d) and heavy ghost plating on scratched area (e).

The dielectric layer remains on the cell and in the module and serves as double antireflective coating. The thickness of the underlying thin conductive oxide can thus be reduced (lower cost) while preserving good optical properties of the whole stack.

For the first cell tests standard M2 cell precursors with ITO and screen-printed seed-grid with 4-busbar-layout have been used, with standard printing parameters, optimized for cells with busbars and with accordingly high silver paste laydown and wide fingers. A thin aluminum oxide layer (8 nm) has been deposited by ALD as plating mask and good plating selectivity as well as continuous copper deposition on the printed grid have been obtained from an acidic copper electrolyte at moderate current density of 8 A/dm<sup>2</sup>. Because of the wider fingers the J<sub>sc</sub> and the cell efficiency were slightly lower after plating. In the next run a grid with very fine lines will be used and the electrodeposited copper will provide the required line conductivity.

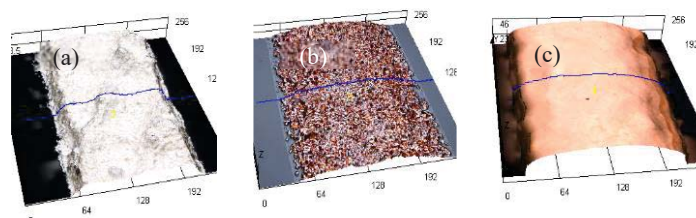
To enable further cost reduction a commercially available copper paste has been tested as seed-grid for plating. The resistivity of the paste is significantly higher than of the silver paste (**Table 2**), but by far sufficient to conduct the small current needed for electrodeposition of copper. Paste optimization will be necessary for printing of very fine lines on textured wafers as well as for contact formation on thin conductive oxides. Contact resistivity of 3.0 and 3.4 mΩ·cm<sup>2</sup> has been measured on IWO and on ITO, respectively. Photoluminescence measurements on heterojunction cell precursors with IWO or ITO with screen-printed copper paste show no impact on cell passivation after annealing at 200°C for 60 minutes. To confirm in extended annealing tests.

**TABLE 2.** Specific line resistivity of low temperature silver paste, copper paste and electrodeposited copper

Paste / electrodeposited Cu	CS-rea [μm <sup>2</sup> ]	Resistance [Ω/cm]	Specific resistivity [μΩ·cm]
Ag paste (curing at 200°C)	2925	0.14	4.0
Cu paste (curing at 200°C)	1880	1.46	27.4
Cu plated on paste	5480*	0.05	2.8
Only plated Cu	3600**	0.05	1.8

\* Entire cross section of the line with Cu plated over Cu paste

\*\* Cross section of the copper paste underneath subtracted



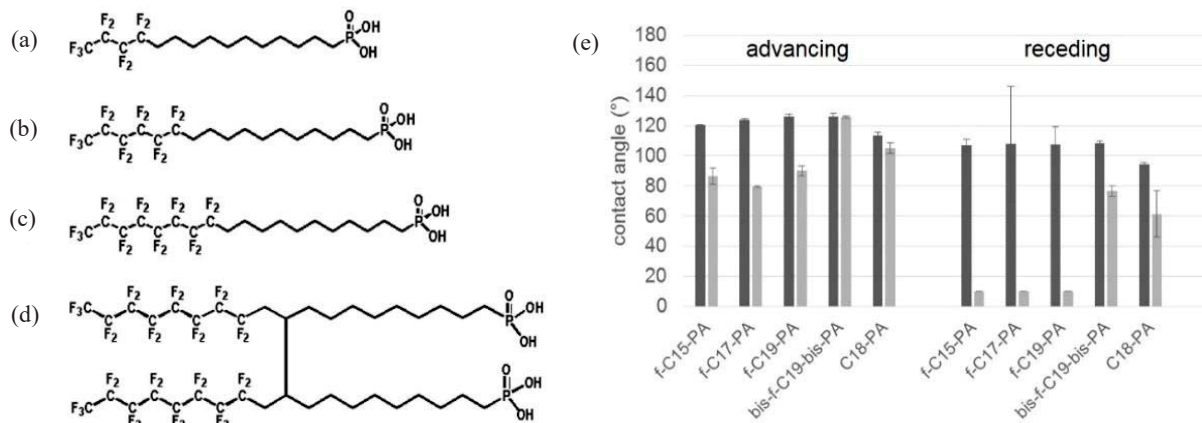
**FIGURE 4.** Lines with screen printed silver paste, screen printed copper paste and copper electrodeposited over copper paste; printed on glass.

## SELF ASSEMBLED MONOLAYER (SAM)

Since SAMs utilize an extremely small amount of material, the monolayer being only ~2nm thick, this approach could achieve plating selectivity with ultra-low costs. Commercially available perfluorinated phosphonic acid as shown in Figure 5 as well as octadecyl phosphonic acid (C18-PA) were applied at first on polished silicon wafers with low roughness ITO [11]. Dynamic contact angles were measured before and after 10 minutes immersion in a highly acidic copper electrolyte. The measurements before and after immersion in the copper electrolyte confirm a lesser attack on the ITO surface when covered by bis-f19-bis-PA and C18-PA molecules. We interpret this as a result of a better packing of the hydrophobic chains in the self-assembled

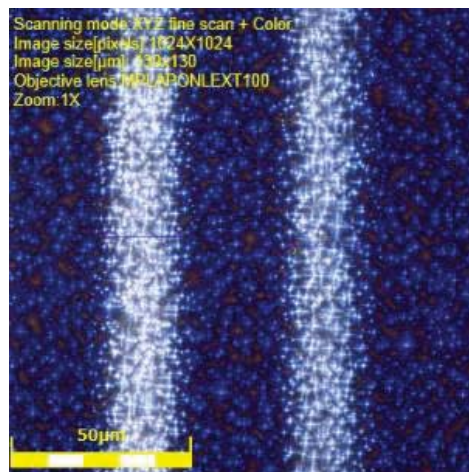


monolayers. While hydrocarbon chains present a linear structure, perfluorinated chains form a helical structure and therefore self-assemble in less compact and more disordered layers. [12]



**FIGURE 5.** Chemical formulas of used perfluorinated phosphonic acids, (a) Nonafluoropentadecylphosphonic acid (fC15-PA), (b) Tridecafluoroseptadecylphosphonic acid (fC17-PA), (c) Heptadecafluorononadecylphosphonic acid (fC19-PA), and (d) Heptadecafluorononylicosanedyl-diphosphonic acid (bis-fC19-bisPA). (e) Dynamic water contact angles of various SAMs on low roughness ITO surface. The contact angles were taken before (dark grey) and after immersion (light grey bars) for 10 min in a highly acidic copper electrolyte.

Octadecyl phosphonic acid (C18-PA) was then applied on textured surface, on a standard M2 HJT cell precursors by spraying and at first patterned with oxygen plasma using a hard mask. Nickel was plated on a cup plater with back side contacting. Lines of 62  $\mu\text{m}$  width have been obtained. However, the plating selectivity was not sufficient, and some ghost plating was present on the SAM covered area. After optimization of spraying parameters and of the patterning 20  $\mu\text{m}$  wide lines and selective plating have been realized (Figure 6).

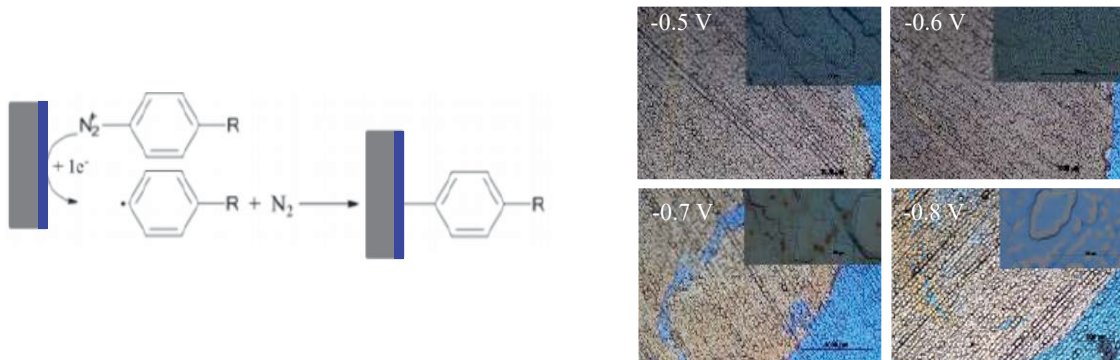


**FIGURE 6.** 20  $\mu\text{m}$  wide lines after Ni plating on a heterojunction cell precursor with SAM mask.

## FORMATION OF A COPPER SEED LAYER BY ELECTROGRAFTING ON ITO

The principle is depicted in Figure 7. Benzodiazonium salts react at the cathode and are covalently bonded to the surface. In case a copper salt is present in the electrolyte, the copper ions are trapped within the electrografted layer and also reduced [13]. For this purpose, a diazonium compound having good complexing properties for copper ions was selected. After optimization of the electrolyte composition and of the deposition potential, homogenous copper-

rich films up to 300 nm thickness have been obtained on polished silicon with ITO. The next goals are application



on bigger cell precursors with textured surface and measurement of contact resistivity.

**FIGURE 7.** (a)Schematic of electrografting and (b) Electrografted copper layers deposited at different potential. Films are more homogenous at -0.5 and -0.6 V than at lower potential.

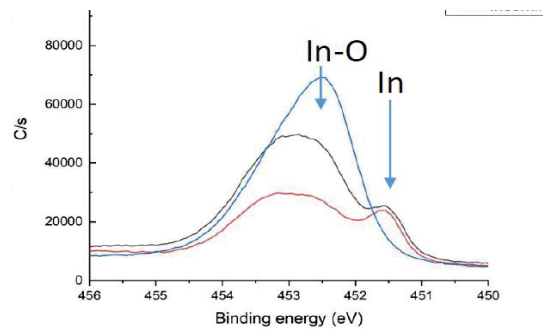
### ITO REDUCTION BY HYDROGEN PLASMA

The adhesion of metal layers electrodeposited directly on thin conductive oxides is not sufficient for metallization of heterojunction cells for standard interconnection with soldered ribbons. Through reduction of the topmost ITO layer to form a thin metallic layer, the adhesion of subsequently electroplated metal is improved.

Good parameters of inductively coupled plasma were found for appropriate ITO reduction. The ITO reduction has been confirmed by lowered sheet resistance and XPS measurements. A smooth indium layer was observed, without spheres as may happen on electrochemically reduced ITO. First tests with nickel layers plated on the reduced ITO indicate good adhesion. Optimization of the plasma parameters is ongoing to fully eliminate the remaining minor impact on cell passivation.

**TABLE 3.** Sheet resistance after H<sub>2</sub>-plasma reduction.

ITO sample	R <sub>sheet</sub> [Ω/square]
As deposited	339
500W ICP-H2	156
700W ICP-H2	81



**FIGURE 8.** XPS measurement on reduced ITO



## SUMMARY

The heterojunction structure offers the unique and specific resistance against copper ingress, confirmed by excellent module stability [14] [15] [16]. However, the implementation of plating in production proceeds slowly. The processes and equipment required for copper plating are new to the solar cell manufacturers and the upfront investment is high. Already existing process options for copper plating offer a cost advantage to silver screen-printing. The strong increase of the silver price in 2020 [17] makes the installation of plating in production more urgent, especially for heterojunction cell manufacturers relying on ribbon interconnection, and necessary even before the PV production will reach terawatt levels.

The results obtained so far within the Ameliz project are encouraging. Partially in an early stage of development, it has been confirmed that the new patterning approaches are principally feasible. A lot of work is required to optimize the process parameters and to optimize the processes towards industrialization but the progress achieved on single process steps may form the base for a copper plating sequence applicable for terawatt PV production in the future.

## ACKNOWLEDGMENT

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