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generate a two-photon entangled pair in an event-ready manner. The QDs can also directly emit two entangled photons via biexciton-exciton cascade decay. Finally, larger Greenberger-Horne-Zeilinger photonic states can be created at distant locations using fusion³³ of two-photon pairs, which will be useful for all-photon quantum repeaters³⁴, distributed quantum sensing⁶, and measurement-based quantum computation³³.

Semiconductor QDs are appealing for near-future applications ranging from high-rate quantum key distribution, long-distance quantum teleportation, multi-photon entanglement distribution across networks³⁵, and intermediate-scale quantum computing³⁶. To this end, further methods need to be developed, such as the control of frequency, time and polarization during the faithful transmissions of single photons over a long distance outside the laboratories. Eventually, no matter what physical system is first proven successful to build practical quantum computers in the future, to link them for a quantum internet, photons will serve as an ideal messenger. □

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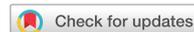
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Competing interests

The authors declare no competing interests.



The path to scalable quantum computing with silicon spin qubits

Silicon spin qubits have demonstrated some promising properties at the individual level, but the technology is beleaguered by a late start and high barriers to entry. To overcome these challenges, the quantum computing and electrical engineering communities will need to find novel ways to work together.

Maud Vinet

In 2021 not a quarter went by without some major announcement in quantum computing making headlines. Whether it is in hardware or software, progress in quantum computing is happening quickly^{1,2}. Research on superconductors, cold atoms, and trapped ion qubits is driving most of these advances. Of the experimental platforms currently on the drawing board, silicon qubits continue to lag behind. The current state of the art stands at a demonstration of just a handful of silicon qubits in a non-scalable configuration^{3,4}.

Yet, silicon qubits hold great promise. Individual silicon qubits have displayed some encouraging properties and collectively they are very well suited to

scale up. Record spin lifetimes have been measured, with coherence times in the millisecond range^{5,6}. High-fidelity single- and two-qubit gates have been reported in a variety of silicon/silicon oxide and silicon/germanium devices, above 99% for both types of gates^{7,8}. And, fast operations, in the microsecond range for all types of gates, have been demonstrated on silicon qubits⁶. Silicon qubits are also naturally well-suited to arrangement in 2D arrays. This is good news for two reasons. First, 2D arrays are compatible with the robust surface code topology needed to implement quantum error correction⁸. Second, 2D arrays can help reduce the number of wires going down to the cryostat through

line-column addressing⁹, reducing at the same time the cryogenic engineering burden. In the same direction, they can operate to 1 K and above¹⁰. Finally — and this is a major advantage — silicon qubits benefit from technology and processes developed to sustain transistor scaling in the semiconductor industry, currently the only industry with proven experience handling billions of semi-identical objects.

Roadblocks for silicon qubits

Quantum computing based on silicon spin qubits is still in its infancy. The first experimental demonstration of a silicon spin qubit only dates back to 2012¹¹; the first complementary metal-oxide-semiconductor

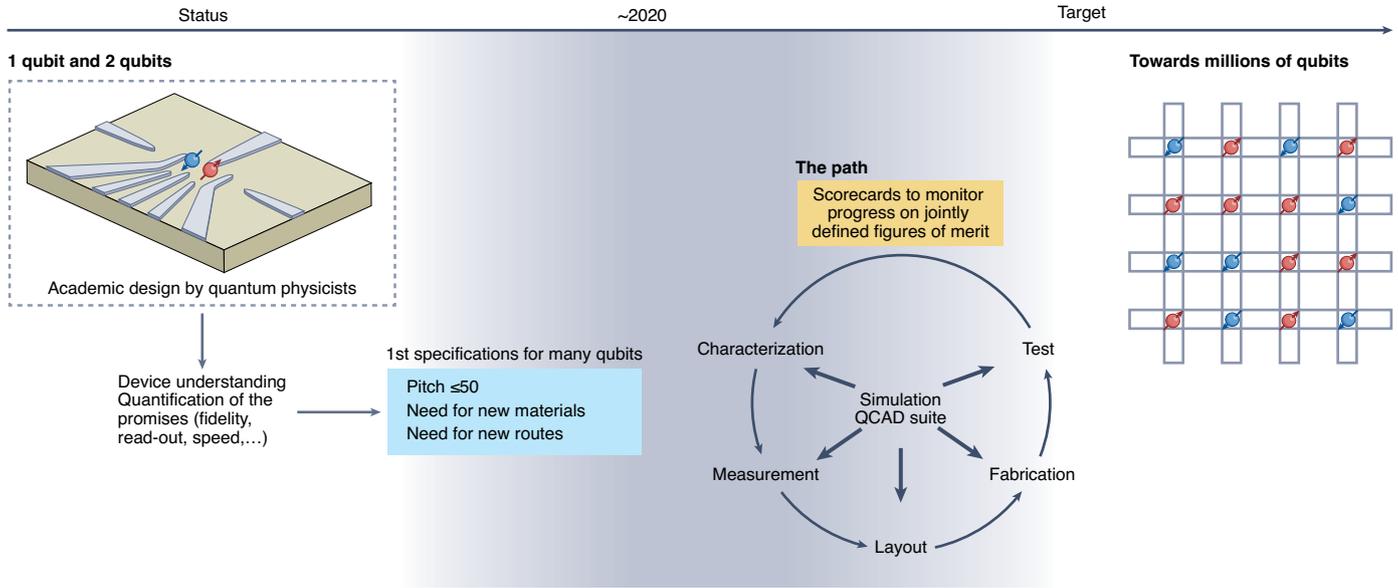


Fig. 1 | How Si qubits could benefit from looking to CMOS to scale up. Silicon spin qubit technology can gain traction from CMOS methodology to reach large numbers of qubits.

(CMOS) device was demonstrated just a few years ago, in 2016¹². Compare that to the first superconductor qubits almost fifteen years earlier¹³. When the concept of a semiconducting qubit was first proposed theoretically in 1998¹⁴, basic research on silicon had already all but ceased. So, the first semiconducting spin qubits were demonstrated in GaAs (ref. ¹⁵), a material particularly appreciated by academic researchers for its high-mobility 2DEG (2D electron gas) and affordable fabrication techniques. But when it appeared that GaAs qubits suffered from a major limitation — a strong hyperfine coupling together with a non-zero nuclear spin that leads to dephasing — a new approach was needed. The search led physicists to Si and SiGe, materials with lower hyperfine coupling. They could even provide a quasi-noiseless environment for electron or hole spins thanks to their nuclear-spin-free isotopes, ²⁸Si and ^{70,72,74}Ge. But they are much more challenging in terms of fabrication, not to mention the supply of isotopically purified materials.

Today, a decade after the first silicon qubit, the community is still debating fundamental questions like the best two-level system for encoding quantum information in a semiconductor. Opinions remain divided between Loss–DiVincenzo, singlet-triplet, hybrid, and charge-based encoding. And then there is the hole versus electron debate. Holes can be manipulated very rapidly using an electric field; electrons require a magnetic field but are reputed to be immune to charge noise and to exhibit long coherence times. Another

question is spin readout. Is it better to improve the techniques traditionally used by physicists¹⁶ or shift to dramatically different paradigms like the multiplexed transimpedance amplifiers introduced by electrical engineers¹⁷? Quantum computing’s small scientific community has been slow to make the decisions needed to move the silicon qubit forward. As there is simply not yet much experimental data to rely on, much of the debate still centres on evidence-based conviction rather than fact-based knowledge.

To scale to many silicon spin qubits means having access to enough qubits fabricated on the most advanced semiconductor-industry equipment. And although silicon qubits leverage advanced CMOS developments, they demand some specific pivots.

From an integration perspective, silicon qubit technology demands an aggressive gate pitch, 50 nm and below; this is below what we are seeing with Intel’s current 10 nm process technology¹⁸. New layout and integration process flows are also needed. Despite the fact that the field is still at an exploratory stage, it is clear that there is no shortcut. Layout developments have to follow the advanced lithography procedure: dedicated design rule manuals are drawn up, layouts are designed, design rule infringement checks are completed, and optical proximity correction is implemented. This is not only costly, but also time consuming.

New materials will also have to be introduced. For the channel, isotopically

purified Si and Si/SiGe stacks will be needed to provide nuclear spin-free active substrates and suppress the spin dephasing associated with hyperfine interaction — this will drastically increase coherence times. However, these materials present supply chain challenges¹⁹ that would hinder their use on a large scale. Specifications for the isotopic purity of the material have yet to be developed, and the best integration scheme to ensure immunity to ²⁹Si diffusion is still an open question.

The requirements for the gate stack are also unforgiving: namely, low or — better — very low charge defects at the channel interface and compatibility of the thermal expansion coefficients across the whole gate stack to avoid local potential peculiarities due to strain²⁰. And, as the dots get smaller or on par with SRAM transistors, device voltage thresholds will depend heavily on metal gate granularity²¹. It’s worth remembering that it takes two to three years to move incrementally from one CMOS generation to the next. For strained silicon transistors with high-*k* dielectrics/metal gate stacks, the journey from lab to production line took eleven years²². The development of silicon qubit technology will be counted in years, as well. Learning cycles are long, and it often takes a year or more between an idea for a device and being able to measure it.

Meanwhile, the semiconductor industry is busy generating revenue from its mainstream business and coming up with its own quantum computing roadmaps, which are mainly hypothetical and long term. In the shorter term, the industry is

banking on technologies that are likely more accessible to semiconductor research and development, like artificial intelligence, in-memory computing, neuromorphic computing, and 3D integration. Intel, with annual revenue of US\$50 billion, has officially spent just US\$50 million over five years on its quantum computing alliance, QuTech. Finally, for process, integration, and electrical engineers, quantum computing is a whole new world, and the fundamental principles and concepts are not exactly intuitive. Still, the market is tantalizing²³. So, it comes as no surprise that there are research and development teams out there trying to develop silicon spin qubits with the goal of fabricating them in the millions and, hopefully, capturing the massive value forecast for universal quantum computing.

Looking to CMOS for inspiration

Silicon-based universal quantum computing is not a physics-only challenge; it is a complex interdisciplinary problem. The quantum computing and electrical engineering communities have started working together through several initiatives²⁴, bridging gaps and cooperating to identify the main challenges and potential solutions.

But this is not enough. To maintain the necessary pace, quantum technology development needs to align even more closely with advanced CMOS strategies and methodologies, as illustrated in Fig. 1. The existing MOS-based information and communication technology know-how, from room temperature down to cryogenic temperatures, and from strong inversion to single- or low-charge transfer, will help bring silicon qubit technology to maturity more rapidly.

The greatest barrier to hardware development is perhaps the lack of a high-throughput electrical characterization infrastructure at the cryogenic temperatures of qubit operation. To go rapidly beyond the scientific 'first' to the technological 'always', statistical data are needed to correlate technological splits and qubit parameters. The first step toward this infrastructure is a high-throughput cryogenic probe station. Next, we will need to establish proxies for qubit performance, determining quality metrics at different fabrication steps just like for transistors. This begins at the substrate level, for instance, with metrics like peak mobility and interface trap density; then, at the quantum-dot level, with the inter-dot tunnelling barrier in the operating regime, charging energy, first electron threshold voltage and respective dispersion, and noise

spectrum. These metrics can be determined using simplified test structures; modules can be designed to specifically address one question. In addition, as fabrication is massively parallel, many designs can be embedded simultaneously: the layouts, the size of the arrays, and the way the qubits are interconnected can be extensively varied inside a chip for evaluation and options comparison. Single-qubit and two-qubit multiplexed arrays can provide a wealth of useful information on the impact of different technological choices on performance; they can also provide early variability data. This new data on materials and integration can in turn feed the 1D and 2D arrays developed in parallel, and the statistical variability will become an input for models and tools for QCAD (quantum computer aided design; a blend of structural modelling, electromagnetic simulation, electronic structure calculations, and descriptions of Coulomb interactions and many-electron states, and qubit operation and dynamics). These QCAD tools will be crucial for early performance assessments of specific layouts and architecture²⁵. Multiscale modelling and simulation can then be used to design devices and architectures, compare alternatives, and assess innovative solutions. This approach will also aid in the interpretation of experiments and the exploration of device physics.

Last, but not least, the same kinds of scorecards that are very successfully used for semiconductor technology (for example, the International Technology Roadmap for Semiconductors (ITRS)/International Roadmap for Devices and Semiconductors (IRDS) roadmap) could be just as effective for quantum computing to measure progress and foster interaction between researchers and engineers in different fields.

The awareness that silicon quantum computing can only be developed by the quantum physics, solid-state physics, electrical engineering, and computer science communities together is very recent. Structuring cooperation will take some effort, but it can be done. The communities will have to determine a set of shared specifications and decide what information is relevant to share with each other and how. The interactions are not quite the same as for CMOS, so some adjustments will have to be made. Trial and error will be part of this process, but once we are on a common path, development will be fast, efficient, and powerful. I also believe that this common path will lead to a quantum computer capable of solving intractable problems. □

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