Vertical Heterojunction Ge0.92 Sn0.08 /Ge GAA nanowire pMOSFETs: Low SS of 67 mV/dec, Small DIBL of 24 mV/V and Highest Gm,ext of 870 μS/μm

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Abstract

We demonstrate high performance vertical heterojunction $Ge_{0.92}Sn_{0.08}$/Ge gate-all-around (GAA) nanowire (NW) pMOSFETs enabled by a top-down approach, a self-limiting digital etching and NiGeSn metallization. Thanks to the GAA NW geometry and EOT scaling, low SS of 67 mV/dec, small DIBL of 24 mV/V, and a high I_{ON}/I_{OFF} ratio of ~10^6 are achieved in the smallest NW device with a diameter down to 25 nm. Furthermore, record high $G_{m,ext}$ of ~870 µS/µm and the best quality factor $Q = G_{m,ext}/SS_{sat}$ of 9.1 are obtained for all reported GeSn-based pFETs.

I. Introduction

Ge(Sn)-based GAA NW MOSFETs have attracted tremendous attention to extend the CMOS roadmap beyond sub-10 nm technology nodes [1-10]. The device architecture utilizes superior properties of Ge(Sn) with high mobilities, high injection velocities etc., meanwhile, it also provides ultimate scalability with strong electrostatics and suppressed short channel effects. Moreover, vertical NW devices can outperform FinFETs and lateral NW devices at the 5 nm node [11]. Recently, vertical GeSn-based GAA NW pFETs have been experimentally achieved with good subthreshold characteristics in spite of large EOT (~ 5 nm) [2]. For performance improvement, EOT scaling should be fully evaluated for vertical Ge(Sn) NW devices.

In this paper, we report vertical heterojunction $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFETs with small NW diameters down to 25 nm and EOT =2 nm, achieving high electrical performance with low SS (Fig. 1), small DIBL, and a high I_{ON}/I_{OFF} ratio. The dependence of key electrical figures of merits (FOMs) on EOT scaling and NW scaling are discussed in detail. The devices also exhibit the highest $G_{m,ext}$ of ~870 µS/µm and a record high quality factor $Q = G_{m,ext}/SS_{sat}$ of 9.1 for GeSn-based pFETs.

II. Material growth and Device Fabrication

The device fabrication starts with high quality material epitaxy of GeSn/Ge/Ge:B stacks grown on 200 mm Si (001) wafers. Boron ion implantation is conducted in the top GeSn layer. Fig. 2 shows the RSM for a 60 nm $Ge_{0.92}Sn_{0.08}$ layer on Ge, indicating a pseudomorphic layer growth with 1.07% compressive strain. The high crystalline quality of GeSn film is proven by the cross-sectional TEM images in Fig. 3. The AFM surface scan (Fig. 4) shows a smooth surface with a small RMS roughness of ~0.85 nm. The low temperature GeSn growth results in an abrupt interface and no intermixing between GeSn and Ge layers as shown in TOF-SIMS depth profiles of Ge, Sn and B atoms (Fig. 5).

The key process steps for device fabrication are shown in Fig. 6. After epitaxial growth, GeSn/Ge NWs are defined by e-beam lithography and top-down patterning with a Cl_2-based etching recipe. Next, digital etching consisting of cyclic self-limiting oxidation and HCl rinse is applied to further shrink the NW diameters. With a radial etching rate of ~0.5 nm per cycle, it is similar to quasi-atomic layer etching to minimize the etching variability. Fig. 7 presents a 25 nm diameter NW with smooth sidewalls. Subsequently, a dielectric combination of $HfO_2/Al_2O_3/GeO_x$ is deposited with post-oxidation process, followed by 40 nm TiN sputtering conformally around the NWs.

Afterwards, spin-on glass (SOG) planarization (cured in N_2 at 350 ºC) is used to position the top gate stack. The top gate stack recess is performed by an optimized isotropic dry etching recipe. A second SOG planarization is then applied as spacer isolation between gate stack and the top contact. The top NiGeSn contact is formed by Ni sputtering and annealing. Next, via openings are used to expose the buried gate and the bottom region. Finally, the device fabrication ends with Ti/Al contact pads by lift-off and post-metallization annealing. Fig. 8 depicts a false-color cross-sectional TEM image of a fabricated vertical GeSn/Ge GAA NW pFET. Note that to avoid Sn segregation in the GeSn layer, all processes are conducted with low thermal budget (< 400 ºC).

III. Results and Discussion

Fig. 9 presents I_D-V_{GS} transfer characteristics of a single vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFET with a smallest diameter of 25 nm. The drain current is normalized with the NW perimeter. Low SS of 67 mV/dec and an I_{ON}/I_{OFF} ratio of ~10^6 at V_{DS} = -0.1V are obtained thanks to superior gate electrostatics. I_D-V_{DS} output curves of the device are plotted in Fig. 10, showing good current saturation. Fig. 11 compares the I_D-V_{GS} curves for 65 nm diameter GeSn/Ge NW devices with various EOT. A significant I_{ON} improvement is obtained by scaling EOT from 5 nm down to 2 nm. As expected, smaller EOT devices exhibit a positive V_{TH} shift. A high drain current I_{ON} of ~245 µA/µm is achieved at V_{GS}-V_{TH} = -0.6V and V_{DS} = -1V in Fig. 12. This device also yields the highest peak $G_{m,ext}$ of ~870 µS/µm at V_{DS} = -0.5V, which is 2.8 times larger compared to $G_{m,ext}$ (~310 µS/µm) for the device with EOT = 5 nm (Fig. 13).

Figs. 14-17 summarize the key electrical FOMs for vertical GeSn/Ge NW pMOSFETs with various NW diameters. Each data point represents the mean value of > 20 devices. Fig. 14 shows DIBL with various NW diameters in the case of EOT = 2 nm. The smallest DIBL of 24 mV/V is achieved and DIBL decreases with NW diameters except for the smallest NW devices. The slight DIBL increase could be attributed to strong surface roughness in the smallest NW devices. As expected, SS decreases with shrinking NW diameter from 65 nm to 25 nm and the devices with smaller EOT have better SS, which is due to stronger electrostatic control (cf. Fig. 15). For the vertical NW architectures, NW diameters play a crucial role in the tradeoff between gate electrostatics and contact resistance. It was confirmed in our previous work [2] that the total resistance R_{tot} was dependent on NW diameters (cf. Fig. 16). In this work, with the improved process and EOT scaling, R_{tot} drops drastically compared to Ge NW pFETs in [2] and remains approximately constant with decreasing diameters. The peak G_{max} for devices with EOT = 2 nm are larger than those with EOT = 5 nm (Fig. 17) and the devices show increasing G_{max} with NW diameters at V_{DS} of -0.5V.

We benchmark the quality factor $Q = G_{m,ext}/SS_{sat}$ at V_{DS}= -0.5V among GeSn-based planar, FinFET, horizontal and vertical NW pFETs (Fig. 18). This work demonstrates the highest $G_{m,ext}$ of ~870 µS/µm and the best Q of 9.1 for all reported GeSn-based pFETs in the literature. This is attributed to the 3D NW geometry, excellent surface passivation and small contact resistance in our NW devices.

IV. Conclusion

Vertical heterojunction $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFETs with smallest NW diameters down to 25 nm are reported. The devices demonstrate low SS of 67 mV/dec, the highest $G_{m,ext}$ of ~870 µS/µm and a record high $G_{m,ext}/SS_{sat}$ of 9.1 for GeSn-based pFETs. The vertical NW platform adopted here is a promising approach for future Ge(Sn) low power logic.

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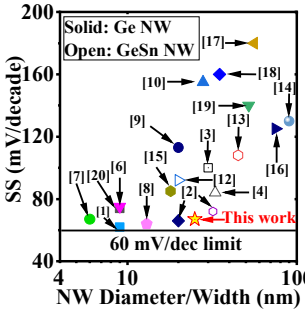


Fig. 1 Benchmark of SS with various NW diameters/widths among the reported Ge(Sn) vertical or lateral GAA NW pMOSFETs. This work demonstrates the low SS of 67 mV/dec for vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pFETs.

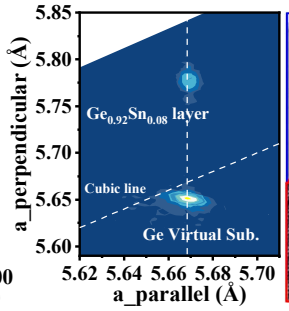


Fig. 2 Reciprocal space mapping (RSM) of a 60 nm thick $Ge_{0.92}Sn_{0.08}$ layer grown on a Ge virtual substrate, showing a pseudomorphic growth and 1.07% compressive strain within the GeSn layer.

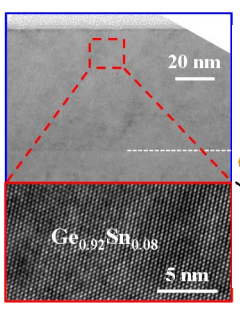


Fig. 3 TEM image (top) of $Ge_{0.92}Sn_{0.08}$ layer on Ge substrate. HRTEM image (bottom) of $Ge_{0.92}Sn_{0.08}$ film with high crystalline quality.

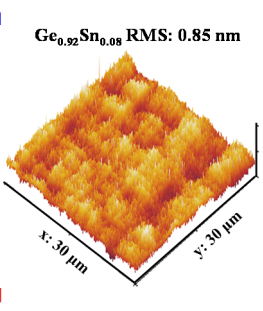


Fig. 4 AFM surface scan image of GeSn layer on Ge showing a smooth surface with a RMS roughness of ~ 0.85 nm.

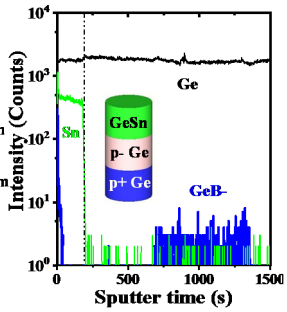
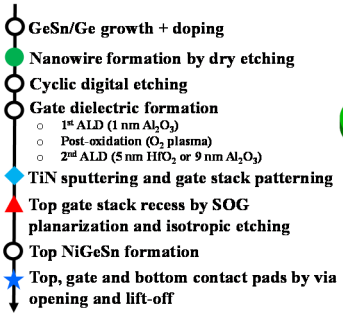


Fig. 5 TOF-SIMS depth profiles of Ge, Sn and B atoms in $Ge_{0.92}Sn_{0.08}$/Ge layers. It depicts an abrupt interface and no apparent intermixing between GeSn and Ge layer due to low temperature growth.



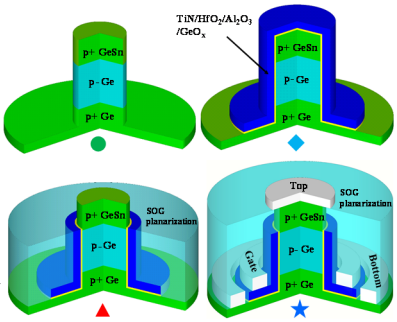


Fig. 6 Key process steps for vertical heterojunction GeSn/Ge GAA NW transistor fabrication. Single GeSn/Ge NW is formed by a top-down approach. Spin-on Glass planarization is applied for interlayer isolation. The processing temperature is kept below 400°C to avoid Sn segregation.

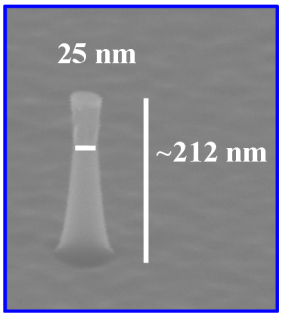


Fig. 7 Tilted SEM image of a vertical GeSn/Ge NW with D = 25 nm by an optimized ICP-RIE recipe and cyclic digital etching, exhibiting smooth sidewalls and a height of ~212 nm.

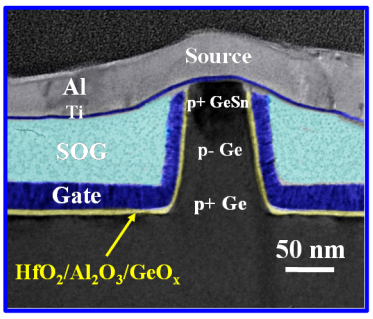


Fig. 8 False-color cross-sectional TEM image of a vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFET with gate stack and contacts.

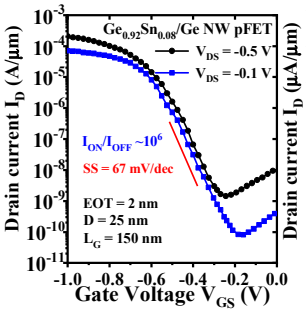


Fig. 9 I_D-V_{GS} transfer curves of a vertical $Ge_{0.92}Sn_{0.08}$/Ge GAA NW pMOSFET with D = 25 nm, L_G = 150 nm and EOT = 2 nm: low SS of 67 mV/dec and an I_{ON}/I_{OFF} ratio of ~10^6 at V_{DS} = -0.1V.

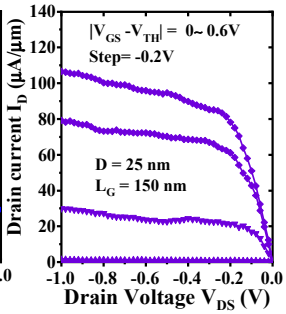


Fig. 10 I_D-V_{DS} output curves of the same device (Fig. 9), showing good current saturation properties.

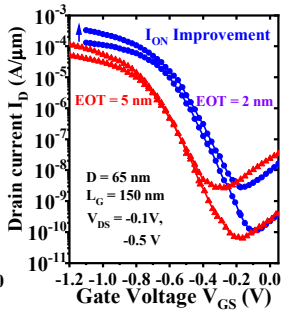


Fig. 11 I_D-V_{GS} curves of 65 nm diameter NW pFETs with EOT of 2 nm and 5 nm, demonstrating a significant I_{ON} improvement with EOT scaling.

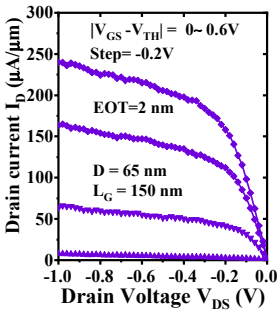


Fig. 12 I_D-V_{DS} output curves of the GeSn/Ge NW device with EOT = 2 nm (Fig. 11) at V_{GS}-V_{TH} = 0 to -0.6V. A high I_{ON} ~245 μA/μm is obtained at V_{GS}-V_{TH} = -0.6V and V_{DS} = -1V.

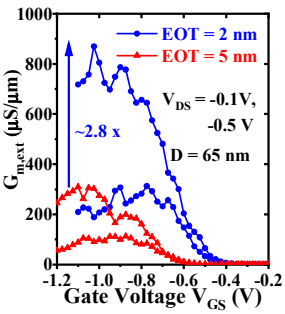


Fig. 13 Extrinsic $G_{m,ext}$ versus V_{GS} at V_{DS} of -0.1V and -0.5 V. The peak $G_{m,ext}$ with EOT = 2 nm, ~870 μS/μm, is 2.8 times larger compared to 310 μS/μm with EOT = 5 nm.

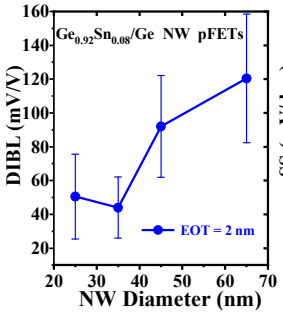


Fig. 14 DIBL versus NW diameter of $Ge_{0.92}Sn_{0.08}$/Ge NW pMOSFETs with EOT = 2 nm.

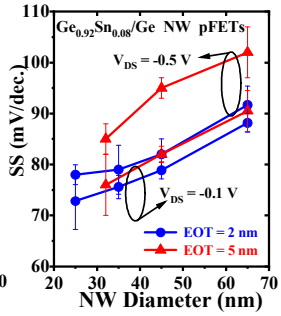


Fig. 15 SS scaling metrics of $Ge_{0.92}Sn_{0.08}$/Ge NW devices with various diameters. SS shows decreasing trends as diameters shrink for devices with various EOT.

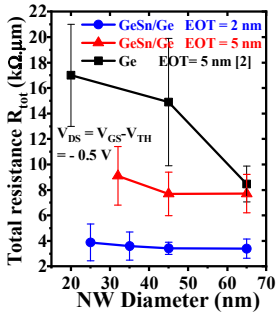


Fig. 16 Dependence of total resistance R_{tot} on NW diameters for GeSn/Ge NW pFETs, showing R_{tot} reduction in comparison to GeSn/Ge pFETs with larger EOT and Ge NW pFETs in [2].

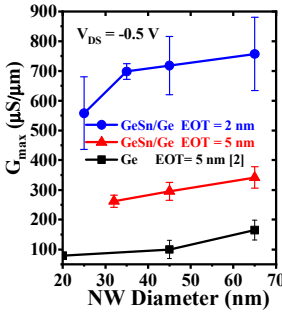


Fig. 17 Peak G_{max} as a function of NW diameters measured at V_{DS}= -0.5V. Larger diameter NW devices show higher G_{max}.

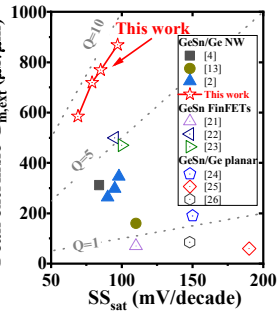


Fig. 18 Benchmark of Q = $G_{m,ext}/SS_{sat}$ at V_{DS}= -0.5V among GeSn-based planar, FinFETs, horizontal and vertical NW pFETs. This work achieves the highest Q for all reported GeSn-based pFETs.