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Experimental Demonstration of Non-Stateful In-Memory Logic with 1T1R OxRAM Valence Change Mechanism Memristors

Henriette Padberg, Amir Regev, Giuseppe Piccolboni, Alessandro Bricalli, Gabriel Molas, *Senior Member, IEEE*, Jean Francois Nodin, and Shahar Kvatinsky, *Senior Member, IEEE*

Abstract—Processing-in-memory (PIM) is attractive to overcome the limitations of modern computing systems. Numerous PIM systems exist, varying by the technologies and logic techniques used. Successful operation of specific logic functions is crucial for effective processing-in-memory. Memristive non-stateful logic techniques are compatible with CMOS logic and can be integrated into a 1T1R memory array, similar to commercial RRAM products. This paper analyzes and demonstrates two non-stateful logic techniques: 1T1R logic and scouting logic. As a first step, the used 1T1R SiO_x valence change mechanism memristors are characterized in reference to their feasibility to perform logic functions. Various logical functions of the two logic techniques are experimentally demonstrated, showing correct functionality in all cases. Following the results, the challenges and limitations of the RRAM characteristics and 1T1R configuration for the application in logical functions are discussed.

Index Terms—1T1R Logic, Non-Stateful Logic, Scouting Logic, Experimental Demonstration, Reliability Issues

I. INTRODUCTION

IN times of reaching the end of Moore's law and dealing with the issue of the memory wall, the search for efficient methods of non-von Neumann computing employs many scientists and engineers [1], [2]. Recently, the research fields of neuromorphic computing and computing in-memory have caught a lot of attention [3], [4], [5], [6]. Computing in-memory implies that logic operations are performed directly in the memory without costly data transfer between the memory and a separate processing unit [7]. Such computing promises energy-efficient computing with the potential to overcome the von Neumann bottleneck. Computing in-memory can be

realized with nonvolatile devices with the resistive random access memory (RRAM) as an outstanding candidate due to its various advantages in power consumption, speed, durability, and compatibility for 3D integration [8], [9]. One promising approach for RRAM-based computing is stateful logic such as MAGIC [10] and IMPLY [11]. In stateful logic, the logical states of inputs and outputs are represented as the resistance states of the memristor devices, with logical '0' as a High Resistance State (HRS) and logical '1' as a Low Resistance State (LRS). However, stateful logic techniques have yet to be demonstrated for large-scale crossbar array implementation. Furthermore, stateful logic is incompatible with CMOS logic and is limited by the device's endurance [12]. Another approach is non-stateful logic, in which different electrical variables represent their inputs and outputs. For example, the inputs are voltages, and the output is the resistance state of the memristor. Non-stateful logic combines the advantages of computing in-memory and CMOS compatibility.

Commercial RRAM products are built in a 1T1R configuration, where every memory cell has a transistor and a memristive device. Wang et al. [13] proposed a functionally-complete Boolean logic based on 1T1R arrays by defining the parameters for the voltages at the gate of the transistor, G , the top electrode, TE , and the bottom electrode, BE , of the memristor as the inputs of the logic gate. Another input is the memristor's initial resistive state, I . The output of the logic gate is read out as the resistive state of the memristor after the logic operation. All four parameters (G , TE , BE , and I) are defined according to the values of the logic gate's inputs, p and q , with four possible combinations. In this brief, the described logic will be referred to as *1T1R logic*.

Another non-stateful logic type suitable for 1T1R arrays is *scouting logic* [14]. Here, the inputs are represented by the resistive states of two memristors, and the output is the measured current during a simultaneous read-out of the inputs. Depending on the selection of a reference current, the logical functions AND, OR, and XOR are performed.

This brief experimentally demonstrates 1T1R as well as scouting logic techniques using SiO_x-based Valence Change Mechanism (VCM) memristors to explore their possibilities for various applications. We show successful operations of both logic types and highlight the critical failure risks, such as the overlap of HRS and LRS state and state-instabilities. Furthermore, the limitations of the 1T1R configuration for other logic techniques are discussed. The results confirm the

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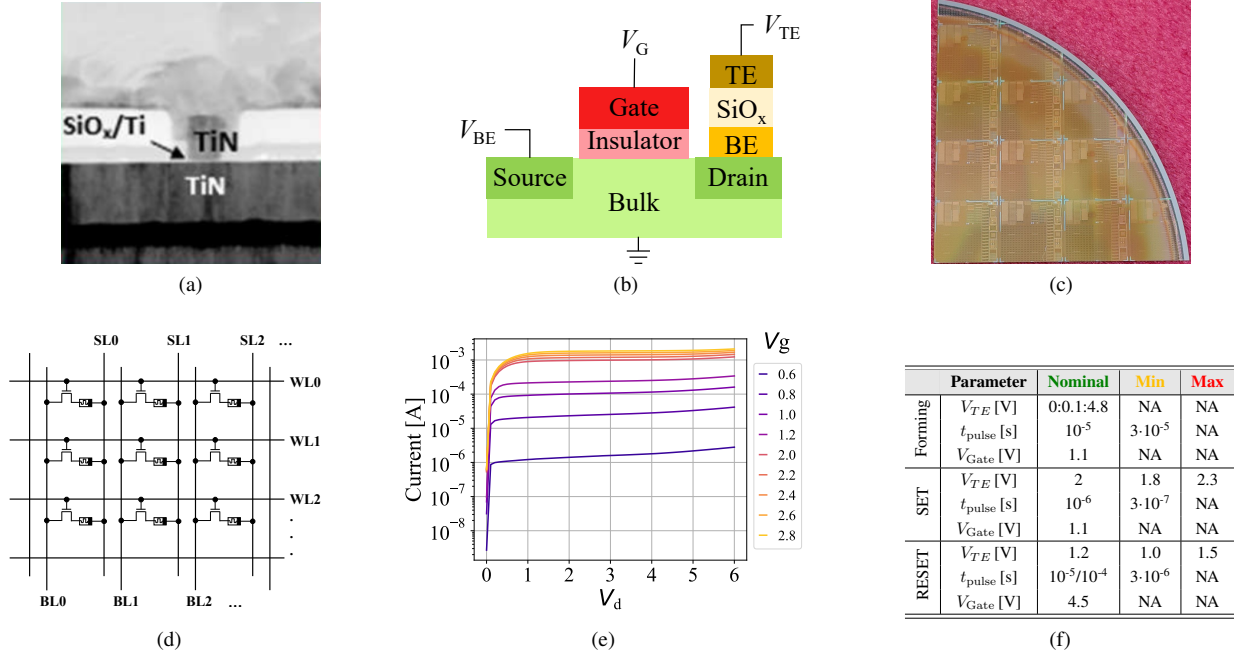


Fig. 1: VCM sample structure and configuration. (a) SEM image of the MIM structure of the Weebit-Nano VCM cells [16]. (b) Scheme of the 1T1R stack. (c) Image of the full sample. (d) Schematic of the 1T1R memory array. (e) The transistor characteristics by current over drain voltages V_d for different gate voltages V_g . (f) Ideal switching parameters of the VCM devices [17].

reliability issues of RRAM devices, especially variability, which is one of the greatest challenges of VCM cells.

II. EXPERIMENTAL MEASUREMENTS

A. Sample

The measurements were performed using the metal-insulator-metal (MIM) structure of VCM cells provided by Weebit-Nano, fabricated at CEA/Leti R&D center in Grenoble France [15]. The devices have the stack composition of TiN as the bottom electrode (BE), SiO_x as the switching material, and Ti as the top electrode (TE). Further device information is shown in Fig. 1. The cell performs a SET process when a positive voltage is applied at the TE with the BE grounded and performs a RESET with a positive voltage at the BE, and the TE is connected to the ground. The switching characteristics of ten different cells are shown in Fig. 2, demonstrating cell-to-cell variability and the cycle-to-cycle variability of HRS and LRS. Nevertheless, the resistances of HRS and LRS do not overlap at any time, with a mean HRS/LRS ratio of 19.4, ensuring a clear distinction between HRS and LRS.

B. Measurement Setup

All tests were performed using a cascade summit12000 probe station, controlled by a Keysight B1500A parameter analyzer.

1) *1T1R Logic*: To realize the combinations of the input parameters for the 16 possible Boolean functions [13], G is connected to the WL, TE is linked to the SL, BE is connected to the BL, and an additional needle grounds the bulk of the

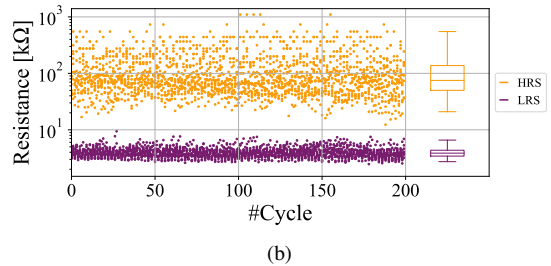
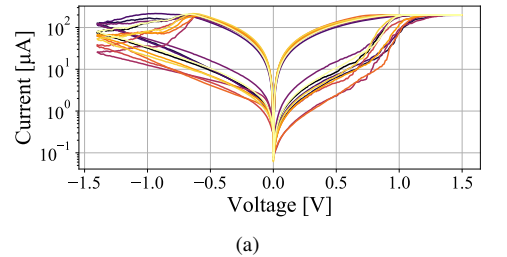


Fig. 2: (a) I-V curves of ten different 1T1R cells. (b) Resistances of HRS and LRS extracted from 100 cycles of 10 cells, 1%-99%-whisker box plot.

transistor. The WL, SL, and BL are defined according to the array structure shown in Fig. 1 (c).

Since there are four input parameters, there are 16 possible input combinations. These configurations are listed in Table I. The column ' TE - BE ' shows if there is a voltage drop over the cell, it is +1 for a positive voltage, -1 for a negative voltage, and 0 for no voltage difference. According to the definition of the cell, a SET is performed for a positive voltage and a

TABLE I: Possible combinations of G , TE , BE , and I .

case	G	TE	BE	I	TE-BE	Process (Possible?)
1)	1	1	1	1	0	/
2)	1	1	1	0	0	/
3)	1	1	0	1	+1	SET (no)
4)	1	1	0	0	+1	SET (yes)
5)	1	0	1	1	-1	RESET (yes)
6)	1	0	1	0	-1	RESET (no)
7)	1	0	0	1	0	/
8)	1	0	0	0	0	/
9)	0	1	1	1	0	/
10)	0	1	1	0	0	/
11)	0	1	0	1	+1	SET (no)
12)	0	1	0	0	+1	SET (no)
13)	0	0	1	1	-1	RESET (no)
14)	0	0	1	0	-1	RESET (no)
15)	0	0	0	1	0	/
16)	0	0	0	0	0	/

RESET for a negative voltage, so the resulting process for $TE-BE=+1$ is a SET and for $TE-BE=-1$ a RESET. If $TE-BE=0$, no process can happen due to the lack of a voltage difference. However, not in all cases of Table I where $TE-BE=+1/-1$ the execution of the given process is possible since the values of G and I have to be considered as well. The transistor is closed if $G=0$ (cases 11-14); therefore, switching is impossible in these cases. Furthermore, if the initial state of the memristor I is 1 and the given process is a SET (case 3), I is already in the LRS so that no switching will occur. This also counts for $I=0$ in combination with a RESET process (case 6). Therefore, all four inputs enable the given switching process only in cases 4 and 5.

Given a truth table with the inputs p and q , each logic function can be realized by setting the parameters G , TE , BE , and I to constants or the inputs p and q [13]. Each combination of G , TE , BE , and I equals one of the cases in Table I, and for each logic function, four cases are possible out of the 16 configurations. For example, if the inputs are $p=q=1$ in the configuration of the NOT p function ($G=0$, $TE=0$, $BE=q$, and $I=\bar{p}$), the resulting input combination equals case 14 of Table I.

Similarly, we tested four logic functions (Table II): OR, AND, NIMP, and XOR. These four functions were chosen because of their importance for different applications. Furthermore, these functions include cases 3-8, 12, 13 and 16, covering all potentially critical cases ($TE-BE \neq 0$) and some uncritical cases with $TE-BE=0$. The cases out of Table I not included by these functions can always be considered non-critical for a correct logical output since there is no possible logical failure without a voltage difference between TE and BE. The cases 11 and 14 do have a voltage difference, however, the transistor is closed and additionally, the voltage polarity is leading to the opposite switching process, so that also these two cases can be considered as non-critical.

2) *Scouting Logic*: In scouting logic, the inputs are represented by the resistive states of two or more memristors, and the output is the current through the memristors while applying a read-voltage [14]. The assignment of the current to logical '1' or '0' is done by defining a reference current. Current higher (lower) than the reference current is defined as '1'

TABLE II: Input Parameters for four logic operations.

	G	TE	BE	I	Out		G	TE	BE	I	Out
OR	1	q	0	p		AND	p	q	0	0	
a) $\rightarrow 8$	1	0	0	0	0	a) $\rightarrow 16$	0	0	0	0	0
b) $\rightarrow 4$	1	1	0	0	1	b) $\rightarrow 12$	0	1	0	0	0
c) $\rightarrow 7$	1	0	0	1	1	c) $\rightarrow 8$	1	0	0	0	0
d) $\rightarrow 3$	1	1	0	1	1	d) $\rightarrow 4$	1	1	0	0	1
NIMP	1	0	p	q		XOR	q	\bar{p}	p	p	
a) $\rightarrow 8$	1	0	0	0	0	a) $\rightarrow 12$	0	1	0	0	0
b) $\rightarrow 7$	1	0	0	1	1	b) $\rightarrow 4$	1	1	0	0	1
c) $\rightarrow 6$	1	0	1	0	0	c) $\rightarrow 13$	0	0	1	1	1
d) $\rightarrow 5$	1	0	1	1	0	d) $\rightarrow 5$	1	0	1	1	0

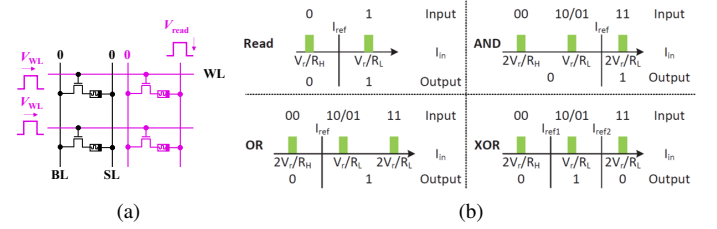


Fig. 3: (a) Array connection to perform scouting logic and (b) selection of reference currents for scouting logic operations [14].

TABLE III: Measurement parameters for both logic types.

variable	SET	RESET	read
V_{TE} [V]	1.3	0	0.1
V_{BE} [V]	0	1.6	0
V_G [V]	1.3	3	3
t_{pulse} [μ s]	1	1	1

('0'). Fig. 3(b) shows the definition of reference currents for Read, AND, OR, and XOR functions. The input combination 10 (cell 1: LRS, cell 2: HRS) is at the same position as 01 (cell 1: HRS, cell 2: LRS) since, in both cases, one memristor is in the HRS, the other in the LRS, and the current should be therefore similar. Two reference currents are needed for the XOR function because the input combinations 00 and 11 have the same output '0'.

For the experimental realization of scouting logic, a read voltage is applied at two parallel connected cells, and the resulting current is measured; V_{read} is applied at one SL and V_{WL} at two WLs to open two transistors, as shown in Fig. 3(a).

Each measurement for both 1T1R and scouting logic is performed with the measurement parameters listed in Table III. The measurement for each logic gate is repeated 100 times to consider cycle-to-cycle variability and was executed in a cascading structure. This was realized by reading out the state of the corresponding memristor after the logic operation and an additional initialization if the cell is not in the logical state that is required for the next cascade.

III. RESULTS AND DISCUSSION

A. Complete Boolean Logic with 1T1R

Fig. 4 shows the results of four logic gates for all four input combinations. The required switching in cases 4 and 5 are observed in all of the logic functions, demonstrating successful

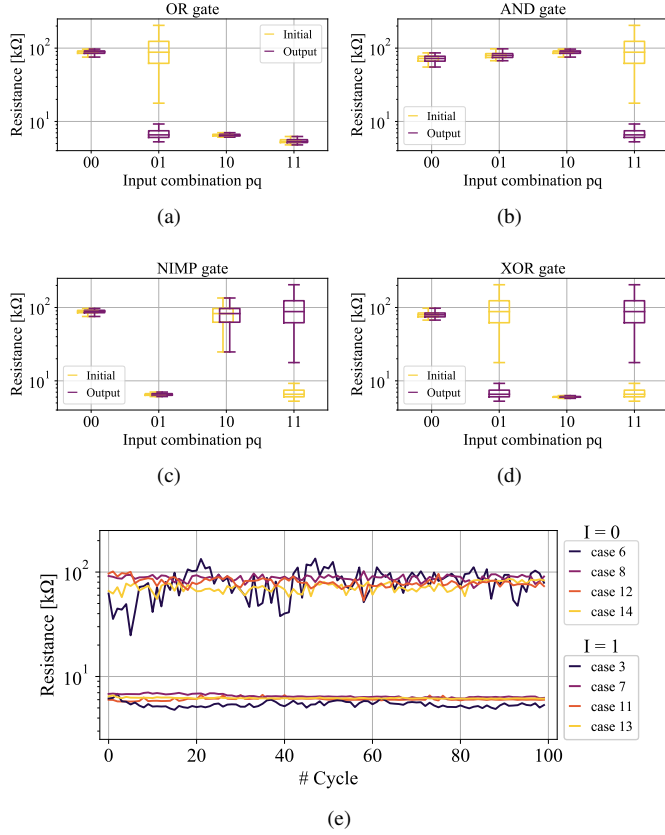


Fig. 4: Experimental results for (a) OR, (b) AND, (c) NIMP, and (d) XOR logic gates. (e) Resistance for all non-switching cases.

switching in each cycle. However, the HRS distribution ranges over an order of magnitude, implying a relatively high cycle-to-cycle variability, as already observed in the previous characterization of the devices (see Fig. 2). The presented results do not overlap the two states, so the correct logical output is ensured. Still, the cycle-to-cycle variability could potentially endanger the correctness of the results for this logic type.

In the cases where no switching is allowed, the initial and output states are identical, as expected. These non-switching cases are shown more precisely in Fig. 4 (e). If the cell is initially in the HRS, the resistance remains high. Similarly, the resistance remains low for an initial LRS. Most cases stay constant at a specific resistance, and only case 6 shows variations that HRS instabilities can explain [18]. Nevertheless, HRS and LRS regions do not overlap. Case 3 shows minor variations as well since the voltage configuration would also allow a switch, but the initial state I is already '1'. Compared to the HRS instabilities, LRS instabilities are negligible. Only these two cases suffer from this issue since, in all other cases, either the transistor is closed, or there is no voltage difference between TE and BE. In summary, these results ensure correct computation with 1T1R configuration.

B. Scouting Logic

The results for the scouting logic are shown in Fig. 5. The gaps between the input combinations make the reference

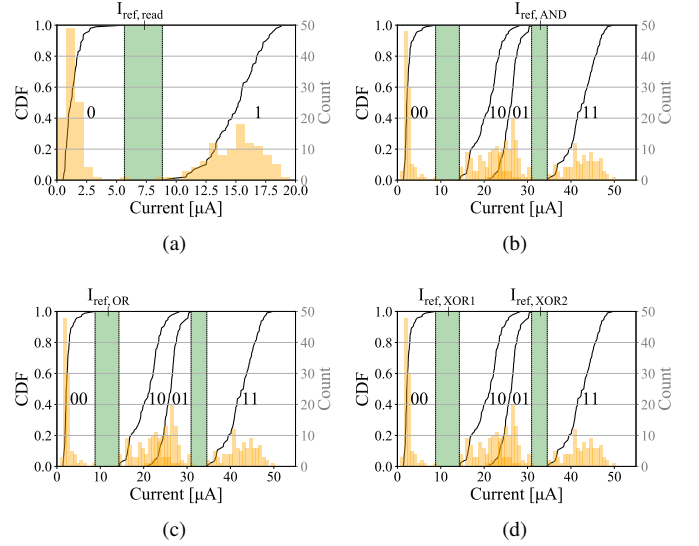


Fig. 5: Experimental results for scouting logic with placing of the corresponding reference current between the four input combinations for (a) read, (b) AND, (c) OR, and (d) XOR operations. A CDF plot shows the distribution of currents of 100 cycles for each input combination.

current's reliable placement possible and ensure a correct operation. Therefore, the values $I_{ref,read} = 7.25 \mu A$, $I_{ref,OR} = I_{ref,XOR1} = 11.55 \mu A$, and $I_{ref,AND} = I_{ref,XOR2} = 32.74 \mu A$ are defined as reference currents for the four functions. For read, AND, and OR, currents higher than the defined reference current correspond to a logical '1', and currents lower than the reference to a logical '0'. For XOR, currents between $I_{ref,XOR1}$ and $I_{ref,XOR2}$ represent the output '1', currents outside of these values are considered as '0'.

The cycle-to-cycle variability observed both in the device characterization and the 1T1R logic is visible in the Gaussian shape of the count distribution of the currents (yellow histogram plots in Fig. 5). If it were even broader, it could result in overlaps of the input states, making a reliable placing of the reference current impossible. Another issue is the cell-to-cell variability, presented in the shift between the black CDF curves of the states 10 and 01 since this shows the different LRS states of different cells. The application of scouting logic can be extended to three or more cells, necessitating a more comprehensive consideration of cell-to-cell variability as the number of cells escalates. This increase can potentially lead to an overlap of input states, thereby increasing the risk of logical failure.

IV. CHALLENGES AND LIMITATIONS

The 1T1R standard configuration is a widely implemented design due to its high selectivity with minimal leakage currents. However, the column-wise SL and BL design faces challenges for serial connection of multiple cells as well as operating different cells in parallel with different voltages. To connect two cells in parallel, both SL and BL have to have the same index, and two additional WL are selected to open the transistors of two cells, as illustrated in Figure 6(a). The

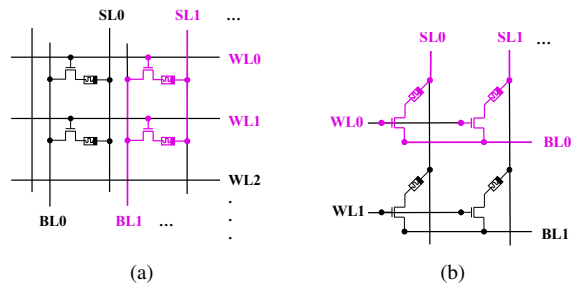


Fig. 6: Connection of two cells in parallel in an (a) 1T1R standard array and a (b) pseudo-crossbar array.

same voltage difference between the top and bottom electrodes is applied to both cells. Since there is no other option for connecting two cells, the application of different voltages at the two cells is impossible. For the demonstrated 1T1R and scouting logic, the given 1T1R configuration fits perfectly; however, this limitation may reduce the potential for other logic in-memory implementations.

A proposed solution for the issue presented is a pseudo-crossbar array, depicted in Fig. 6(b). This design facilitates parallel connection by selecting two SLs, one BL, and one WL enabling the application of different voltages to each cell.

Besides the array architecture, RRAM technology has challenges, especially cycle-to-cycle and cell-to-cell variability. Our results show that the distribution, especially of the HRS, ranges over an order of magnitude. Another challenging issue is the different SET and RESET voltages required for different cells. Finding the exact parameters to ensure a reliable, correct logic operation and minimal power consumption is crucial.

The 1T1R logic technique exhibits notable advantages due to its simplistic design, employing only a single memristor. Scouting logic demonstrates significant potential as it employs a low voltage and no switching during logical operations, promising reduced power consumption and prolonged device lifespan. However, the need to initialize the inputs occasionally, as well as the need to switch the devices in 1T1R logic, is a major limitation of non-stateful logic. Similar techniques to those used in Resch et al. [12] must be used to increase the lifetime of the devices.

V. CONCLUSION

This brief successfully demonstrated computing by SiO_x VCM cells in a 1T1R array. The cells can distinguish between the high resistance state (HRS; logical '0') and the low resistance state (LRS; logical '1'). Two non-stateful logic types, a complete Boolean function with 1T1R array and scouting logic, have been experimentally investigated. All critical cases in the Boolean set with 1T1R array have been successfully operated without logical failures. Furthermore, the scouting logic had sufficient room for placing a reference current to distinguish between '0' and '1' for the logic functions AND, OR, and XOR. The limitations of the 1T1R array are evident in the parallel connection of cells and applying different voltages at each cell. Additionally, reliability issues of VCM devices still need to be investigated.

With further research and development, the opportunities of this technology can be further explored, ultimately leading to greater efficiency in time and energy.

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