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Annika F Wandesleben, Delphine Truffier-boutry, Frédérique Glowacki, Agnès Royer, Maximilian Lederer, et al.. Influences and diffusion effects of lithium contamination during the thermal oxidation process of silicon. *Advanced Engineering Materials*, 2024, 26 (13), pp.2400396. 10.1002/adem.202400396 . cea-04767710

**HAL Id: cea-04767710**

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Submitted on 5 Nov 2024

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# Influences and Diffusion Effects of Lithium Contamination during the Thermal Oxidation Process of Silicon

Annika F. Wandesleben,\* Delphine Truffier-Boutry, Frédérique Glowacki, Agnès Royer,\* Maximilian Lederer, Benjamin Lilienthal-Uhlig,\* and Carla Vogt\*

Due to the increasing number of application fields using lithium compounds in the microelectronics sector, it is necessary to investigate the contamination influence and the effects of lithium on silicon and silicon oxide. To be able to use lithium in a controlled manner in complementary metal–oxide–semiconductor clean room environments, the various diffusion effects during an important process in semiconductor manufacturing, the thermal oxidation of silicon to form silicon oxide, are investigated herein. This includes the diffusion within the wafer, between wafers, and into the furnace environment. For this purpose, wafers are intentionally contaminated, oxidized, and then analyzed with vapor phase decomposition inductively coupled plasma mass spectrometry. The results of this study are correlated with typical contamination levels in state-of-the-art cleanroom facilities to enable classifications of the results for the semiconductor sector. Furthermore, the effect on the growth rate and uniformity of silicon oxide is evaluated by ellipsometry and topography measurements. Finally, electrical measurements of the oxide layer have shown that there is a significant influence on the silicon oxide quality, meaning that lithium can have a detrimental effect on devices.

## 1. Introduction


Contaminations could generally lead to a deterioration in product quality and a yield reduction, so it is important to be able to assess the potential risk of novel contaminants. Potential lithium (Li) contaminations are becoming more relevant due to new nanoelectronic devices. Li compounds are used in the semiconductor field, for example, for the production of photodiodes,<sup>[1]</sup> zero-resistivity electrode materials,<sup>[2]</sup> spatial light modulators,<sup>[3]</sup> optical switches,<sup>[4]</sup> and microbatteries,<sup>[5–8]</sup> in particular also thin-film batteries.<sup>[9,10]</sup> Even for neutron detectors<sup>[11–13]</sup> and photodetectors,<sup>[14,15]</sup> the use of Li-containing material is on the rise. Furthermore, promising applications for magnetic oxide semiconductors may open up in the future.<sup>[16]</sup> Apart from the new applications, the extensive use of glass wafers represents a source of contamination because they could contain Li.<sup>[17]</sup>

The increasing use of Li-containing components bears the risk for a Li contamination of equipment and handling systems and then to cross-contamination of subsequent wafers. The exact distribution and diffusion effects during the processes are not yet sufficiently understood. In state-of-the-art cleanroom facilities, it is common to avoid Li contamination by eliminating potential sources. This means avoiding the use of Li or to separate everything that comes into contact with it. One reason for this is that the detection of Li is not straightforward, as it is not detectable by total reflection X-ray fluorescence.<sup>[18,19]</sup> As the surface analysis has to fulfill a detection limit of  $<1 \times 10^{10}$  at  $\text{cm}^{-2}$  Li, only vapor phase decomposition coupled with inductively coupled plasma mass spectrometry (VPD–ICP–MS) remains as commonly used analysis technique. Many complementary metal–oxide–semiconductor (CMOS) materials have been investigated in previous publications, for example, their solubility and diffusion behavior, their influence on oxide growth, and other properties.<sup>[20–25]</sup> For the conscious use of Li, it is necessary to perform fundamental studies on the influence of this element in a comparable way as for CMOS materials that are already in use. For the assessment of Li as a contaminant, Scott already has shown that Li leads to an increase in the silicon oxide growth rate.<sup>[26]</sup> The study was conducted with relatively highly concentrated contamination solutions up to 10 ppm<sup>[26]</sup> without reporting the resulting contamination values in at  $\text{cm}^{-2}$

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 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/adem.202400396>.

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DOI: 10.1002/adem.202400396

for the wafer surface. In this work, these results are confirmed and the growth rate is correlated with typical contamination levels in state-of-the-art cleanroom facilities to enable classifications of the results for the semiconductor sector. The experiments and analyses performed investigate the various diffusion effects during one important process in semiconductor manufacturing—the thermal oxidation of silicon (Si) to form silicon oxide (SiO<sub>2</sub>). For this purpose, wafers were intentionally contaminated with Li by spin coating at different contamination levels:  $1 \times 10^{11}$  at cm<sup>-2</sup> (level 1),  $1 \times 10^{12}$  at cm<sup>-2</sup> (level 2), and  $1 \times 10^{13}$  at cm<sup>-2</sup> (level 3). These values correspond to Li contamination in the ppb ( $\mu\text{g kg}^{-1}$ ) range. Then the reference wafers, contaminated wafers, and filler wafers were oxidized and the diffusion within the wafer, between wafers, and into the furnace environment was analyzed by VPD–ICP–MS and liquid phase decomposition bulk ICP–MS (LPD bulk ICP–MS). VPD–ICP–MS is used to determine Li contamination on the surface of wafers up to the method detection limit of  $1 \times 10^8$  at cm<sup>-2</sup>, while LPD bulk ICP–MS can be used to detect Li contamination in the first two  $\mu\text{m}$  of the silicon bulk of wafers up to the method detection limit of  $3.1 \times 10^9$  at cm<sup>-2</sup>. Due to the use of Li and the so far unpredictable cross-contamination risk, the wafers were oxidized in a furnace dedicated to Li. As a further safety measure, the Li-contaminated wafers were processed in a closed cage instead of the usual open boat to minimize the contamination of the furnace. The effect on the growth rate and the uniformity of the SiO<sub>2</sub> were evaluated by ellipsometry and atomic force microscopy (AFM) measurements to analyze the topography. In addition, electrical measurements of the oxide layer were executed to determine the influence on the oxide quality. For all measurements in this study, the number of repetitions performed is indicated by *n*.

## 2. Results and Discussion

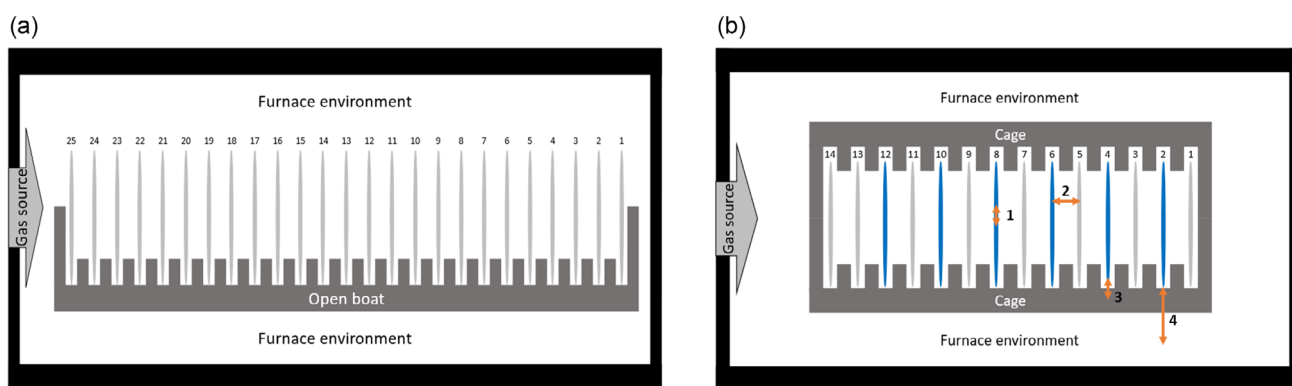
During the usual oxidation process in the open boat, the wafers are surrounded by the furnace environment; this is illustrated by the left schematic in **Figure 1**. The right schematic shows the shielding of the wafers to the furnace environment due to the closed cage, used for the experiments, and the possible diffusion paths (marked in orange) based on the contaminated wafers (marked in blue).

and thus the oxidation of the wafers; nevertheless, the wafers are more shielded than in the usual open boat.

To investigate cross-contamination effects during runs with contaminated wafers, the intentionally contaminated wafers were separated from each other with filler wafers. Through the analysis of those wafers by VPD–ICP–MS, diffusion to neighboring wafers and thus diffusion over short distance can be studied. The possible diffusion paths are within the wafers 1), between wafers 2), and over longer distances into the cage 3) or the furnace environment 4).

To observe the diffusion of Li during the oxidation process, the Li concentration before and after the oxidation was determined. VPD–ICP–MS was used to analyze the Li concentration on the surface of the wafers and LPD bulk ICP–MS measurements were used to analyze the Li concentration in the first two  $\mu\text{m}$  of the Si bulk of the wafers. First, a measurement of bare Si wafers was conducted to ensure that no base contamination was detectable. Then, to measure the influence on the furnace as well as the cage, two types of oxidized reference wafers were used in this study. For a reference of the furnace, bare Si wafers were processed in the open boat of the furnace. This boat is used to process wafers without Li, but in the past, it was used to process wafers with deposited Li-containing layers. Therefore, the Li contamination level was observed. For the second reference type, the oxidation was performed in the closed cage used for the oxidation of Li-contaminated wafers. Hence, the second reference provides the cage contamination level. Two wafers per reference were analyzed and the mean values are summarized in **Table 1**. In case of nonmeasurable values, the method detection limit (MDL) is indicated instead.

Table 1 shows that neither the wafer reference has Li contamination on the surface, nor in the first two  $\mu\text{m}$  of the bulk, as expected for bare Si wafers. The furnace reference, being the contamination level of the furnace at the beginning of the experiments, was measured in the furnace open boat. The reference Li level of the closed cage was measured before starting runs with contaminated wafers. This closed cage reference level was slightly higher than the furnace level. No Li was analyzed by LPD bulk ICP–MS in the first two  $\mu\text{m}$  of the bulk. Thus, the furnace and the closed cage were already contaminated before starting the experiment which contributes to the mentioned baseline levels of Li. The cause is that the furnace was used in the past to process wafers with Li containing layers and based



**Figure 1.** Schematic illustration of the furnace process with a) open boat and b) closed cage; blue = contaminated wafers and orange = diffusion paths.

**Table 1.** VPD–ICP–MS and LPD bulk ICP–MS values of the references,  $n = 2$ .

	Wafer reference	Furnace reference	Cage reference
VPD surface	MDL	$9.50 \times 10^9$ at $\text{cm}^{-2}$	$1.65 \times 10^{10}$ at $\text{cm}^{-2}$
LPD bulk	MDL	MDL	MDL

on the results it could be verified that the furnace has a nonreversible Li contamination level.

For the evaluation of the diffusion behavior of Li during the oxidation process, the actual Li contaminations of the intentionally contaminated wafers were determined before the furnace process. These values have confirmed that the intentional contamination worked as planned. The results are at the contamination levels of  $1 \times 10^{11}$ ,  $1 \times 10^{12}$ , and  $1 \times 10^{13}$  at  $\text{cm}^{-2}$  as expected. No Li was detected by LPD bulk in the first two  $\mu\text{m}$  of the intentionally contaminated wafers. However, it cannot be excluded that Li contaminations lower than the detection limit of  $3.1 \times 10^9$  at  $\text{cm}^{-1}$  are present in the bulk. As the concentrations on the surface are consistent with the hypotheses made in advance, it is nevertheless assumed that Li was only applied superficially as planned and did not diffuse into the bulk at room temperature.

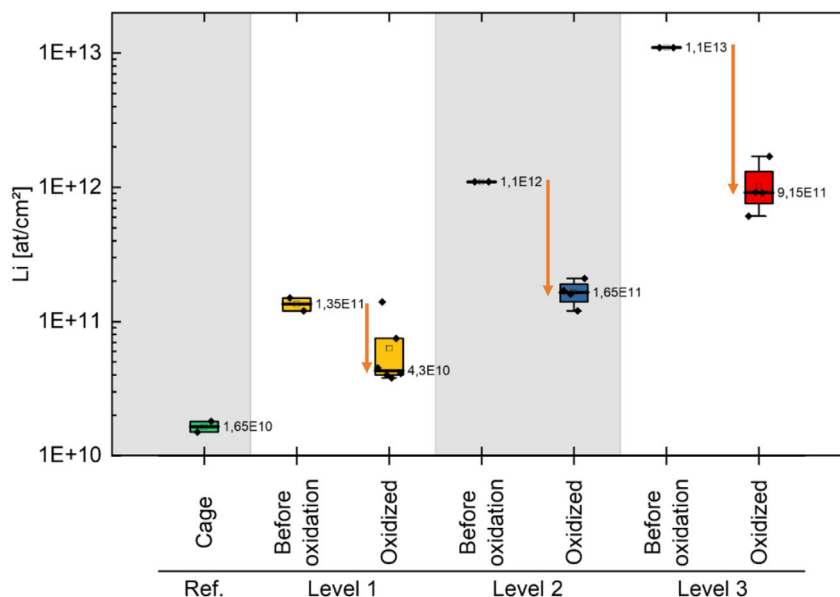
The effect of the furnace oxidation process on the Li distribution is shown by the comparison of the VPD–ICP–MS surface results before and after oxidation (Figure 2). In general, the Li concentration is significantly higher for the wafers before oxidation than for the oxidized wafers. Thereby, the higher the initial concentration, the higher the Li decreases for the oxidized wafers. This can be identified by the increasing difference of the median values, marked with vertical arrows in Figure 2. During the oxidation process, the contamination

decreases of about half a decade for level 1, of about one decade for level 2, and over one decade for level 3.

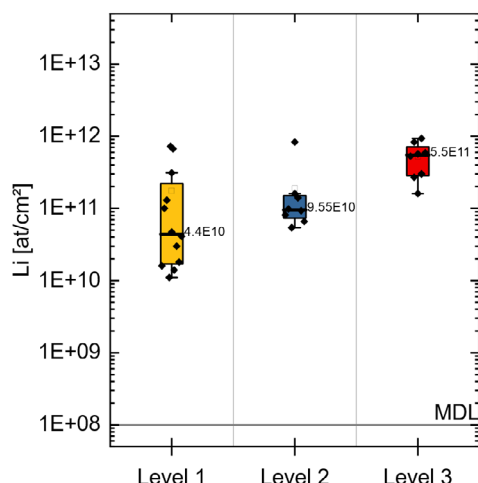
The reduction of the Li concentration, determined by VPD–ICP–MS, could be explained by three different diffusion processes. One way of explanation is that the Li has diffused within the Si wafer and hence a part of the Li is located in the bulk instead of on the surface. In Figure 1 (right schematic), this path is marked with number 1. To examine this hypothesis, LPD bulk measurements were performed to investigate the possible diffusion of Li into the first two  $\mu\text{m}$  of the Si bulk. In all these measurements, Li values were below the method detection limit of  $3.9 \times 10^9$  at  $\text{cm}^{-1}$ . However, this result does not exclude the possibility that Li diffuses through the wafer. It is known that Li diffuses very quickly,<sup>[27,28]</sup> at  $950^\circ\text{C}$  Li has a diffusivity  $>1 \times 10^{-6} \text{ cm}^2 \text{ sec}^{-1}$ <sup>[28,29]</sup> and thus diffuses faster than copper, which is known as a fast diffusing material in the semiconductor sector.<sup>[28]</sup> Therefore, Li could distribute rather quickly within the wafer and could possibly no longer be detected in the first two  $\mu\text{m}$ .

The second possibility is the diffusion over short distances from the contaminated wafers via the gas phase to the nearest wafers in the closed cage. In Figure 1 (right schematic), this path is marked with number 2. The Li values of the filler wafers (between the intentionally contaminated wafers) after the oxidation process are shown in Figure 3.

The graph clarifies that all filler wafers, which were not intentionally contaminated with Li before oxidation, are contaminated after the oxidation process. This result shows that a diffusion phenomenon occurs from one wafer to another via the gas phase. The higher the original Li concentration on intentionally contaminated wafers was, the higher Li concentration on the filler wafers was measured. It is noticeable that for all three levels, the measured values can be up to around  $1 \times 10^{12}$  at  $\text{cm}^{-2}$  as maximum and that just the median value of the Li contamination increases



**Figure 2.** VPD–ICP–MS values for Li contamination of cage reference ( $n = 2$ ) and contaminated wafers before oxidation ( $n = 2$ ) and after oxidation (level 1  $n = 6$ , level 2  $n = 4$  and level 3  $n = 4$ ).

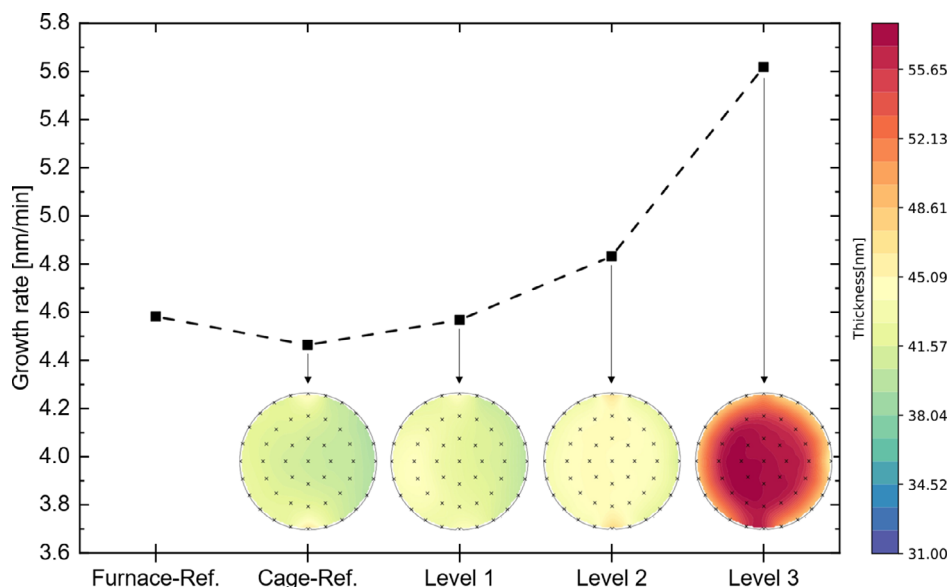


**Figure 3.** VPD-ICP-MS values for Li contamination of the filler wafers after oxidation near intentionally contaminated wafers of level 1 ( $n = 12$ ), level 2 ( $n = 8$ ), and level 3 ( $n = 8$ ).

steadily. The three median values show an almost linear progression. An explanation for the increasing values and the maximum value at the same time could be the continuous gas flow in the furnace. It can be assumed that the continuous gas flow only

**Table 2.** Silicon oxide thickness for the references and the different contamination levels of li.

	Furnace reference	Cage reference	Level 1	Level 2	Level 3
Average	$41.2 \pm 1.4$	$40.2 \pm 1.2$	$41.1 \pm 1.3$	$43.5 \pm 1.3$	$50.6 \pm 2.1$
SiO <sub>2</sub> [nm]					



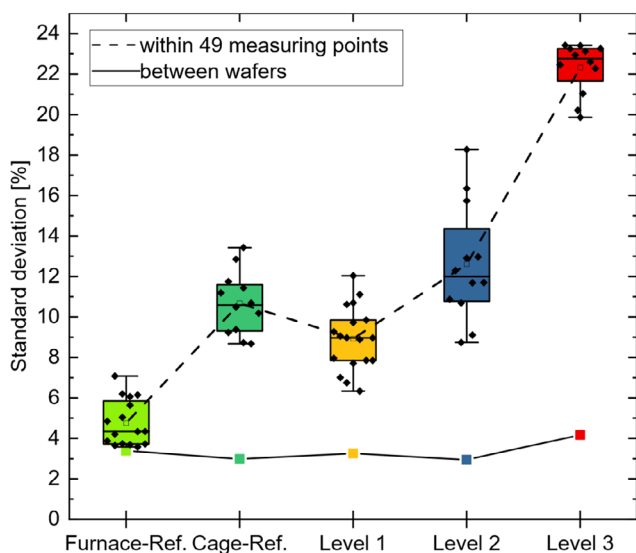
**Figure 4.** Growth rate of silicon oxide on the wafers for the references and the different contamination levels of Li and wafer maps from slot position 8 in the cage.

enables a limited transmission of Li, although the incidence of this maximum transfer increases with increasing contamination. Based on the results, it can be concluded that the Li diffuses from the contaminated wafers to the nearest ones in the closed cage during the oxidation process.

The third possibility of cross-contamination is a long-distance diffusion into the hardware of the tool and into the closed cage. The two options of long-distance diffusion are marked in Figure 1 (right schematic) with numbers 3 and 4. A contamination control of the furnace was realized after the runs and the measured Li concentration was about  $3 \times 10^{11}$  at  $\text{cm}^{-2}$  in comparison with the initial value of about  $9.5 \times 10^9$  at  $\text{cm}^{-2}$ . This result shows that Li diffuses into the furnace environment and leads to contamination of the tool. This probably occurs less through the wall of the closed cage than through the holes in the closed cage, through which the gas flow in the cage is enabled. We have also seen that processing uncontaminated wafers allows to reduce the furnace contamination level to about  $1 \times 10^{10}$  at  $\text{cm}^{-2}$ , but not lower.

In addition to the diffusion of the Li, the influence of Li on the oxide growth and the SiO<sub>2</sub> characteristics can be observed by the experiments. For the analysis of the oxide growth and the uniformity of the silicon oxide, 49-point measurements were conducted by ellipsometry after oxidation to determine the silicon oxide thickness of all wafers. The following number of wafer samples were analyzed: furnace reference  $n = 16$ , cage reference  $n = 12$ , level 1  $n = 18$ , level 2  $n = 12$ , and level 3  $n = 12$  and are evaluated in Table 2, Figure 4 and 5. The resulting mean values of the silicon oxide thickness are summarized in Table 2.

The results of Table 2 show no measurable difference of the silicon oxide layer thickness on the wafers between the references and level 1 due to the standard deviation; this can be attributed to the similar level of contamination. Based on the contamination for level 2 and especially for contamination level 3, there is a clear increase of the silicon oxide thickness with



**Figure 5.** Relative standard deviations of the resulting silicon oxide thicknesses for the different contamination levels of Li, between the wafers plotted as squares and within the 49 measuring points of each wafer plotted as boxplot.

increasing Li concentration. Consequently, the silicon oxide thicknesses after processing depend on the initial Li contamination level. To illustrate these results and to include the influence of the Li on the uniformity of the formed oxide, Figure 4 shows the resulting growth rate of silicon oxide on the wafers for the references and the different contamination levels of Li and one wafer map for the cage reference and per contamination level. All wafer maps are from the slot position 8 in the cage.

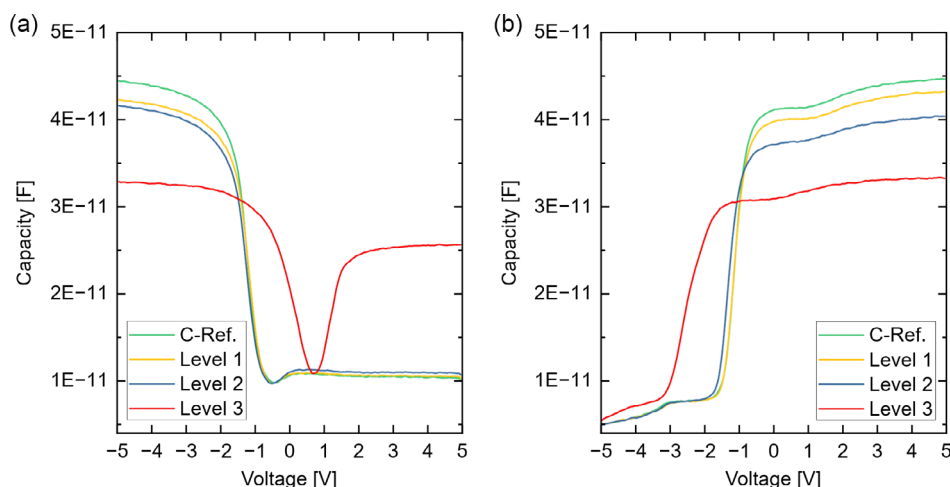
The growth rate shows a significantly increasing curve with a difference of  $1.15 \text{ nm min}^{-1}$  between the cage reference wafers and the level 3 of the intentionally contaminated wafers. Therefore, it can be said that Li impurities have a strong impact on oxide growth. Consequently, particular care must be taken in front-end-of-line processes, e.g., gate oxidation of transistors. An explanation for the increased growth may be an expansion of volume due to the insertion of Li<sup>[30]</sup> and a formation of Li-silicates (e.g.,  $\text{Li}_2\text{Si}_2\text{O}_5$  and  $\text{Li}_4\text{SiO}_4$ ) and  $\text{Li}_2\text{O}$ .<sup>[31,32]</sup> The wafer maps indicate a uniform growth of the silicon oxide. To be able to give an exact statement on the uniformity of the silicon oxide, it is necessary to consider the standard deviations of the ellipsometry measurements. In Figure 5, the relative standard deviations between the wafers and within the measuring points of each wafer are plotted. The relative standard deviation between the wafers remains constant at low values, independent on the contamination level. This means that the average oxide thickness of the different wafers varies only minimally within and between batches. In contrast to this, the relative standard deviation of the 49 measurement points per wafer increases with a similar curve progression as the growth rate from Figure 4 with high values, especially for contamination level 3. Thus, the layer thickness within a wafer varies from measuring point to measuring point and therefore there is an effect on the uniformity within the wafer. One reason for this could be that the Li application by

spin-coating did not lead to an exact equal distribution on the surface, even if the same amount was applied in total.

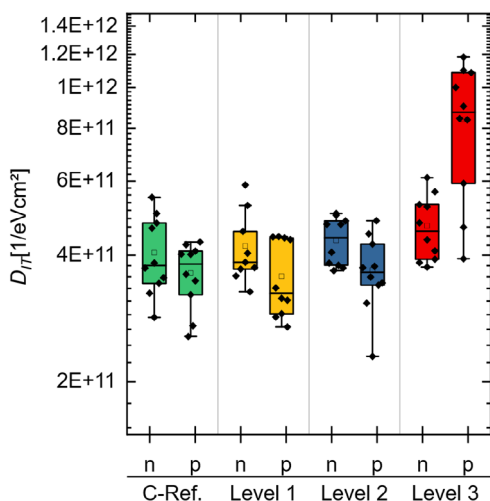
To assess the effect of these standard deviations on the actual topography of the wafers, the roughness of the wafers was analyzed with AFM. These measurements showed that the roughness is only in the range of the measurement variation of the tool, which is around  $0.22 \text{ nm}$ . It can be concluded that there is no considerable influence of Li on the roughness at concentrations up to  $1 \times 10^{13} \text{ at cm}^{-2}$ . This confirms the impression based on the wafer maps that the oxide growth is uniform despite the high relative standard deviations.

To evaluate the silicon oxide quality, electrical measurements were conducted. It was determined that the dielectric constant for the n-doped wafers had a value around  $4.00 \pm 0.05 \text{ F m}^{-1}$  across the various levels. For the p-doped wafers, the dielectric constant values were  $3.95 \pm 0.05 \text{ F m}^{-1}$  for reference, level 1, and level 2 and  $4.05 \text{ F m}^{-1}$  for level 3. Even the value of contamination level 3 does not represent a significant deviation. Thus, there is no significant difference and the results fit with the literature values of thermal silicon oxide.<sup>[33]</sup> For further consideration regarding changes in the characteristics of the oxide, the capacitance–voltage ( $C/V$ ) curves were consulted. For this purpose, Figure 6 shows the  $C/V$  curves at  $1 \text{ kHz}$  for p-doped (plot a) and n-doped wafers (plot b). In general, the capacity decreases; this can be attributed to the increase of the oxide layer thickness, but it is also an indication of a deterioration in the silicon oxide quality. For the p-doped wafers with contamination level 3, a strong inversion of the curve can be seen, which can be attributed to mobile negative charge carriers, i.e., electrons. At contamination level 3, there is also a shift of the flat band, which indicates that fixed negative charge carriers have been inserted.<sup>[34]</sup> Interstitial doping of the oxide layer with Li could therefore have taken place.<sup>[30,35,36]</sup>

For the evaluation of the silicon oxide quality, the interface trap density ( $D_{IT}$ ) is calculated. Based on the observed peak in the conductance–voltage ( $G/V$ ) curve, it is possible to extract  $D_{IT}$ -values.<sup>[37,38]</sup> The results are shown for the frequency  $1 \text{ kHz}$  in Figure 7. The values are not significantly different from each other, only for p-doped wafers with level 3 contamination an increase of the value was noticeable. Therefore, it can also be concluded that the effect on p-MOS is stronger than on n-MOS. This fits with the considerable change already observed in the  $C/V$  curve. However, for the evaluation of the other values, the basic contamination of the furnace and of the cage must be considered. As we already have a high base contamination, the reference and low levels cannot be differentiated and conclusions cannot be drawn, as the discrepancies are not sufficient. In general, lower  $D_{IT}$ -values indicate an improvement in the quality of the oxide. For a high-quality thermal oxide, the  $D_{IT}$ -value should be less than  $1 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ ; a value around  $1 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$  would be ideal. Thus, all values, including the reference, do not fulfil the desired quality. Based on these results, it can be assumed that the existing base contamination of the furnace and the cage already prevent high-quality oxidation; this effect is even stronger at contamination level 3. It can therefore be concluded that a Li contamination above  $1 \times 10^{13} \text{ at cm}^{-2}$  leads to a deterioration in silicon oxide quality, presumably due to interstitial doping with Li.



**Figure 6.** C/V Curves for the cage reference and the different contamination levels of Li at 1 kHz a) p-doped  $n = 10$  and b) n-doped  $n = 9-10$ ; dot area  $0.0005 \text{ cm}^2$ .



**Figure 7.**  $D_{IT}$ -values for the cage reference and the different contamination levels of Li at 1 kHz; dot area  $0.0005 \text{ cm}^2$ ;  $n = 9-10$ .

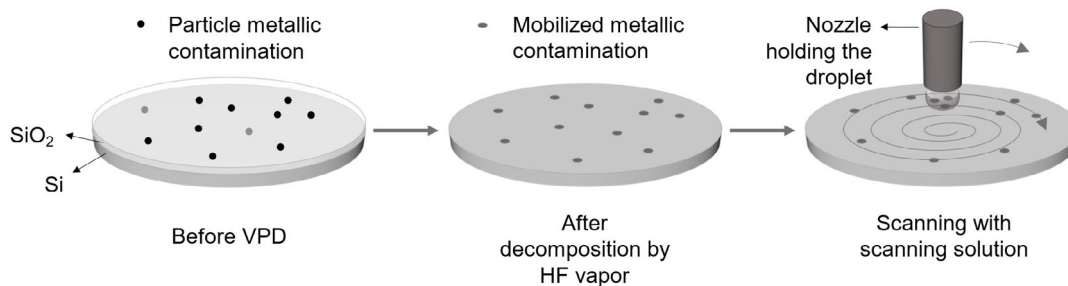
### 3. Conclusion

We have determined that Li diffuses during the thermal oxidation of silicon in a furnace. Accordingly, the Li amount on the surface of the contaminated wafers decreases significantly. For the reduction of the Li concentrations determined by VPD-ICP-MS, three different possibilities of diffusion exist. The first, diffusion within the wafer, could not be validated experimentally. However, this may be a result of the quick diffusion and distribution of Li within the wafer, which is then no longer detectable in the first two  $\mu\text{m}$ . The second possibility, Li diffusion over a short distance between the wafers via the gas phase could be proven, as there is a clear Li diffusion between wafers processed in the same batch. The third possibility, a Li diffusion over a long distance could also be demonstrated, as the furnace is also contaminated by processing intentionally Li-contaminated wafer.

The Li contamination of the furnace decreases after processing uncontaminated wafers to a value of about  $1 \times 10^{10}$  at  $\text{cm}^{-2}$  which is the baseline value of the tool contamination. In addition, the growth rate shows a significantly increasing curve with a difference of  $1.15 \text{ nm min}^{-1}$  between the reference wafers and the Li-contaminated wafers at  $1 \times 10^{13}$  at  $\text{cm}^{-2}$  (contamination level 3). Consequently, it can be said that the contamination level of Li has a considerable influence on the oxide growth rate. An explanation for the increased growth may be an expansion of the volume due to the insertion of Li and a formation of Li-silicates (e.g.,  $\text{Li}_2\text{Si}_2\text{O}_5$ ,  $\text{Li}_4\text{SiO}_4$ ) and  $\text{Li}_2\text{O}$ . Care must be taken in front-end-of-line processes, e.g., the gate oxidation of transistors. However, the formed silicon oxide layer is uniform and Li contamination has no influence on the roughness. The electrical measurements have shown that a Li-contaminated furnace leads to a deterioration of the silicon oxide quality. In addition, Li contamination of  $1 \times 10^{13}$  at  $\text{cm}^{-2}$  supplies additional electrons as fixed and mobile charge carriers. This indicates an interstitial doping with Li and implies that Li can have a detrimental effect on devices. The study provides a basis for the assessment of the impact of Li in CMOS clean room environments and thus the first step for the controlled use in state-of-the-art cleanroom facilities.

### 4. Experimental Section

**Intentional Contamination:** Bare Si wafers were deliberately contaminated with Li by spin coating at different contamination levels:  $1 \times 10^{11}$  at  $\text{cm}^{-2}$  (level 1),  $1 \times 10^{12}$  at  $\text{cm}^{-2}$  (level 2), and  $1 \times 10^{13}$  at  $\text{cm}^{-2}$  (level 3). Li solutions with different concentrations were prepared depending on the desired concentration on the surface of a 200 mm wafer. A single Li element stock solution with  $1000 \text{ mg L}^{-1}$  from Thermo Scientific was diluted with ultrapure water and 69.5%  $\text{HNO}_3$  to a resulting  $\text{HNO}_3$  concentration of 1%. The wafer was placed in a POLOS 300 spin coater from SPS, 100 mL of the contaminated solution was poured on the wafer to cover the whole surface, and after 1 min of exposure time, the wafer was spun for 2 min at 2000 rotations per minute. This process allowed homogeneous contamination and drying of the wafer.



**Figure 8.** Schematic illustration of the VPD process.

**Oxidation:** Following contamination, the wafers were dried for 24 h before they were used further. Then, a thermal silicon oxide of 40 nm was formed at 950 °C under oxygen at atmospheric pressure for 90 min in a horizontal furnace dedicated to Lithium from ACTEMIUM (branch of VINCI Energies). During the oxidation, the gases flow continuously through the quartz tube. To minimize the cross-contamination risk, one safety measure was the use of a closed cage for Li-contaminated wafers. This closed cage has holes to allow the gas flow and thus the oxidation of the wafers; nevertheless, the wafers are more shielded than in the usual open boat.

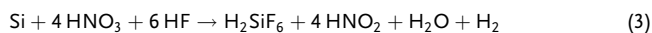
**Analytical Techniques:** VPD–ICP–MS was used to quantify Li contamination on the surface of the wafers. The VPD tool Rigaku V300 was used together with the Agilent 8800 ICP–MS. The VPD technique is a sample preparation that enables the analysis of metallic contaminations in and directly under the silicon oxide layer. **Figure 8** illustrates the layers with the metallic impurities and the VPD process in a schematic way.

First, the decomposition by HF vapor dissolves the silicon oxide layer according to the chemical reactions shown in Equation (1) and (2).<sup>[33,39]</sup>



Afterward, a droplet scans the surface and collects all mobilized contaminants. This droplet can then be analyzed by ICP–MS to quantify the metallic contaminants. As scanning solution, a mixture of 2% HF and 2% H<sub>2</sub>O<sub>2</sub> is used. This technique allows to analyze the Li concentration on Si wafers after the intentional contamination to determine the real concentration on the wafer. In addition, the Li concentration in the silicon oxide can be determined after the oxidation process. The values were restricted by the MDL. To determine the MDL, the errors of all process steps had to be included; therefore, the noise of blank samples that have passed through the entire analysis process was considered.<sup>[40]</sup> Thus, blank samples are produced by performing the entire VPD process with bare Si wafers and the resulting solution for the ICP–MS analysis contains all human and mechanical manipulations and influences. This value is usually higher than the classical limit of detection, which only includes the noise of the ICP–MS during the analysis of an unprocessed blank sample. As already the presence of contamination is important in the semiconductor sector, a limit of quantification was not calculated. For Li, the MDL is  $1.0 \times 10^8$  at cm<sup>-2</sup> for VPD–ICP–MS surface analyses.

Following the VPD–ICP–MS measurement, LPD bulk ICP–MS analyses were performed to measure the Li concentration in the first two μm of the Si bulk. It was used to analyze Li diffusion into the Si bulk after the temperature influence of the oxidation process. For this process, a mixture of HNO<sub>3</sub> and HF was used as digestion solution. During LPD bulk, the wafer was clamped in a polytetrafluoroethylene mold that was the same size as the wafer and was then completely covered with the digestion solution to ensure a homogeneous etching process.<sup>[41]</sup> During an exposure time of one hundred seconds, the reaction from Equation (3) is assumed to take place.<sup>[33]</sup> The pipetted solution was afterward analyzed with the Agilent 7900 ICP–MS.



The MDL for LPD bulk ICP–MS analyses is  $3.1 \times 10^9$  at cm<sup>-2</sup>; as this is a different method with different chemicals and more human influences, the value is higher than for VPD–ICP–MS.

The influence of Li contamination on the oxide growth rate was evaluated measuring the oxide thickness by ellipsometry. 49-point mappings of the entire 200 mm surfaces have been recorded using the Atlas XP+ from Nanometrics.

To investigate the topography of the silicon oxide, AFM measurements were used to analyze the effects of increasing Li concentration on oxide roughness. For this purpose, the topography was analyzed with a fine tip on areas of 1 μm × 1 μm and 10 μm × 10 μm in the center and at the edge of the wafers using the FastScan AFM from Bruker.

Furthermore, electrical measurements with a CVM92-A from Four Dimensions were performed to observe the impact of Li contamination on the silicon oxide quality. The tool performs electrical C/V and G/V measurements by using a mercury electrode. The mercury electrode had a dot area of 0.0005 cm<sup>2</sup>. At a frequency of 1 kHz, voltages of 5 to –5 V for p-doped and –5 to 5 V for n-doped wafers were applied to measure the C/V and G/V curves. To ensure accurate calculations, the actual SiO<sub>2</sub> thicknesses at the measurement points were determined in advance. The D<sub>IT</sub>-values were calculated with a Python script written by Fraunhofer IPMS CNT.

## Acknowledgements

This study was supported by TEMPO project. The TEMPO project has received funding from the Electronic Components and Systems for European Leadership Joint Undertaking under grant agreement no. 826655. This Joint Undertaking receives support from the European Union's Horizon 2020 research and innovation program and Belgium, France, Germany, Switzerland, The Netherlands. Special thanks to Fabrice Nemouchi who made this study possible as well as to Thierry Lardin and Delphine Autillo from the conta metal team at CEA-Leti for their great support during the realization of the experiments. Furthermore, the authors would like to thank Vincent Lafage, Xavier Garros, and Tadeu Mota Frutuoso for their support with the electrical measurements and not to forget the laboratory manager Nicolas Chevalier for his support, e.g., during the evaluation of the AFM measurements.

Open Access funding enabled and organized by Projekt DEAL.

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.



## Keywords

cleanroom, complementary metal–oxide–semiconductor, contamination, diffusion, lithium, silicon oxide, VPD–ICP–MS

Received: February 23, 2024

Revised: April 17, 2024

Published online: May 16, 2024

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