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Two-level Stacked Nanowire MOSFETs: A Low Temperature Analysis of the Low-Field Mobility Degradation Factors

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Abstract— This study explores the carrier mobility and its degradation factors in relation to temperature for 2-level stacked nanowire MOSFETs within the temperature range of 100 K to 400 K. The low-field carrier mobility and its degradation factors were extracted using the Y-function. Additionally, it was observed that the peak transconductance is achieved at a higher overdrive voltage ($V_G - V_{TH}$), particularly as the temperature decreases. Notably, the low-field mobility is more sensitive in wider devices. Compared to other technologies such as omega-gate nanowires and planar fully depleted SOI transistors, this technology exhibits less sensitivity of low-field mobility to temperature variations. The first-order degradation factor was observed to decrease with rising temperature, while the second-order factor exhibited an increase within the same temperature range. The variation in the first and second order degradation factors with temperature is more pronounced in wider devices.

Index Terms—2-level stacked nanosheets, MOSFETs, Electrical Characterization, Low-temperature.

I. INTRODUCTION

Multiple-gate field-effect transistors (MuGFETs) stand out as some of the most dependable devices, allowing the continued downscaling of MOSFETs into the nanometer range [1], [2]. Vertically stacked nanowire MOSFETs, also known as stacked nanowires, present promising prospects for future technological nodes [3], [4], [5]. They effectively enhance the current density of nanometer-long MOSFETs without increasing the silicon footprint while maintaining commendable performance and scalability. These MOSFETs are constructed with two or more levels of superimposed narrow and thin silicon layers, often referred to as nanosheets. These layers are enveloped by the gate stack, ensuring robust electrostatic control over the channel charges, and mitigating the occurrence of short-channel effects[3].

Beyond technological scaling, it is established that operating MOSFETs at low temperatures improves various electrical properties of the devices, including carrier mobility and subthreshold slope[6], [7], [8].

Our previous results published in [9] are here extended by providing additional results in a wider temperature range. The significance of studying advanced transistors under low-temperature conditions is underscored by the growing importance of quantum computing[10], [11]. As the field of quantum computing advances, the demand for precise control and understanding of semiconductor devices at extremely low temperatures becomes paramount[11]. Understanding how fundamental parameters such as low-field carrier mobility and its degradation factors behave with temperature variation is of great importance for the design of

reliable circuits and systems[1], [12].

Given this context, the following study develops the behavior of the carrier mobility and its degradation factors in the temperature range between 100 K and 400 K and relate them to scattering mechanisms.

II. DEVICE, EXPERIMENTS AND METHODS

The devices were manufactured at CEA-Leti in France, featuring 2-level n-type silicon stacked nanowire MOSFETs on Silicon-On-Insulator (SOI) wafers with a buried oxide thickness of 145 nm. The undoped body region is enclosed by a gate stack of HfSiON and TiN gate metal. The equivalent oxide thickness (t_{ox}) is approximately 1.3 nm. Devices with variable fin width (W_{FIN}) of 10 nm, 20 nm, and 25 nm, and a fixed channel length (L) of 100 nm were measured. The silicon thickness (H_{FIN}) at each nanowire level, along with the vertical separation between channels, remains constant at 9 nm[3].

To assess thermal performance, each transistor underwent temperature exposure ranging from 100 K to 400 K using the Low-Temperature Micro-Probe (LTMP) System from MMR Technologies. Post-stabilization at the designated temperatures, we recorded drain current (I_D) versus gate voltage (V_G) curves using a Keysight B1500 Semiconductor Characterization System. The applied drain voltage (V_D) was maintained at 25 mV and 40 mV, while V_G varied from 0 V to 1.1 V in increments of 10 mV.

III. RESULTS AND DISCUSSION

In Figure 1, the $I_D \times V_G$ curves are presented for temperatures ranging from 100K to 380K for one of the studied transistors with $W_{FIN} = 10$ nm, $L = 100$ nm, and an applied drain voltage of 25 mV, for both linear and logarithmic scales.

From Figure 1, a steeper slope is noticeable in the subthreshold region for lower temperatures. The obtained threshold voltages vary from 0.59 V (at 380K) to 0.72 V (at 100K) and the inverse subthreshold slope remains close to the theoretical minimal value obtained by the relation ($S = k T/q \ln 10$), both characteristics have been previously discussed and presented in earlier works[9], [12], [13]. The Zero-Temperature Coefficient (ZTC) denotes the gate bias at which temperature fluctuations have minimal impact on the drain current [14] and for this device this point is clearly noticeable around 0.95V, above the threshold voltage for all temperatures. This clearly defined ZTC point indicates a reduced series resistance variation over the temperature.

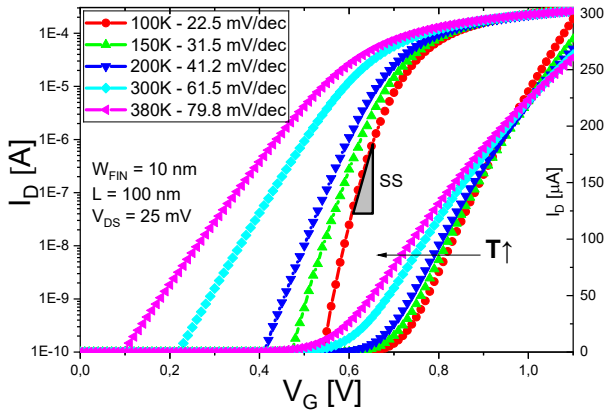


Figure 1 - Drain current as a function of gate bias with $V_D = 25$ mV. The same data is plotted in linear and logarithmic scales.

Figure 2 shows the transconductance as a function of gate voltage, within the studied temperature range. It is obtained from the derivative of the drain current curves with respect to the gate voltage. With the decrease in temperature, the transconductance reaches higher values, and these values are attained at higher gate voltages[9]. Similar behavior is also observed in other technologies[15], [16]. Table I presents the gate voltage overdrive ($V_{GT} = V_G - V_{TH}$) for the maximum transconductance in the whole temperature range.

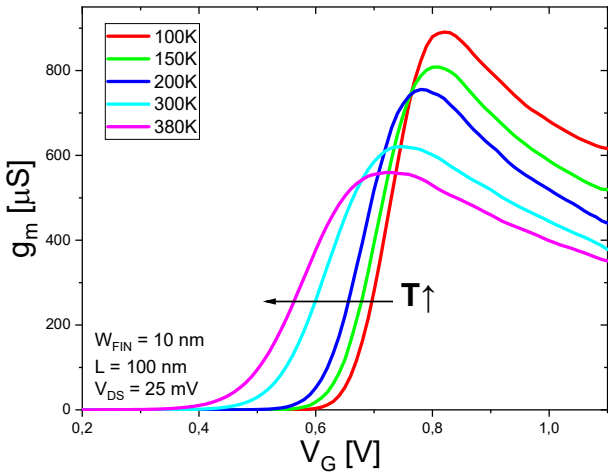


Figure 2 - Transconductance as a function of the gate bias.

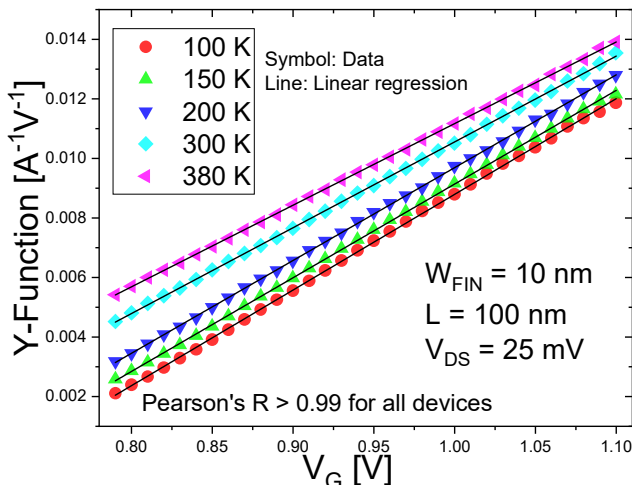


Figure 3 - Y-function by the gate bias for $V_D = 25$ mV, for a device with $W_{FIN} = 10$ nm and $L = 100$ nm.

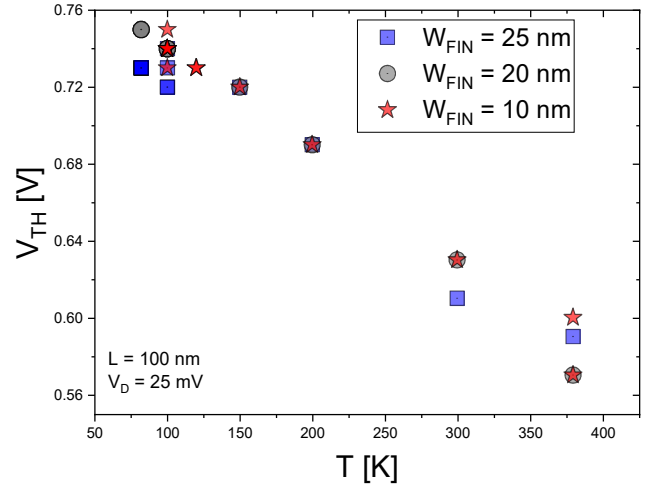


Figure 4 - Threshold Voltage as a function of temperature for devices with 10 nm, 20 nm and 25 nm of width.

In the following analysis, the study of mobility and degradation factors is further explored. The acquisition of these data comes from the curves, Figure 1 and Figure 2, already presented, and the application of the 'Y-function'[17], [18] method, a numerical method well-established in the literature that disregards the effects of series resistance.

The extraction of electrical parameters using the Y-function method is highly dependent on the linear regression in the linear region of the Y-function. Figure 3 shows the plot of the Y-function as a function of gate voltage and the linear regression for each temperature of that device. This demonstrates good linearity, with R-squared values above 0.99 for all the devices studied in the entire temperature range.

Figure 4 illustrates the threshold voltage for devices with $L = 100$ nm and fin widths W_{FIN} of 10, 20, and 25 nm. It is observed that the threshold voltage exhibits a linear trend with respect to temperature variations while showing no relevant dependence on variations in fin width[13].

As the analysis relies on a numerical method applied to experimental data and is therefore susceptible to variations, we applied the method to various samples from different chips on the same wafer. Figure 5 illustrates the maximum low-field mobility for several W_{FIN} as a function of temperature. It can be observed that wider devices are more sensitive to temperature variations, a behavior already observed and attributed to the higher contribution to the total current conduction from the upper and lower planes (100 plane) with higher carrier mobility compared to the conduction in the side walls (110) [9], [13]. To emphasize this trend, Table 1 presents the slopes of the curves derived from linear regression of the plotted data, the fitted curves.

As observed in [12] for devices from the same technology, this kind of device is less sensitive to temperature changes than others. This characteristic can be a favorable aspect for applications with significant temperature variations. For comparative purposes, Table 2 compares the percentage variation in low-field mobility for a decrease of 100K (300K to 200K) among other technologies. To ensure a fair comparison between the technologies, devices with similar channel lengths (L) were selected. Such as planar fully depleted (FD) SOI ($L = 90$ nm), SOI FinFET ($L = 90$ nm), and SOI Ω -Gate Nanowire ($L = 100$ nm).

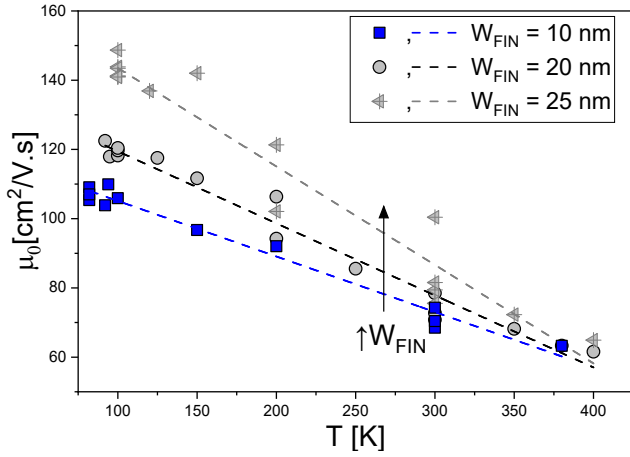


Figure 5- Low-field mobility versus Temperature.

Table 1 - Slopes of the linear regression of maximum low-field mobility in function of temperature.

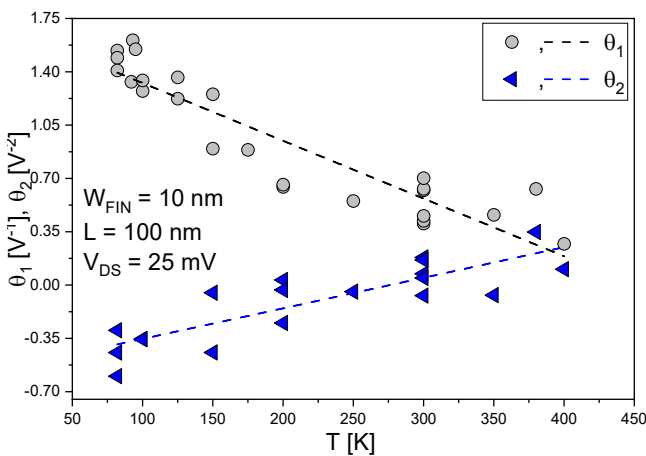
W_{FIN} [nm]	$d\mu_0/dT$ [$\text{cm}^2/\text{V.s.K}$]
10	-0.16
20	-0.21
25	-0.28

Table 2 - List of technologies and the percentage improvement in low-field mobility at 200K compared to a temperature of 300K.

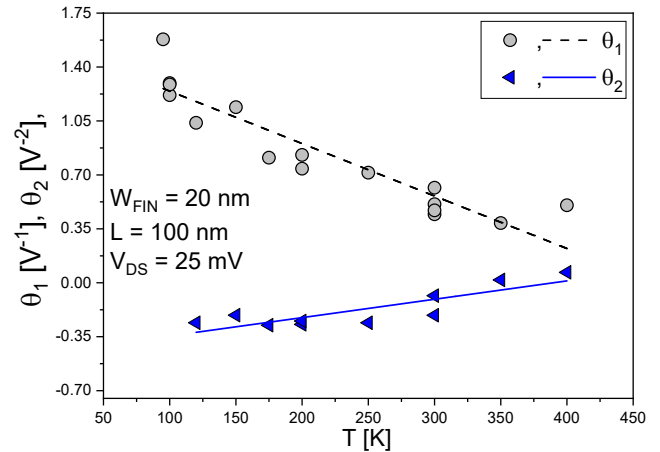
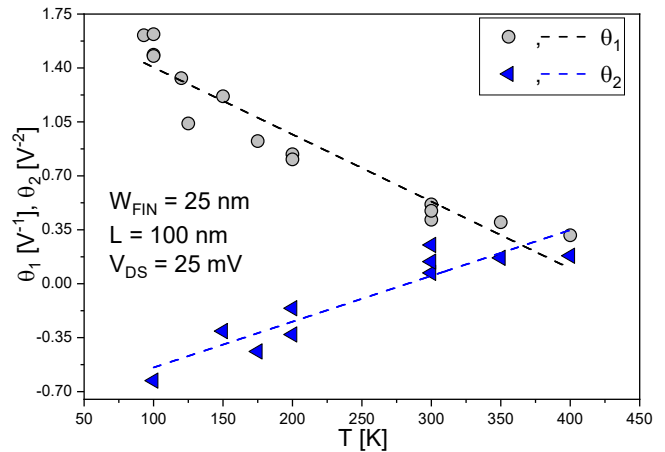
Technology	$\uparrow\% \mu_0$ (300K – 200K)
Ω-Gate Nanowire[19]	$\sim 40\%$
FinFET [15]	$\sim 35\%$
FDSOI [20]	$\sim 40\%$
2-level Stacked Nanowire	$\sim 24\%$

Equation (1) relates effective mobility (μ_{eff}) to maximum low-field mobility (μ_0), degradation factors (θ_1, θ_2), gate voltage (V_G), and threshold voltage (V_{TH})[7], [21]:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_G - V_{TH}) + \theta_2((V_G - V_{TH}))^2} \quad (1)$$

Figure 6 – Mobility degradation factors as a function of temperature for devices with $W_{FIN} = 10\text{nm}$.

In Figure 6 and Figure 7, the obtained values of mobility degradation factors are presented as a function of temperature for different fin widths. The data distribution was approximated to a linear regression, and their slopes are presented in Table 3 and Table 4, respectively. The data presented in these tables indicate that both first and second-order degradation factors variation with temperature are dependent on the fin width. The wider transistor presents a larger variation of the mobility degradation factors, which suggests a correlation between scattering phenomena and the electrostatic coupling, crystallographic orientation.

Figure 7 – Mobility degradation factors as a function of temperature for $W_{FIN} = 20\text{nm}$.Figure 8 – Mobility degradation factors as a function of temperature for $W_{FIN} = 25\text{nm}$.

From the presented data in Figure 6, Figure 7 and Figure 8, one can see a clear downward trend in the first-order degradation factor (θ_1) with increasing temperature and an increase in the second-order degradation factor (θ_2) with rising temperature. Both behaviors are consistent across all studied devices, with channel width showing no impact on the exposed data. Comparing the slopes presented in the tables, it is evident that θ_1 is more sensitive to temperature changes than θ_2 , as the absolute values of the slopes of its curves are larger. Different trends of variation in these factors were observed in FDSOI[20], [22] and in planar CMOS technologies [7].

Table 3 - Slopes of the linear regression of θ_1 in function of temperature.

W_{FIN} [nm]	$d\theta_1/dT$ [V^{-1}/K]
10	-3.6E-3
20	-3.4E-3
25	-4,3E-3

Table 4 - Slopes of the fitted curves of θ_2 in function of temperature.

W_{FIN} [nm]	$d\theta_2/dT$ [V^{-2}/K]
10	2.0E-3
20	1.2E-3
25	2.9E-3

This difference is attributed to the change in the scattering mechanism with greater impact as the temperature changes. At lower temperatures, surface roughness predominates[20], [23], and with the increase in temperature, its relevance decreases. A behavior similar to that presented by θ_1 and also observed in[24].

The increase in low-field mobility with decreasing temperature is attributed to the reduction of phonon scattering[7], [20], a behavior corresponding to that presented by θ_2 .

In equation (2), we have the transconductance model obtained with the parameters extracted by the Y-function.

$$g_m = \frac{\mu_{eff} C_{ox} W_{eff} V_{DS} (V_G - V_{TH})}{L} \quad (2)$$

where C_{ox} is the gate oxide capacitance per unit area, W_{eff} is the effective channel width.

To validate the efficacy of the employed methodology, Figure 9 illustrates the experimental transconductance juxtaposed with its counterpart reconstructed by the model. A good agreement is found in every temperature.

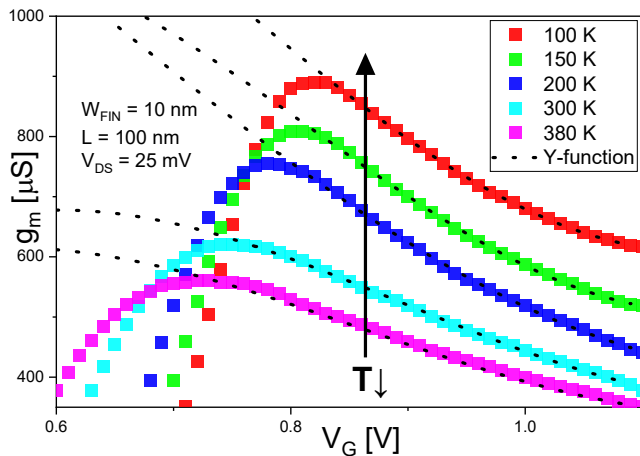


Figure 9 - Transconductance Experimental and Transconductance obtained by the Y-function method.

IV. CONCLUSION

This study provides an examination of how temperature influences device characteristics and performance metrics in 2-level stacked nanowire transistors with varying channel

widths. Our findings clearly illustrate that wider channel devices demonstrate increased sensitivity to temperature changes, particularly affecting low-field mobility and the degradation factors, θ_1 and θ_2 . Also was observed a clearly ZTC point at 0,95 V, which indicates a reduced impact of the series resistance with the temperature lowering. The sensibility of low-field mobility was compared to other technologies and the 2-level stacked nanowire shows a lower sensibility compared to the other technologies with indicates a robustness of the operation of these devices. As wider devices show heightened sensitivity not only in mobility but also in how temperature impacts the first-order (θ_1) and second-order (θ_2) degradation factors. Notably, θ_1 is more affected by temperature variations than θ_2 , which aligns with the dominant surface roughness scattering mechanisms observed at lower temperatures.

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