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Temperature Dependence of 1200V-10A SiC Power Diodes: Impact of Design and Substrate on Electrical Performance

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Introduction: Bulk 4H-SiC substrates growth requires a long, energy-intensive and costly process, which limits the availability of SiC substrates for devices production today. Consequently, 3C-poly silicon carbide substrates (pSiC) are currently being considered as an alternative for SiC power devices fabrication. For example, utilizing the Smart Cut™ technology, SmartSiC™ substrates are engineered to achieve better device yield and to optimize conduction losses [1] by bonding a high quality mono crystalline 4H-SiC layer on top of a low resistivity poly-SiC substrate (reported to offer about one order of magnitude lower resistivity values [1]). In this work, we study the impact of temperature on the static electrical parameters of 1200V power 4H-SiC diodes with various designs and architectures (Schottky, JBS, hexagonal and stripe cells) fabricated on 150 mm bulk 4H-SiC and 3C-pSiC based substrates (SmartSiC™). Additionally, switching characteristics were investigated, revealing no significant dependency on the substrate type.

Devices Fabrication: Three power diodes architectures (Schottky, PiN, and JBS: **Fig. 1a-b**) were fabricated with a process flow designed for 1200V blocking voltage capability [2], with Al implanted p+ guard rings and a JTE annealed at 1700°C to achieve the breakdown voltage target (**Fig. 1c**). Various anode and edge terminations were designed and fabricated on both 4H-SiC bulk and SmartSiC™ substrates (**Fig. 1d**). The substrates were not thinned and backside contact formation was performed using laser annealing.

Results and Discussion: I(V) measurements were carried out in both reverse and forward modes to assess the impact of designs and substrates. **Fig. 2** highlights the off-state characteristics with examples of three reference diode types that were reverse biased on both bulk and SmartSiC™. Non-destructive avalanche mode was reached with similar performance (leakage, V_{AV}) observed for both substrates (due to identical drift layer and device structure). Wafers mapping and yield evaluation confirmed a minimal substrate contribution to defects that could propagate to the epilayer, leading to off-state performance degradation such as BPDs or TEDs [3]. As expected from SiC impact ionization coefficients, avalanche voltage increased at elevated temperatures for all designs and substrates types.

Specific differential resistance (R_{DIF}) decreased as Schottky surface ratio increased for both bulk and pSiC-based substrates (**Fig. 3**). With our design, hexagonal configuration resulted in lower resistances (**Fig. 3b**). In all cases, the JBS fabricated on SmartSiC™ exhibited a high current conduction and less resistance in the ohmic regime (Fig. 3a), confirming the impact of the substrate resistivity. **Fig. 4** shows the JBS R_{ON-BV} figure of merit for the studied samples with a comparison to state-of-the-art JBS diodes [4]. The observed conduction gain for the SmartSiC™ sample (compared to bulk) was further investigated at high temperatures in **Fig. 5**. This figure illustrates that the extracted R_{DIF} between 25 to 200°C exhibited an exponential temperature dependence. At 200°C, the absolute R_{DIF} difference further increased by +0.5 mΩ.cm² with a relative difference remaining at 21%. **Fig. 6** proposes another way to evaluate the impact of the diode design/substrate on the resistance-temperature dependence by plotting $R_{DIF}(200^\circ\text{C})$ versus $R_{DIF}(25^\circ\text{C})$. Based on the observed trend across all data (including additional 1.7 kV epiwafer with same device process [2] and ref [5]) we can infer that all diodes designs (regardless of the epi or the substrate) follow the same predictive $R_{DIF}(T)$ model proposed in Fig. 6. In **Fig. 7**, Schottky R_{DIF} at 200°C has been segmented into its three main contributions. SmartSiC™ substrate (350μm, no thinning) exhibits lower resistance even compared to thinned (110μm) bulk epiwafer.

- [1] E. Guiot *et al.*, PCIM Europe 2022, Nuremberg, Germany, 2022, pp. 1-7.
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 [4] A. Gendron-Hansen *et al.*, Materials Science Forum, Vol. 924 (June 2018), pp. 585-88.
 [5] J. Millan *et al.*, 2008 International Semiconductor Conference, 2008, pp. 53-59.

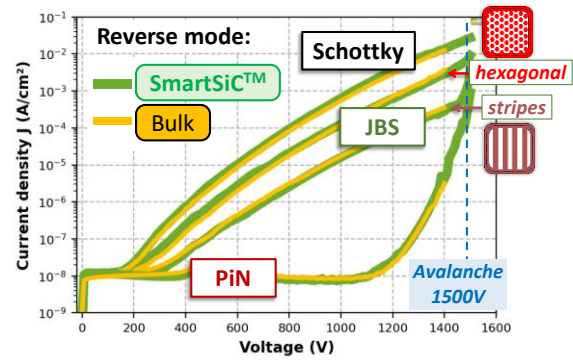
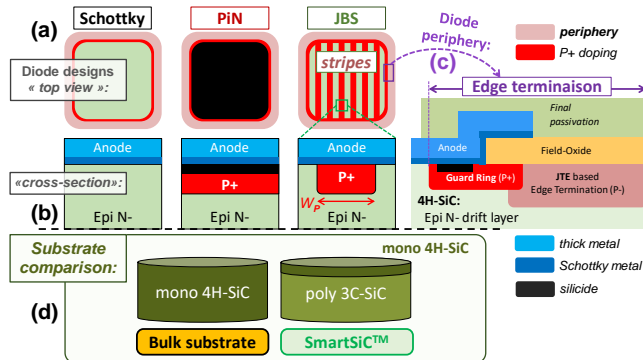


Fig. 1. Description of diodes samples (Schottky, PiN, and JBS) - **a)** top view, **b)** anode cross-section with **c)** edge termination cross-section at the diode periphery; and stripes) and PiN. Anode surface is 2.01mm².
d) standard 4H SiC bulk and new SmartSiC™ wafers.

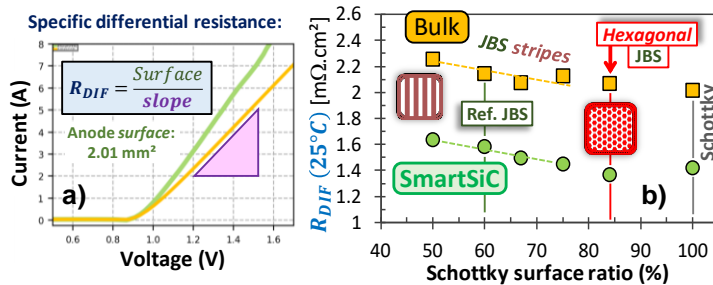


Fig. 3. Specific differential resistance R_{DIF} (definition in a) for different JBS diode designs (+Schottky) as function of the Schottky surface ratio.

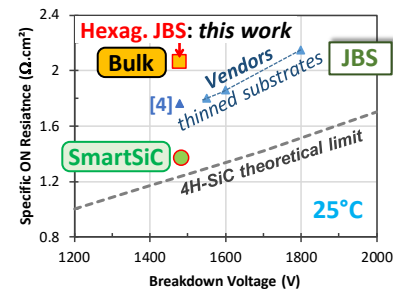


Fig. 4. Hexagonal JBS specific ON resistance versus breakdown voltage (bulk, SmartSiC™), compared to similar diodes (incl. commercial products) [4].

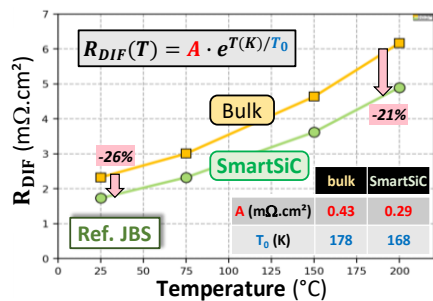


Fig. 5. Impact of temperature (25-200°C) on measured specific differential resistance (R_{DIF}) for JBS diode (reference design). For both samples, the data can be fitted using an exponential model (as observed for results in [5], cf. Fig. 6).

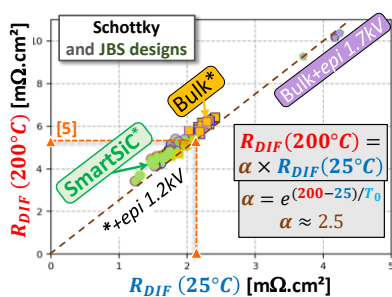


Fig. 6. Measured differential resistance at 200°C vs. 25°C for various JBS designs (+Schottky) on different sites (for two wafers with same 1200V epi, +1700V bulk epiwafer). Ref [5] data are in agreement with the observed trend.

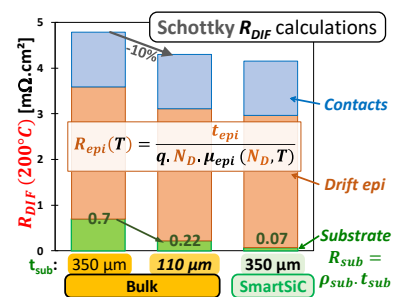


Fig. 7. R_{DIF} (at 200°C) partitioning calculations for Schottky Barrier diodes (SBD) with same epi. For bulk epiwafer, R_{DIF} is reduced by -10% with substrate thinning. SmartSiC™ substrate enables further reduction without thinning.