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New Insights using Avalanche Mode for On-wafer Evaluation of SiC Diodes Technology and Design Ruggedness

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Abstract— On-wafer measurements of 1200V rated 4H-SiC power diodes have been performed in near avalanche mode to investigate the stability and robustness of the devices. The method consists of biasing the SiC diodes at near-avalanche current or voltage levels for a variable period of time. The drifting of the static electrical parameters (leakage current, avalanche voltage, Schottky barrier height) is then studied. For two different SiC diode processing technologies, two drift behaviors of the blocking I-V curves were observed. Impact ionization, which is responsible for the avalanche phenomenon at high electric fields, has been localized and distinguished between the active region of the devices and the edge termination region, depending on the processing technology. Electroluminescence observations and numerical simulations were performed to confirm the interpretation of the electrical results. The robustness of the method was further supported.

Keywords— SiC, Diode, JBS, on-wafer, avalanche, ruggedness, termination, stress test, TCAD

I. INTRODUCTION

Today most of Si and SiC power devices are avalanche rated. The devices are able to sustain a given energy and current in avalanche mode [1-3], making the component safe in case of overvoltage in the power converter. Avalanche mode can be observed in static I-V curves extracted from on-wafer or packaged devices measurement (Table 1).

TABLE 1 USUAL HIGH VOLTAGE RELIABILITY CHARACTERIZATION METHODOLOGIES [1,2,3] FOR SiC DEVICES AND BASIC COMPARISON WITH THE PROPOSED METHOD (FIG. 1).

Method:	HTRB	H3TRB	UIS	This work
DUT	package	package	package	On-wafer
Set up	High voltage power supply, 1000 h	Climatic chamber, high voltage supply	High current / high voltage power supply	Wafer prober, high voltage SMU
Advantages	« Si legacy »	Passivation and package oriented	Establish true device performance limits (SOA)	Non destructive, Avalanche localisation
Limitations	not (always) suitable for SiC, time consuming	Heavy set-up, time consuming	Destructive	Preliminary ruggedness assessment

Avalanche is caused by impact ionization phenomena involving both holes and electrons flowing in the drift area, independently of the unipolar or bipolar nature of the device. Having a high density of electrons and holes under high electric field bias may generate degradation events not seen during standard operation electrical tests. In this work, we present an innovative stress methodology (Fig. 1) to evidence electrical parameters drift caused by the power device design or its processing technology. This method was applied to 4H-SiC 1200V rated power diodes for validation purpose.

II. PROPOSED METHODOLOGY

The key advantages of the proposed method are the following:

- We test the devices on-wafer using solely a wafer prober and a HVSMU (Fig. 1a).
- The method allows to test and compare devices (featuring different architectures, different designs) co-integrated on a single wafer.

This approach can be easily implemented to perform a relatively fast preliminary screening (compared to usual reliability techniques) of new designs or any technological change. The method is composed of three main steps (described in Fig. 1b).

- Step 1 consists in a standard blocking mode I(V) measurements. In the case of the tested SiC diodes, an example of reverse I(V) curve [4] is illustrated in Fig. 1a. It enables to identify the current at which avalanche starts (I_{AV}).
- Step 2: a new measurement of the same device is set to apply a DC current stress slightly above I_{AV} for a given duration (Fig. 1b). We can bias either in voltage or in current, which leads to similar results. For better accuracy, biasing in current is preferred since the current range is larger than the voltage one above avalanche.
- Step 3 (and 4): Standard blocking mode I(V) measurement (similar to step 1) is performed in order to highlight an eventual drift of the electrical behavior. Furthermore the time-dependence recovery of the shifted I(V) can be investigated through additional measurement (step 4).

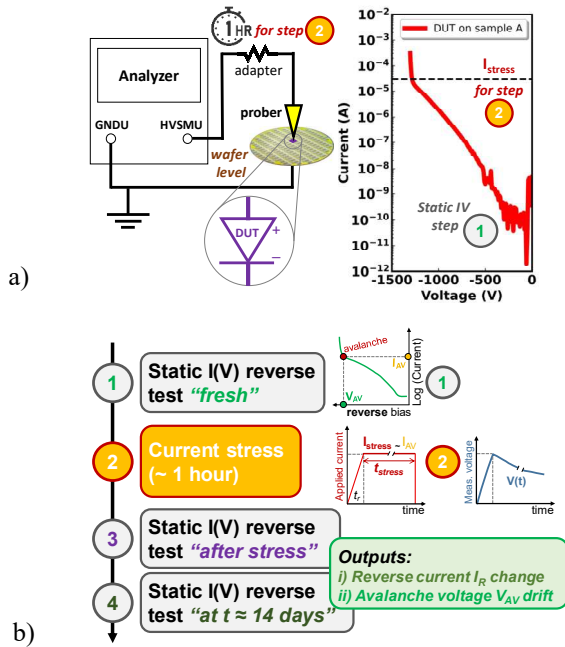


Fig. 1: a) general concept of the proposed test method based on avalanche mode bias starting with on-wafer static I(V) reverse characteristic measurement using high voltage SMU. b) Test sequence for the proposed method. Step 1 is a standard reverse I(V) measurement. Step 2 is a DC current stress using a constant I_{stress} closed to avalanche (Fig. 1a). Additional static I(V) (step 3 and 4) enable to monitor I_R and V_{AV} potential drift and recovery.

The main interest of this method is the activation of both electrons and holes currents under high electric field bias. This evidences possible instabilities/drifts, which depend on the avalanche breakdown location [5] (active area, and periphery). High temperature can also be applied during step 2 to enhance the physical phenomenon, or during step 3 (and 4) to accelerate the relaxation of the electrical characteristics.

In this first study, 150 mm wafers with 1200 V-rated 4H-SiC power diodes were considered. Tests were performed on SiC JBS power diodes fabricated with two process technologies. The key features and differences of these two SiC technologies are listed in Table 1.

The main variations concern the implanted Aluminum profile, the Schottky contact metal, and the field oxide dielectrics stack.

Table 2 COMPARISON OF THE MAIN TECHNOLOGICAL PARAMETERS BETWEEN THE TWO PROCESSES (SAMPLES A AND B) USED FOR THE FABRICATION OF THE SiC JBS (JUNCTION BARRIER SCHOTTKY) DIODES. FOR PROCESS A, TWO EPI CONFIGURATIONS HAVE BEEN USED ON DIFFERENT WAFERS.

Samples:	A		B
Epilayer doping, thickness	$8 \times 10^{15} \text{ cm}^{-3}$ 12.7 μm	10^{16} cm^{-3} 10 μm	$6.8 \times 10^{15} \text{ cm}^{-3}$ 12.6 μm
P+ surface doping	$4 \times 10^{19} \text{ cm}^{-3}$		$3 \times 10^{19} \text{ cm}^{-3}$
P+ profile depth	500 nm		350 nm
JTE profile dose	$1.2 \times 10^{13} \text{ cm}^{-2}$		$1.1 \times 10^{13} \text{ cm}^{-2}$
JTE profile max. implant energy	360 keV		340 keV
Schottky metal	Titanium (Ti)		Tungsten (W)
Interface dielectric	thermal dry oxide 1		thermal dry oxide 2
Diode active area	2.01 mm^2		2.6 mm^2

III. EXPERIMENTAL RESULTS

In Fig. 2, we show the JBS reverse voltage monitoring at a fixed current stress of 1 hour for both A and B processes (step 2). For both cases, we observe a change of the anode voltage with stress time, but in opposite directions: voltage

increase for A, voltage decrease for B. This discrepancy is attributed to different degradation phenomena, as discussed in next section.

In step 3 of I(V) characteristic shown in Fig. 3 (sample A), the increase of the avalanche voltage (V_{AV}) is confirmed while the leakage current below avalanche remains the same. The V_{AV} drift is not permanent and starts to relax back several hours after the stress (step 4, in Fig. 4).

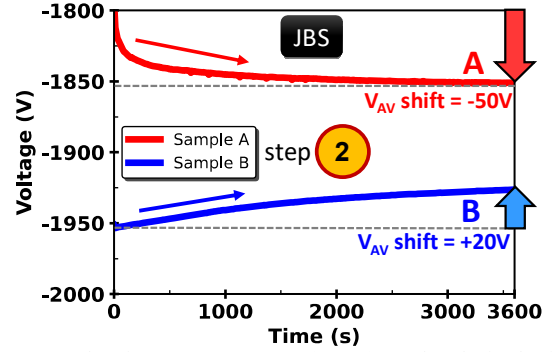


Fig. 2: Example of current stress step (step 2) results obtained with the method for JBS devices from samples A and B. Diode reverse voltage is plotted as a function of time for a 1-hour current stress. The devices are operating in avalanche mode.

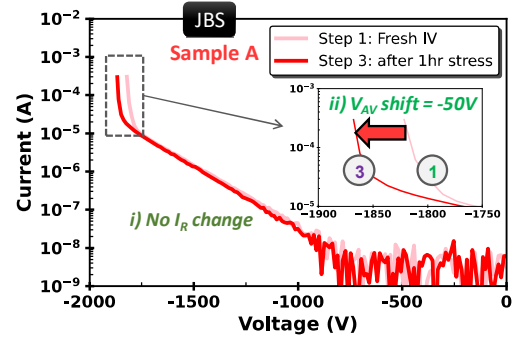


Fig. 3: I(V) curves for step 1 (fresh) and 3 (after 1 hour stress @ 30 μA) for a JBS diode from sample A. Reverse current below avalanche is unchanged, whereas avalanche voltage V_{AV} is shifted (-50 V). Edge termination is a JTE with 4 inner rings + 3 outer rings [8].

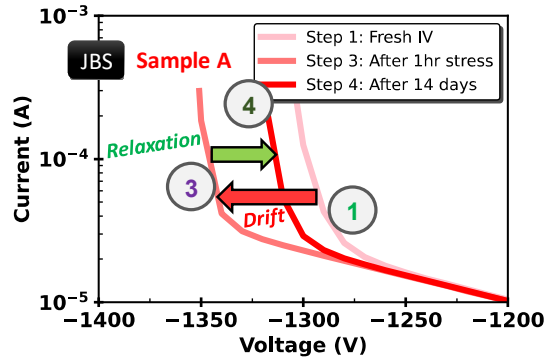


Fig. 4: Example of step 4 results (sample A with 10 μm epi) with partial recovery observed after 14 days. Time constant for recovery is very slow. The drift is not caused by a destructive phenomena, which supports the presence of charge effects in the oxide instead of an oxide structural degradation.

The behavior of sample B (Fig. 5) is utterly different. The avalanche voltage V_{AV} is not affected by the stress, whereas the reverse leakage current before avalanche is 3 times higher. This leakage current is mainly dependent on the Schottky contact properties. From forward I(V) measurements before and after stress (Fig. 6), we can derive a change in the Schottky barrier height of sample B, where we observe a decrease from 1.098eV before stress to 1.011eV after. The drift in sample B is not recovered when measuring after several days (step 4: not shown here). One

can note that the forward I(V) characteristics of sample A is not modified before and after stress (Fig. 6), indicating that the Schottky contact is in this case stable with a Schottky barrier height fixed at 1.57eV (cf. unchanged leakage current in step 3 and 1, Fig. 3).

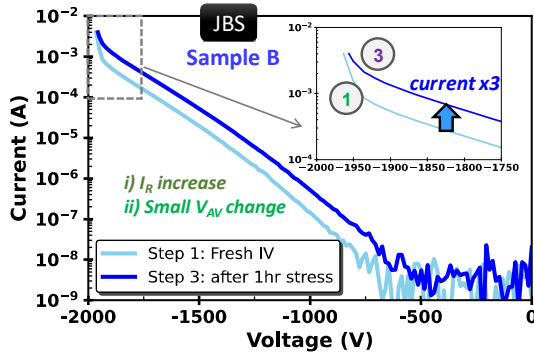


Fig. 5: I(V) curves for step 1 (fresh) and 3 (after 1 hour stress @ 3mA) for a JBS diode from sample B. Reverse current increases here, whereas avalanche voltage is almost not impacted. Edge termination is a JTE with 3 inner rings. P+/Schottky ratio is the same as for JBS of process A.

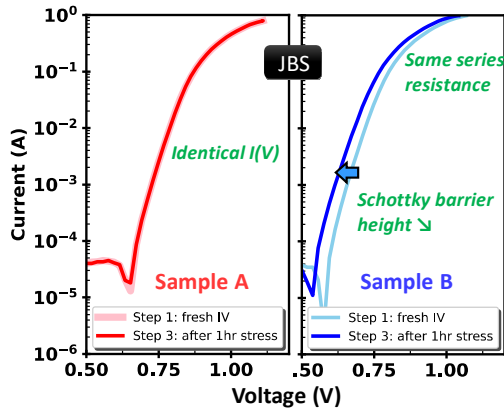


Fig. 6: Forward I(V) measurements to step 1 and 3 for samples A and B highlighting the change (after step 2 stress) in the JBS Schottky barrier height of sample B [6]. Sample A forward characteristics are identical. In both cases, series resistances in the ohmic conduction region are unchanged.

Beside, when applying a stress current corresponding to a voltage below the avalanche point ($I_{\text{stress}} < I_{\text{AV}}$), no drift is observed (Fig. 7). These results highlight the fact that the method implies a stress current close to I_{AV} (and thus that the avalanche process is responsible for the observed drift).

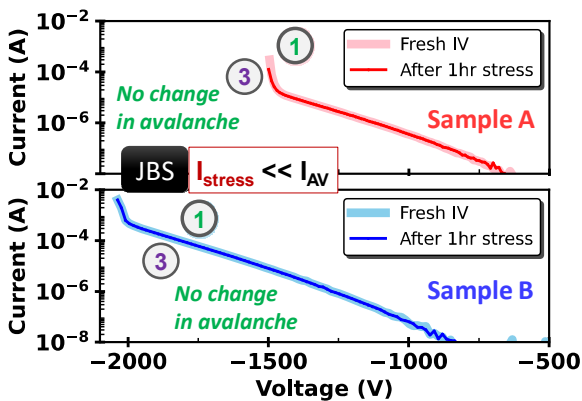


Fig. 7: Reverse I(V) characteristics before and after current stress below avalanche mode. No drift of the curves is observed if current stress ($I_{\mu\text{A}}$ here) is lower than avalanche current level ($I_{\text{AV}} \sim 10\mu\text{A}$ for A, $\sim 500\mu\text{A}$ for B). Sample A characteristics correspond to the 10 μm epilayer wafer. Similar behavior is obtained for the 12.7 μm epilayer wafer of process A.

IV. DISCUSSION ON METHODOLOGY

The required stress current condition ($I_{\text{stress}} \sim I_{\text{AV}}$) tends to indicate that both electrons and holes are involved in the

observed I(V) drift (avalanche). For sample A, the avalanche drift recovery (Fig. 4) indicates that the corresponding effect can be attributed to the trapping and de-trapping of hot carriers. This has been confirmed by a stress under electroluminescence, which demonstrated the presence of light emission around the termination region due to the recombination of electron-hole pairs and the release of light energy (photons) by impact ionization. The stress method leads to the generation of hot carriers, specifically electrons, which gain sufficient energies to be subsequently injected and trapped at the field oxide/SiC interface, in accordance with the increase of the avalanche voltage (Fig. 4, step 3), predicted by simulations. These carriers are then de-trapped, leading to the recovery of the initial characteristics (Fig. 4, step 4). However, the relaxation time constants are unusually high for electron de-trapping. Then, hole trapping may also be involved. Besides, the localization of the electroluminescence (Fig. 8) confirm that these occurrences take place within the termination region of the device.

In the case of **sample B**, the absence of leakage current recovery indicates that no trapping/de-trapping occurs during the stress. The degradation affects the tunneling current through the Schottky contact. Thus, the impact ionization is most probably localized beneath the Schottky contact in the active area. The evolution of the Schottky interfacial properties (anode part, Fig. 6) indicates that the anode area is rather affected by the stress sequence than the termination region. In fact, Schottky interfacial properties were modified by the recombination process with time. The electric field at the anode interface would have caused an image-force barrier lowering, which is responsible of the shift in barrier height seen. This has been confirmed with high current level (around 0.5mA) electroluminescence stress, where no light emission was observed in the periphery area.

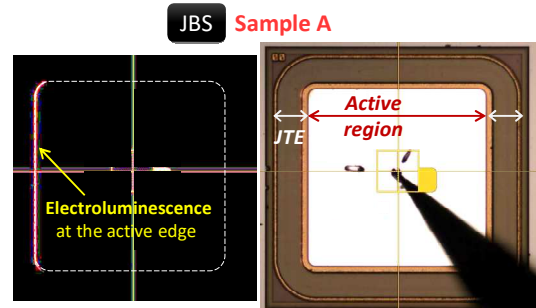


Fig. 8: Top view of a sample A diode under current stress through the probe optical microscope. Electroluminescence generated by electrons-holes recombination is observed on the left side of the active area due to the anisotropy of the impact ionization in the SiC crystal.

To investigate the stress sequence parameters, we tested several stress durations (Fig. 9) and different stress current levels (Fig. 10). Concerning the impact of the stress duration, we observe at least two phases during step 2: for stress duration below 200 s, we see a steady increase of voltage. After 200 s the voltage increase drops. In addition, beyond 5 h, the voltage starts to saturate. Further investigations are needed to clarify the exact reason for these characteristics.

The voltage drift between step 3 and 1 (Fig. 10) clearly depend on the I_{stress} . A minimum I_{stress} value is required (30 μA here) and for stress larger than 100 μA , we observe a saturation in the voltage drift. The cumulative time/current effect can be related to the injected charges, which are responsible for the observed phenomenon, which tends to saturate.

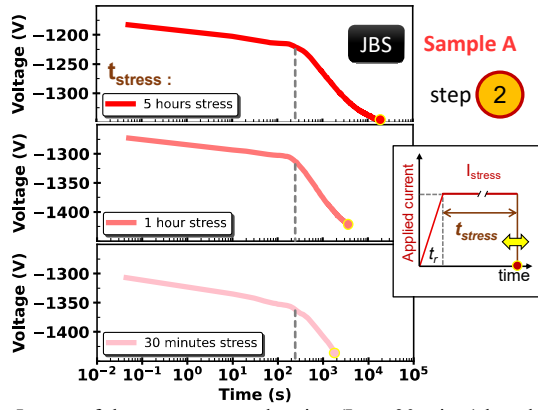


Fig. 9: Impact of the current stress duration (I_{stress} : 30 min, 1 h and 5 h, on three different devices) on the reverse voltage drift during step 2. Log scale for time enables to identify a change in the voltage evolution after 200 s of stress.

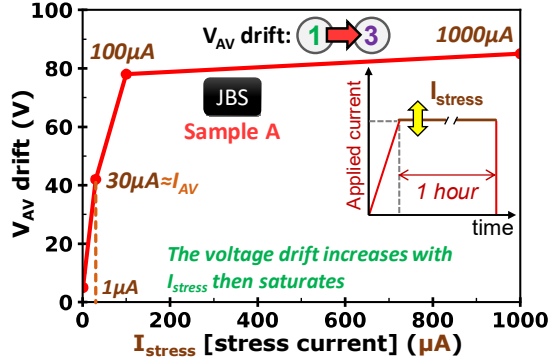


Fig. 10: Impact of the stress current value on the avalanche voltage V_{AV} drift for a 1 hour stress (same design, different devices). Saturation of the V_{AV} drift value is seen above a given current bias (around $100\mu\text{A}$ for the device used in this figure). This value will depend on the device design.

V. SIMULATIONS

We can speculate from the former that the drift may reach a steady level after 5 hours indicating a saturation in the carriers injected in the oxide [7]. From the latter we can presume that the drift widens with high stress current bias to reach the same saturation. TCAD simulations have been performed to better understand the drift mechanism. Simulation results show a strong presence of the electric field around the termination inner rings (Fig. 11). This is in agreement with the localized peaks of impact ionization rates observed in Fig. 12. These hot spots of generated electron-hole pairs are the direct cause of light emission seen by electroluminescence in Fig. 8.

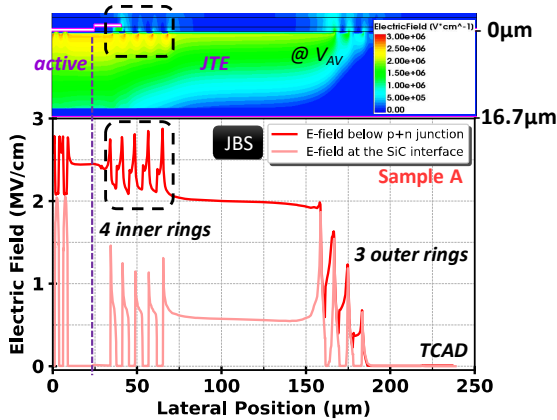


Fig. 11: TCAD simulation showing the electric field distribution: a) 2D mapping, b) corresponding outlines at the surface of the SiC, and below the junctions of the p^+ rings. The e-field peaks beneath the inner rings correspond to the electroluminescence location (Fig. 8).

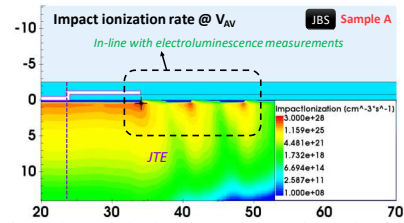


Fig. 12: Simulated impact ionization 2D mapping of sample A JBS (via TCAD Sentaurus). Peaks around the first 3 internal p^+ guard rings at the beginning of the JTE during avalanche mode are observed. Combined with electroluminescence, these peaks endorse the assumption of injected hot carriers into the oxide at the JTE edge (same region of light emission).

VI. CONCLUSION

In summary, the proposed current stress in avalanche mode allows to evidence possible degradation phenomena in SiC power diodes. From the different samples put under test, we observed two separate drift types. For sample A, an increase in the avalanche voltage is caused by the injection of hot carriers into the passivation layer covering the termination region, which in turn manipulates the charge balance and affects the electric field distribution around the termination region. In sample B, no drift in the avalanche voltage was seen. However, a clear increase in the reverse leakage current and the extracted Schottky barrier height was observed. The electric field at the anode interface would have caused an image-force barrier lowering, which is responsible of the shift in barrier height seen. Another hypothesis is than local self-heating modified the structural characteristics of the metal-semiconductor interface, like a crystallization of the tungsten layer used in this sample.

This stress test method performed on-wafer brings new insight into the device characteristics. The possibility to perform the test on-wafer shortens the development phase. This non-destructive test is potentially useful as a wafer level reliability (WLR) protocol to control the stability of a fabrication process in a production line and the long-term reliability of the device.

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