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Impact of the recessed gate depth on the GaN metal-oxide-semiconductor high electron mobility transistor performances: New insights on mobility extraction


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
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ABSTRACT

This paper provides a comprehensive study of the impact of the gate recess depth (RD) on the GaN-on-Si MOS-HEMTs DC performances. $I_{DS} = f(V_{GS})$ and $I_{DS} = f(V_{DS})$ measurements are conducted at 25 and 150 °C, respectively, in forward and blocking modes. The gate recessed depth (50, 150, and 350 nm) is modulated by adjusting the plasma etching time, which is a critical step for improving the dielectric/GaN interface quality and the gate channel electron mobility. Three distinct regions can be defined separately: the bottom, the sidewall, and the corner region being the junction between the two previous regions. To assess the impact of gate recessed depth (RD) on the several mobilities around the gate cavity first, we applied our previous methodology allowing us to extract the bottom (μ_{bot}) and the entire sidewall region mobility (μ_T), without distinction from the corner. The mobility of the transverse region was found surprisingly to increase with deeper RD. To gain insight into the impact of the RD on this transverse section, a new extraction methodology is proposed to extract separately the gate corner (μ_{corner}) and sidewall (μ_{SW}) mobility. These extractions show that the corner mobility is found to be reduced compared to the sidewall one ($\mu_{corner} < \mu_{SW}$) evidencing the different weighting contributions over the transverse mobility. Moreover, these mobilities are found to be more degraded compared to the bottom one, highlighting the different contributions on the on-state resistance (R_{ON}). Indeed, the on-state resistance is lowered with the shallower RD due to the reduced sidewall resistance contribution (lower sidewall length) and despite the incremental contribution of the bottom resistance (larger effective gate length). However, the shallower RD shows an increase in the drain-source leakage current in reason of a lower gate electrostatic control. Technology Computer Aided Design (TCAD) simulations of the three RD morphologies are carried out to validate the experimental trends and the proposed methodology.

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I. INTRODUCTION

In high-power applications, gallium nitride (GaN) is a promising technology for reaching high breakdown fields and high mobilities. Especially, the MOS channel HEMT with a fully recessed MOS gate architecture is an attractive solution among normally-off HEMTs for power conversion systems. MOS-HEMTs are proposed to overcome the limits of the temperature dependency of the resistance R_{ON} , typically observed on pGaN gate architectures, as well as improve the gate robustness.^{1,2} However, if GaN MOS-HEMTs

are developed to reach low on-state resistance while maintaining normally off-state and higher reliability,³ they still suffer from degraded channel mobility due to gate-etching and Oxide/GaN interface poor quality ($\mu \leq 200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).⁴⁻⁷ Indeed, the inductively coupled plasma-reactive ion etching (ICP-RIE) process, used to create the gate cavity, is known to induce surface damage such as dangling bonds, roughness, impurities, defects, and amorphization on the surface.^{8,9} To reduce the damages, a few additional steps of atomic layer etching (ALE) have proven their efficiency at the bottom of the gate.^{2,10} Its principle is as follows: a precursor

reacts with surface atoms, then another reagent eliminates both surface atoms and precursors in another reaction, leading to small-step etching of the surface. This process provides better control and improved surface quality for GaN compared to ICP-RIE etching.

In this study, we compared three different RDs and their impacts on the MOS-HEMT DC performances. For this purpose, scanning transmission electron microscope (STEM), forward $I_D(V_G)$, and blocking $I_D(V_D)$ measurements are performed, as well as mobility extractions based on a new methodology. This methodology allows us to distinguish the contributions of the sidewall, corner, and bottom to the channel's resistance.^{10–13} Finally, TCAD simulations of the studied devices are compared to the experimental data, to validate the mobility extractions, giving additional insights into the gate morphology impact on the on-state performances.

II. PROCESS AND DEVICE TECHNOLOGY

The recessed MOS-HEMT devices are fabricated on 200 mm Si substrates as illustrated in Fig. 1. First, transition layers are used to overcome the lattice and thermal mismatch between GaN and Si.¹⁴ Then, a carbon-doped GaN is added to prevent the vertical breakdown followed by an unintentionally doped (NID) GaN layer grown by metal organic chemical vapor deposition (MOCVD).^{15–17} On top of the GaN an AlGaIn layer is deposited to form the heterojunction at the origin of the bi-dimensional electron gas (2DEG).^{18–20} Finally, a MOCVD SiN is used as a passivation layer.^{21–23} The recessed gate structure is fabricated by an AlGaIn/GaN dry etching (ICP-RIE), followed by cycles of ALE.^{9,24–27} In this work, the recessed depth (RD) is modulated by adjusting the dry etching time leading to three different RDs: 50, 150, and 350 nm. After GaN surface conditioning by wet cleaning, gate stack formation is carried out with the deposition of Al_2O_3 as a dielectric layer by atomic layer deposition (ALD) and then the gate metal, as reported in Fig. 2. Finally, fully recessed Ti/Al ohmic contacts annealed at low temperatures are used for source/drain contacts.

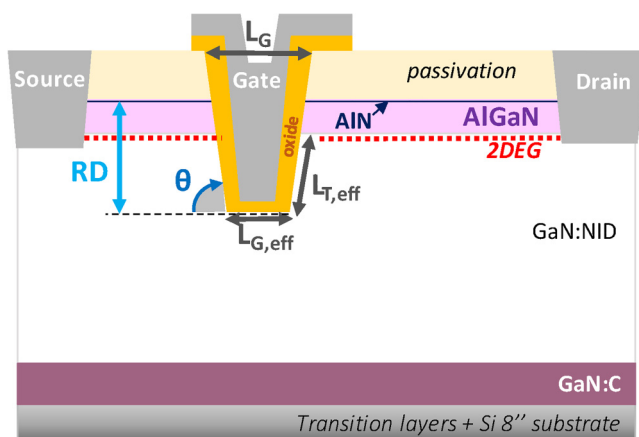


FIG. 1. Schematics of the fabricated GaN-on-Si MOS-HEMTs with fully recessed gate.

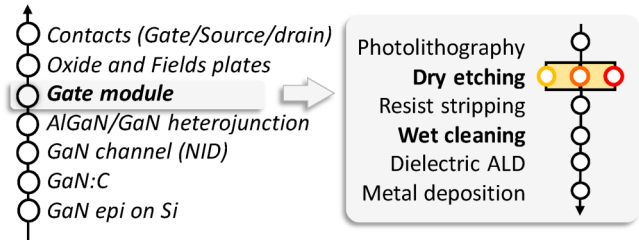


FIG. 2. Process flow with a focus on the gate etching and splits with 3RDs.

The corresponding STEM images of the fabricated devices are shown in Fig. 3 for three different gate lengths (L_G): 0.25, 0.5, and 1 μm , corresponding to the mask opening. By comparing the RDs of 50–150 nm and 350 nm, we see differences in the bottom region. At 50 and 150 nm, the bottom cavity is rather horizontal independently of L_G , whereas at 350 nm specifically for large L_G of 1 μm , a bowing effect appears.^{13,24} In addition, by decreasing the L_G dimension for the 350 nm case, a trench effect is observed: a change in the slope appears. This was reported in the literature and is likely due to the non-directional incident ions and the difficulty in accessing the deeper part of the cavity.²⁸ In Figs. 4 and 5, we report, respectively, the recess depth and sidewall angle as a function of the effective bottom gate length ($L_{G,eff}$) for the fabricated devices.

In Fig. 4, the RD and the effective bottom gate lengths ($L_{G,eff}$) are reported. These parameters of the devices are measured through ϵ Tilt SEM imaging and calibrate with the STEM images.¹² $L_{G,eff}$ is calculated according to the following equation:

$$L_{G,eff} = L_G - \frac{2 \cdot RD}{\tan(\theta)}. \quad (1)$$

First, the measured RD corresponds to the expected values (50, 150, and 350 nm). Second, $L_{G,eff}$ is lower than L_G value which is consistent with the fact that, the etching induces an angle of the sidewall. $L_{G,eff}$ is found to be smaller in the case of a deeper RD. Figure 5 illustrates this observation, by reporting the sidewall angle (SWA or θ) variation vs $L_{G,eff}$ for the different RDs. Small variability between the measured devices is observed and the SWA is found to be steeper with smaller L_G .

III. DEVICE ELECTRICAL CHARACTERISTICS

The devices are electrically characterized in forward and blocking modes to determine the effect of the RDs on the DC performances.

A. Forward mode

$I_D(V_G)$ measurements are carried out in the forward mode varying the gate voltage (V_G) from 0 to 6 V at a drain voltage (V_D) of 0.5 V at 25 $^\circ\text{C}$ in Fig. 6(a) and 150 $^\circ\text{C}$ in Fig. 6(b). Regardless of L_G and RD, no effect on the subthreshold regime (SS) and threshold voltage (V_{TH}) is observed, whereas $R_{ON} (=V_D/I_D)$ increases for

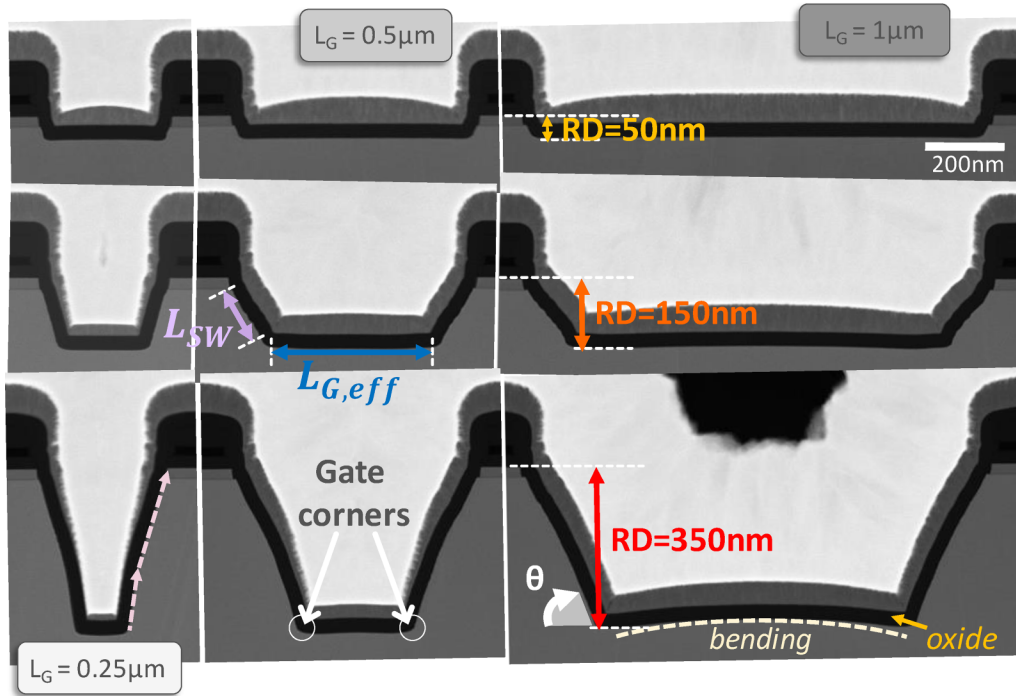


FIG. 3. TEMs images of splits varying the RD, respectively, 50, 150, and 350 nm and for three gate lengths: 0.25, 0.5, and 1 μm.

the larger L_G . A complex dependency between R_{ON} and RD at shallower RD (50 and 150 nm) is reported. Where first for L_G of 0.25 μm and 0.5 μm the I_D values are higher in the case of the RD of 50 nm, but that is no longer the case at $L_G = 1 μm$ where the

improved I_D value is obtained for the RD of 150 nm. However, a substantial signature is observed at the 350 nm RD. This effect can be related to differences on the bottom mobility and effective gate length defined by the RD. Similar trends are observed at 150 °C.

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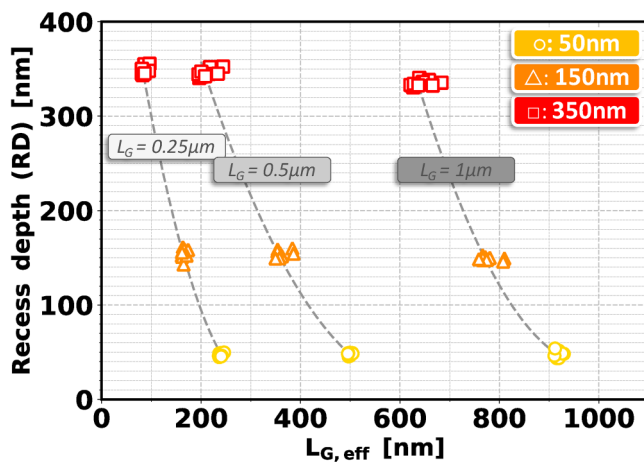


FIG. 4. Recess depth (RD) as a function of the effective bottom gate length for the three etching conditions (dimensions based on STEM images).

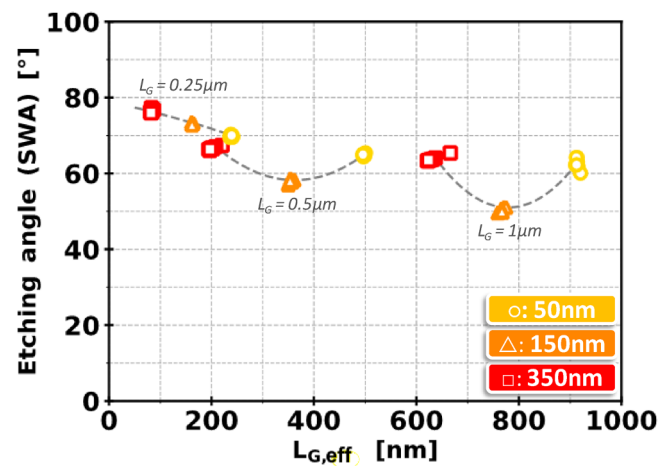


FIG. 5. $L_{G,eff}$ as a function of the sidewall angle (SWA) for the three recessed depths measured on several devices.

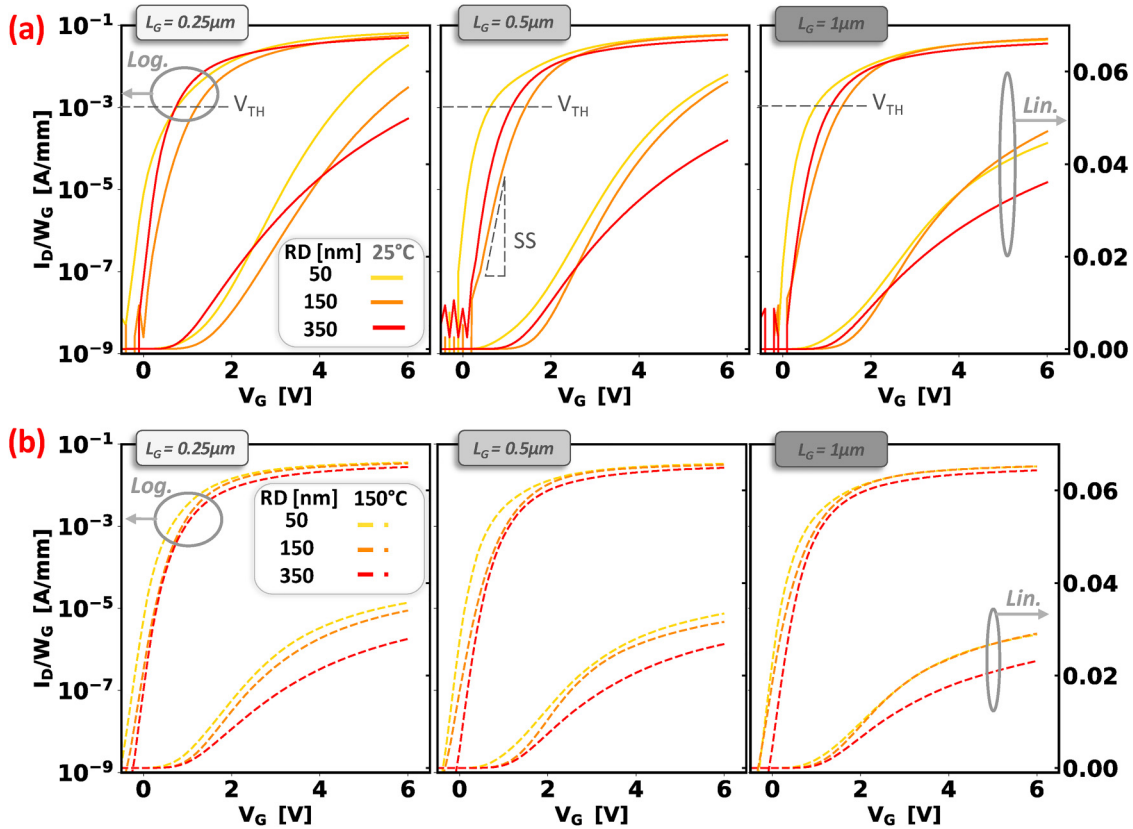


FIG. 6. Drain current vs gate voltage $I_D(V_G)$, for the three gate lengths (in log/lin scale); (a) at 25 °C and (b) at 150 °C.

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B. Blocking mode

Drain (I_D), source (I_S), and gate (I_G) leakage currents are also shown in Fig. 7 during the blocking mode for all the RDs at L_G of 0.5 μm . Measurements are carried out by varying the drain voltage (V_D) from 0 to 800 V at a gate voltage of $V_G = -4$ V. At 25 °C [Fig. 7(a)], no differentiable effect on the leakage currents is observed between the splits due to the very low values above the resolution limits. At 150 °C [Fig. 7(b)], for a deeper RD, the effective gate surface increases leading to a larger I_G . On the contrary, the lateral current leakage I_S decreases due to better electrostatic control of the gate in a deeper area and the presence of the gate. These differences among the RDs are observed starting at $V_D = 200$ V. However, the limiting mechanism of I_D at $V_D = 800$ V, not represented here is the leakage due to the bulk, whose degradation factor in temperature ($I_{B, 150^\circ\text{C}}/I_{B, 25^\circ\text{C}}$) is about 10.

IV. MOBILITY EXTRACTION

A. General methodology

In order to evaluate the impact of RD on the previous forward characteristics and gain insight on the dependency between R_{ON} , RD and effective gate length, a new extraction methodology is proposed.

As represented in Fig. 8, the MIS-HEMT resistance contributions are reported and the total resistance (R_{ON}) can be defined as

$$R_{ON} = 2R_c + R_{2DEG,S} + R_{2DEG,D} + R_{channel}, \quad (2)$$

where R_c , $R_{2DEG,S}$, $R_{2DEG,D}$, and $R_{channel}$ are, respectively, the contact, the 2DEG, and the channel resistance. R_c is determined by transmission line measurements (TLM) and is about 0.25 and 0.3 Ω mm, respectively, at 25 and 150 °C which represents the minor contribution to the total on-state resistance. R_{2DEG} is measured on gated Van der Pauw test structure and the corresponding electron mobility is extracted using the Split-CV methodology.²⁹ The R_{2DEG} values are found around 360 and 880 Ω/\square , respectively, at 25 and 150 °C, and the associated mobility is around 2140 and 870 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. The degradation factor ($R_{2DEG, 150^\circ\text{C}}/R_{2DEG, 25^\circ\text{C}}$) of 2.2 is related directly to the degradation of the mobility.

A methodology utilizing linear interpolations is suggested for assessing the impact of channel resistance ($R_{channel}$) on R_{ON} . More precisely, the objective is to differentiate the mobility degradation on the bottom and transverse regions of the gate cavity. The extractions are performed on several devices, for each one taking into account of its specifics dimensions in terms of $L_{G,eff}$. Figure 9

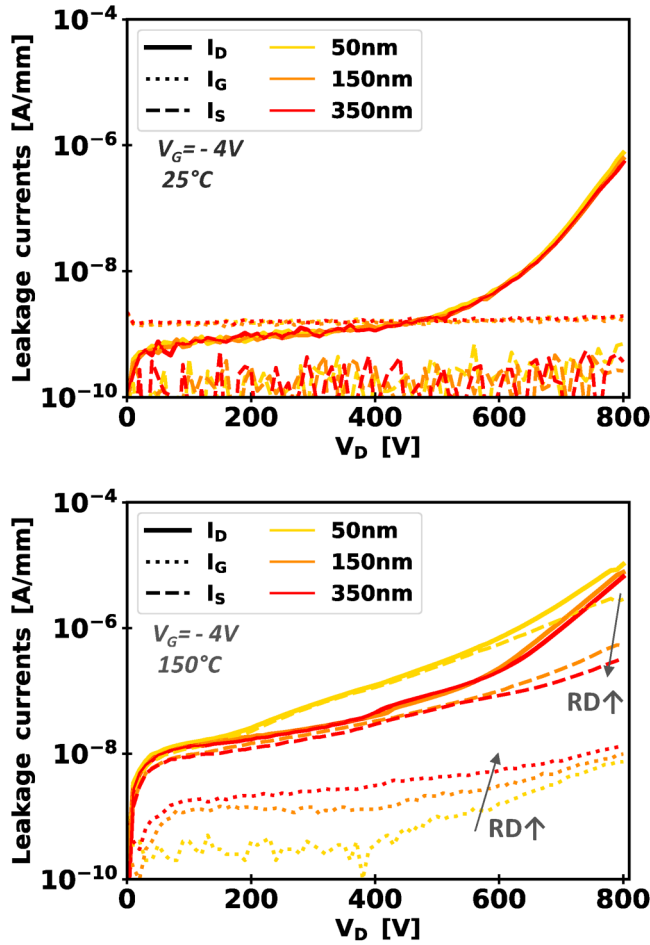


FIG. 7. Measured drain (I_D), gate (I_G), and source (I_S) leakage currents at 25 °C/150 °C in the blocking mode ($L_G = 0.5 \mu\text{m}$) for the 3 RD values (median).

illustrates this methodology. First, our previous methodology,¹⁰ recalled in Fig. 9(a), is applied, in order to determine the bottom mobility (μ_{bot}) and the transverse mobilities (μ_T). For that, R_{channel} is plotted as a function of $L_{G,\text{eff}}$ for several V_G values from 1 V to 6 V, according to Eq. (3). Here, two $R_{\text{channel}}(L_{G,\text{eff}})$ were considered: one using devices (specifically dedicated for such extractions) with large L_G (10–60 μm) giving more accuracy on the bottom extractions due to the negligible effect of the access; another one using the devices with smaller L_G (0.5–1 μm) to be more accurate on the effect of the access regions. Then, from the slope, the sheet bottom resistance ($r_{\square,\text{bot}}$) is extracted. The transverse resistance (R_T) is determined at the condition $L_{G,\text{eff}} = 0$ and depend on the transversal length (L_T).

$$R_{\text{channel}}(V_G) = R_T(V_G) + R_{\text{bottom}}(L_{G,\text{eff}}, V_G). \quad (3)$$

The bottom and transverse mobilities are calculated using electron density (N_S) from the capacitance measurements and the previous extractions of R_T and R_{bottom} .

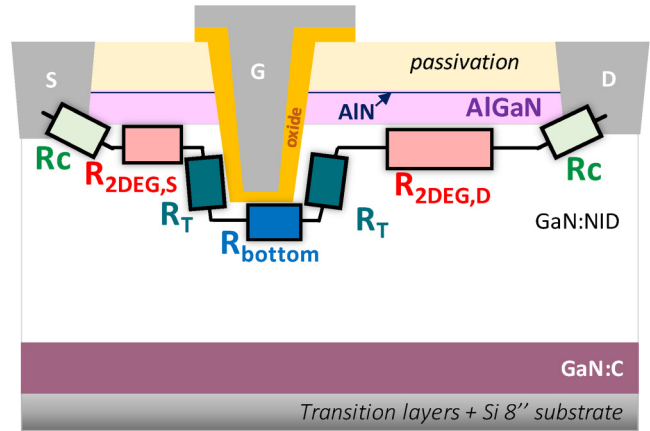


FIG. 8. Schematic of the overall resistance contributions on the on-state resistance.

Second, the new model presented in Fig. 9(b) and in Eq. (4), will be applied to estimate the degradation on the corner and sidewall regions, to give additional insight into the process degradation around the gate cavity,

$$R_{\text{channel}}(V_G) = R_{\text{SW}}(V_G) + R_{\text{corner}}(V_G) + R_{\text{bottom}}(V_G). \quad (4)$$

This method required several sidewall length variations (L_{SW}), accessible through the RD splits (50, 150, and 350 nm). The

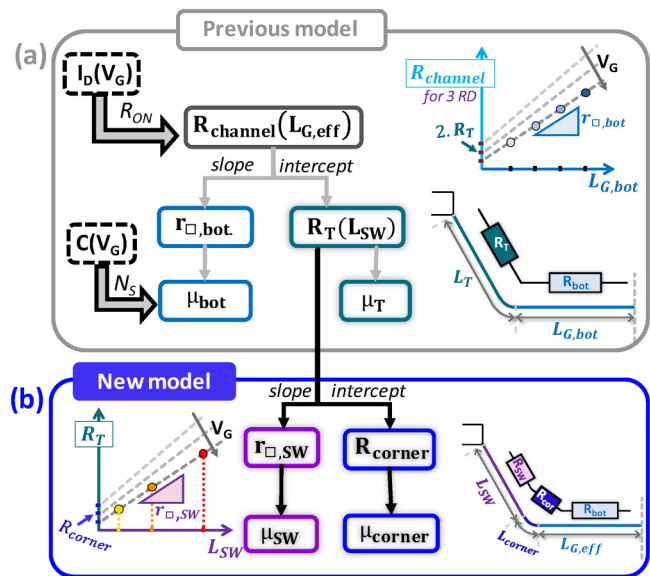


FIG. 9. General mobility extraction methodology to extract the three mobilities μ_{bot} (Fig. 13), μ_{SW} (Fig. 17), and μ_{corner} (Fig. 17), based on (a) the previous model from,¹⁰ (b) the proposed new model.

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previous R_T is plotted as a function of L_{SW} . The slope is related to the sidewall resistance (R_{SW}) and the intercept is related to the corner resistance (R_{corner}). Finally, μ_{SW} and μ_{corner} will be determined.

B. Extraction of the bottom mobility (μ_{bot})

To neglect the undesired effects of the morphology such as bowing effect, appearance of double slope on the sidewall of the gate cavity, transistors with large $L_{G,eff}$ from $10\ \mu\text{m}$ to $60\ \mu\text{m}$ are considered and characterized by $I_D(V_G)$ measurements for the 3 RDs at 25°C and 150°C from which R_{ON} can be calculated [$R_{ON}(V_G) = V_D / I_D(V_G)$]. $R_{channel}$ is then obtained from Eq. (2) by removing the access resistance form the total resistance [$R_{ON}(V_G) - (R_C + R_{2DEG,S} + R_{2DEG,D})$]. The corresponding $R_{channel}(V_G)$ is then plotted vs the $L_{G,eff}$ for various V_G values from 1 to 6 V as reported in Fig. 10.

The sheet bottom resistance [$r_{\square,bot}(V_G)$] is extracted from the slope of the $R_{channel}(L_{G,bot})$ characteristic as shown in Fig. 11, as a function of V_G . In addition, an inset of this resistance at $V_G = 6\ \text{V}$ is reported showing a clear evidence of a degradation of the sheet bottom resistance for the deeper RD (350 nm) while an optimum condition is found for 150 nm RD regardless of the V_G value.

Finally, μ_{bot} is determined from the previous $r_{\square,bot}(V_G)$ characteristics as a function of the electron density (N_S) according to Eq. (5), that is,

$$\mu_{bot} = \frac{1}{q \cdot N_S \cdot R_{channel}}, \quad (5)$$

where q is the electron charge. N_S is considered uniform around the gate channel (cavity) and is extracted by capacitance measurements $C(V_G)$ for the three RDs at 25 and 150°C as reported in Fig. 12. $C(V_G)$ characteristics are reported at both temperatures and no change is observed for the 3RDs in terms of electron density.

In Fig. 13 we report the extracted bottom mobility (μ_{bot}) as a function of N_S , obtained from Eq. (5), at both 25 and 150°C . For

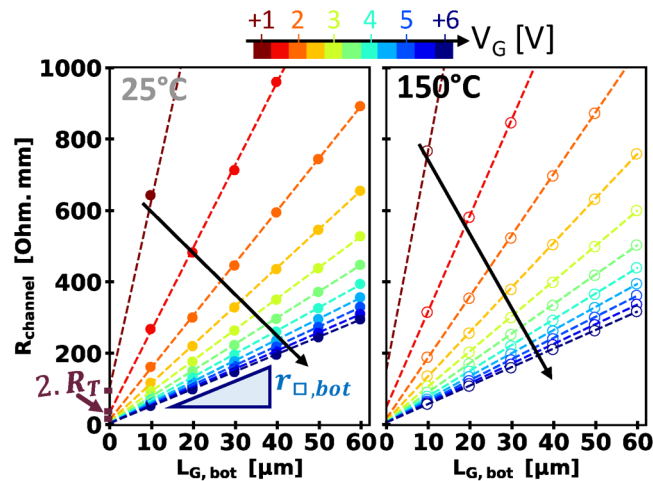


FIG. 10. Channel resistance (median) as a function of the bottom length for RD = 50 nm at $25^\circ\text{C}/150^\circ\text{C}$ for $V_G = 1-6\ \text{V}$ (with a 0.5 V step).

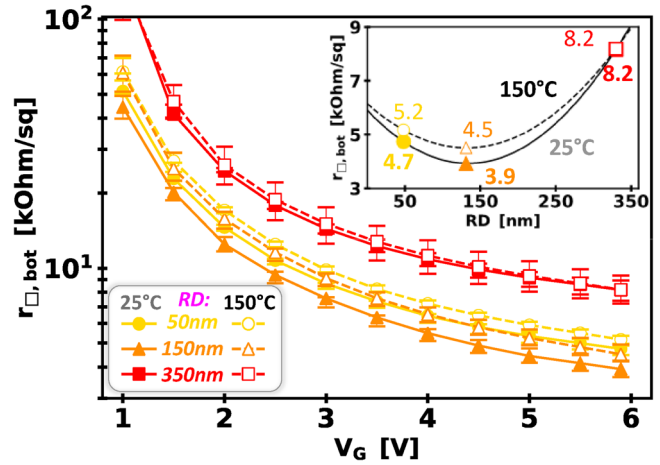


FIG. 11. Extraction of the sheet bottom channel resistance $r_{\square,bot}(V_G)$ for the 3RDs at $25^\circ\text{C}/150^\circ\text{C}$, inset: zoom on the $r_{\square,bot}$ values at 6 V for the two temperatures and the 3 RDs.

the shallow RDs (50/150 nm), the bottom mobility are found improved compared to the deepest one (350 nm) at both temperatures. This degradation can be related to either the proximity of the GaN:C layer enhancing the roughness mechanism, either to the degraded GaN bulk quality in deeper regions or the exposition etching time which is longer for the 350 nm RD. By comparing the μ_{bot} results at 25 and 150°C , it comes out that the temperature dependence (T°) is small ($<15\%$) for all the RDs. This slight variation with temperature can be explained by the effect of defects and not to the phonons.

C. Extraction of the transversal mobility (μ_T)

Based on previous work,¹⁰ $\mu_T(V_G)$ is calculated at 25 and 150°C from the intercept of the $R_{channel}(L_{G,bot})$ characteristics at

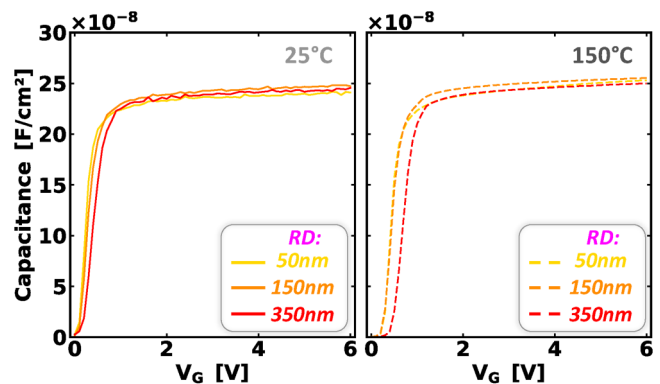


FIG. 12. $C(V_G)$ measurements performed on large devices at a frequency of 10 kHz.

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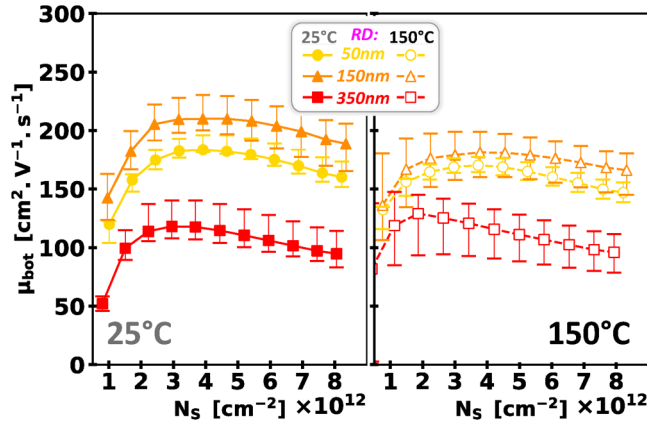


FIG. 13. Bottom channel mobility as a function of the electron density $\mu_{bot}(N_s)$ for the 3 RDs at 25 °C/150 °C.

$L_{G,bot} = 0$ for the overall RDs, according to Eq. (6), as reported as a function of N_s in Fig. 14,

$$\mu_T(V_G) = \frac{1}{q \cdot N_s(V_G) \cdot R_T(V_G)}. \quad (6)$$

For this purpose and in order to have a more precise extraction of μ_T , devices with smaller L_G (0.5, 1, and 2 μm) are considered contrary to the previous bottom mobility extraction (Fig. 10). Interestingly, we find that μ_T increases with deeper RD at both temperatures. Indeed, a value of 22, 81, and 93 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ at 25 °C and 26, 59, 77 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ at 150 °C is obtained at $V_G = 6 \text{ V}$ or equivalently $N_s \approx 8 \times 10^{12} \text{ cm}^{-2}$, respectively, for 50, 150, and 350 nm RD. The small temperature dependency of μ_T ($\approx 20\%$) is expected and is similar to the one found for μ_{bot} for all the RDs.

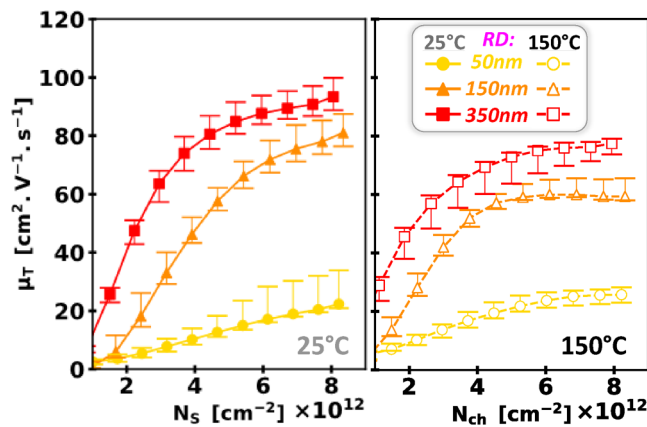


FIG. 14. Extraction of the transversal mobility (μ_T) as a function of the electron density N_s at 25 °C and 150 °C [from the intercept of the $R_{channel}(L_{G,eff})$].

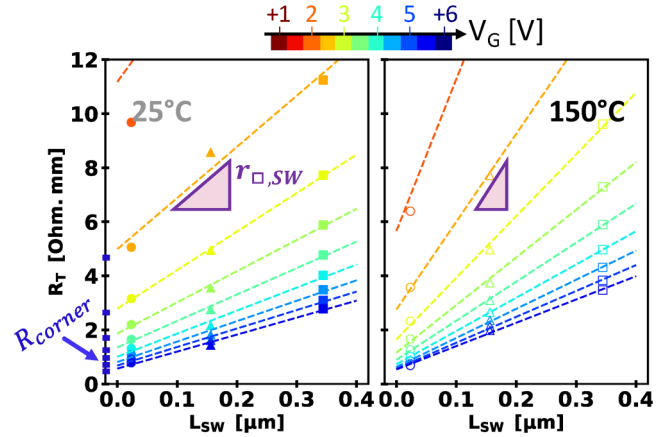


FIG. 15. Transversal resistance (R_T) (median) as a function of the sidewall lengths (L_{SW} taken from the STEM images for the 3RDs) at 25 °C/150 °C for $V_G = 1-6 \text{ V}$ (with 0.5 V step).

μ_{bot} is found to be higher than μ_T , likely due to the anisotropic ALE etching, and to the photolithography process, which induced more defects on the sidewall independently of the RD.

To explain the observed trend on μ_T , the only plausible assumption is to consider a non-uniform mobility along the trench cavity, specifically a difference between the sidewall and corner region. Indeed by assuming a much more degraded mobility in the corner region compared to the sidewall one, a more important weighting contribution of the corner region over the total transversal length ($L_T = L_{SW} + L_{corner}$) for shallower RD¹¹ could explain the observed mobility degradation. Indeed, during dry etching, due to the non-vertical trenches, degradation mechanisms in the corner regions are reported, supposedly due to energetic ions deflected from the sidewall surface to the corners.²⁸

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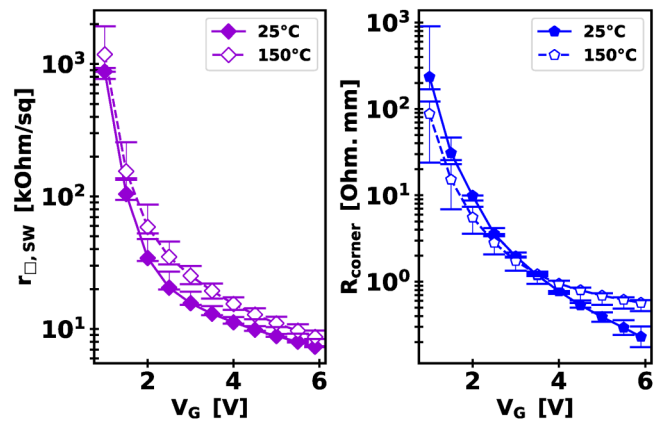


FIG. 16. Extraction from the slope and the intercept of the $R_T(L_{SW})$ at 25 °C/150 °C of (in Fig. 15); Left) the sheet sidewall channel resistance $r_{sq,sw}$ as a function of V_G ; and Right) corner resistance (R_{corner}), as a function of V_G .

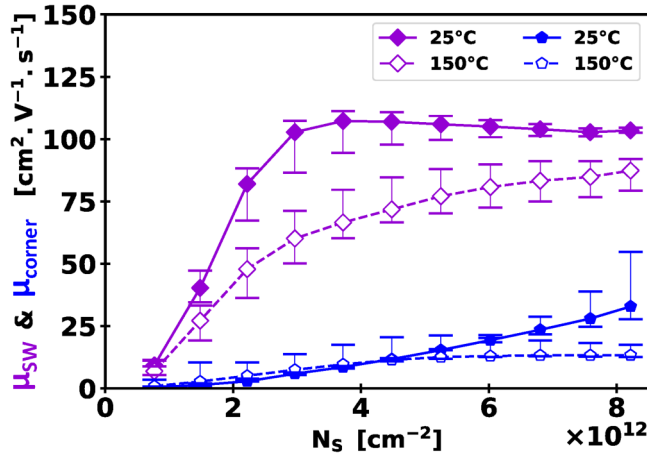


FIG. 17. Extracted mobility contributions for the sidewall (μ_{SW}) and corner (μ_{corner}) vs the electron density N_S at 25 °C/150 °C, for $L_{corner} = 10$ nm.

D. The mobility contributions around the gate: Decorrelation of the sidewall and corner mobility

In Fig. 15, the earlier extracted transversal resistance [$R_T(V_G)$] is reported as a function of the gate sidewall length (L_{SW}), obtained from the STEM images (Fig. 3), respectively, at 25 and 150 °C. The linear relationship between these two parameters, regardless of V_G and temperature, proves that the sidewall and corner mobility are identical between the different recess depths. $\mu_{corner}(V_G)$ and $\mu_{SW}(V_G)$ are then calculated from the corresponding sheet sidewall resistance [$r_{\square,SW}(V_G)$] and corner resistance [$R_{corner}(V_G)$]. $r_{\square,SW}(V_G)$ and $R_{corner}(V_G)$ are extracted, respectively, from the slope and intercept of $R_T(V_G, L_{SW})$ characteristics at 25 and 150 °C, as reported in Fig. 16.

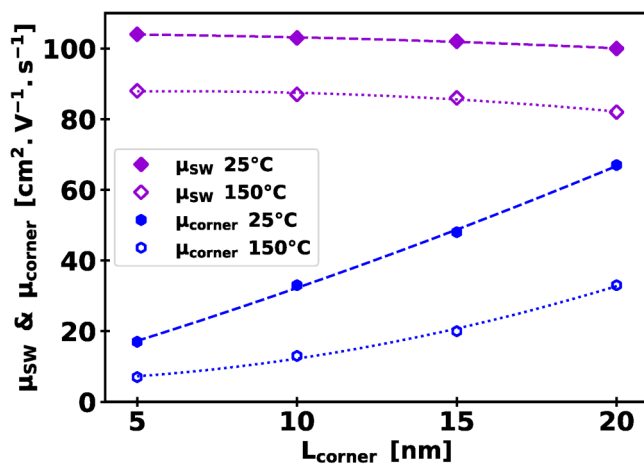


FIG. 18. Sensibility of L_{corner} on μ_{SW} and μ_{corner} .

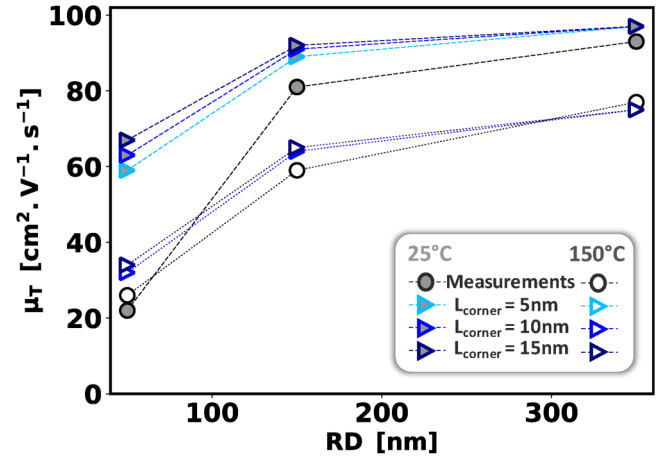


FIG. 19. Comparison of the extracted mobilities μ_T (measurements) to the calculated $\mu_{T,cal}$ from the values (at $V_G = 6$ V) of μ_{SW} and μ_{corner} (Figs. 14 and 18).

Similarly to the bottom mobility, μ_{SW} and μ_{corner} are evaluated using Eqs. (6) and (7) that are, respectively,

$$\mu_{SW} = \frac{1}{q \cdot N_S \cdot r_{\square,SW}}, \quad (7)$$

$$\mu_{corner} = \frac{L_{corner}}{q \cdot N_S \cdot R_{corner}}, \quad (8)$$

where L_{corner} is the corner length estimated from the STEM images (≈ 10 nm in Fig. 3). μ_{SW} and μ_{corner} are shown as a function of N_S at 25 and 150 °C in Fig. 17. μ_{corner} is found to be degraded compared to μ_{SW} at both temperatures. At high temperatures and $N_S = 8.2 \times 10^{12} \text{ cm}^{-2}$, both μ_{SW} and μ_{corner} are degraded by $\sim 15\%$ and 60% , respectively.

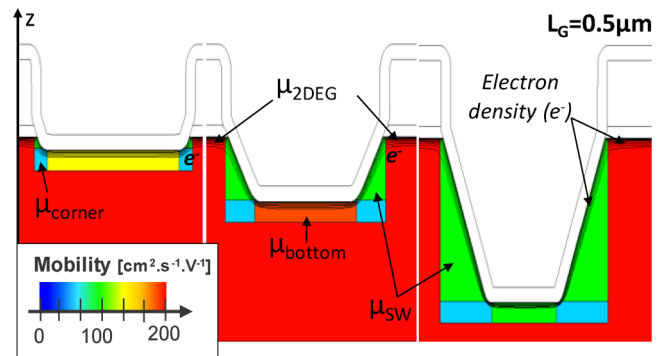


FIG. 20. TCAD simulated structures (RD, $L_{G,eff}$ and SWA) according to STEM images (Fig. 3) and representation of the mobility regions (bottom, sidewall, and corner) and electron density.

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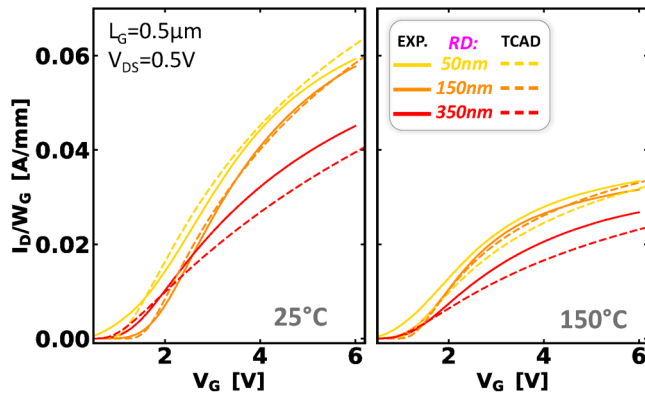


FIG. 21. Simulated $I_D(V_G)$ for the 3RDs for $L_G = 0.5 \mu\text{m}$, and comparison with the experimental data (median) at 25 °C and 150 °C.

As illustrated in Fig. 18, the extraction of μ_{corner} and μ_{SW} is reported at $V_G = 6 \text{ V}$ as a function of L_{corner} . Indeed, the extracted mobility values are impacted by the uncertainty around the L_{corner} value. Specifically μ_{corner} is found to be highly affected and increases with larger L_{corner} . On the contrary, μ_{SW} is found to be nearly constant, and therefore its extraction is unaffected by this uncertainty. A 20 nm corner length seems maximum considering the previous TEM image (Fig. 3) and Fig. 18, while values around 10 nm look more relevant for extraction. Finally, we can describe these mobilities with the transverse mobility, by considering their simple resistance dependency ($R_T = R_{\text{SW}} + R_{\text{corner}}$), that leads to the following expression:

$$\mu_{T,\text{cal}} = \frac{(L_{\text{corner}} + L_{\text{SW}}) \times (\mu_{\text{corner}} \times \mu_{\text{SW}})}{(L_{\text{SW}} \times \mu_{\text{corner}}) + (L_{\text{corner}} \times \mu_{\text{SW}})}. \quad (9)$$

In Fig. 19, the calculated $\mu_{T,\text{cal}}$ values [Eq. (9)], using the extraction of the μ_{SW} and μ_{corner} , are compared to the ones extracted experimentally with the previous methodology. The value of $\mu_{T,\text{cal}}$ is found to followed a similar trend that of μ_T which

confirmed the importance of the corner in the interpretation of the degradation mechanism around the gate cavity.

V. TCAD SIMULATIONS

Finally, TCAD simulations are carried out in order to validate the mobility extractions and to confirm the consequent experimental trend on the DC performances. The simulated gate morphologies for the three RD values for a L_G of $0.5 \mu\text{m}$ are reproduced to account for the experimental STEM observations using the *sprocess* module of Synopsys, and are illustrated in Fig. 20. Electrical simulations were performed with Synopsys S-Device module. The spontaneous and piezoelectric polarization into the AlGaIn, AlN and GaN are taking into account by considering two interface polarization charges at the AlGaIn/AlN and AlN/GaN interfaces. To validate the mobility extractions at 25 and 150 °C (Figs. 13 and 17), their values have been directly used as input for the $I_D(V_G)$ simulations. No dependency with temperature and saturation velocity is considered since these experimental values (used as input in TCAD) already take these effects into account. The mobility values at $V_G = 6 \text{ V}$ allows to predict and validate the extraction and the experimental trend observed specifically at strong inversion. In Fig. 21, simulations (dashed lines) are compared to the experimental $I_D(V_G)$ measurements (solid lines) for the three RDs. The results show that the $I_D(V_G)$ curves are well reproduced and close to the experimental data at both temperatures.

We have also mentioned, the effect of the RD on the leakage currents during the blocking mode (Fig. 7), specifically the rise of the lateral leakage current (I_s) with shallower RD. This can be explained by the different distributions of the electrostatic potential around the gate cavity between the different RDs. The simulated electrostatic potential distributions at $V_G = -4 \text{ V}$ and $V_D = 650 \text{ V}$, are reported in Fig. 22 for the three RDs. The electrostatic potential of the gate cavity extends to the deeper GaN-NID region for larger recess depths. Moreover the presence itself of an enlarged gate cavity prevents from the rising of the lateral leakage current. However, the increase of sidewall length and the appearance of a sharper angle with deeper RD, leading to an increase of local electric field, increases the gate leakage current. However, the sharper

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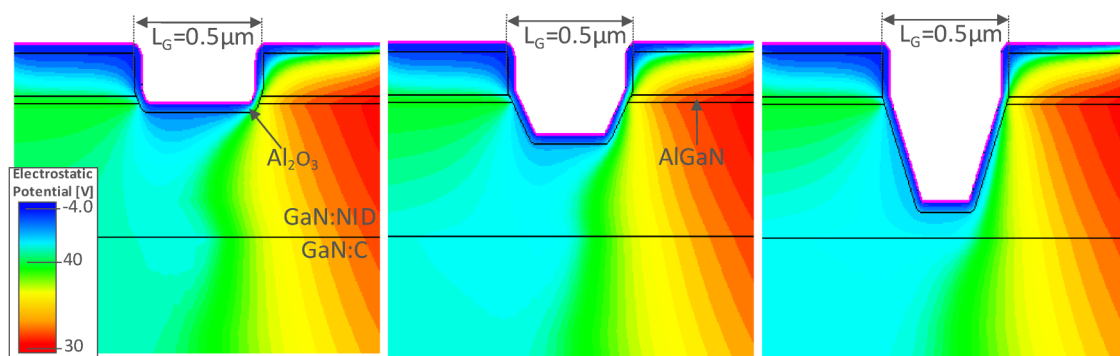


FIG. 22. Simulated electrostatic potential distribution around the recessed gate of the device, at $V_G = -4 \text{ V}$, and $V_D = 650 \text{ V}$.

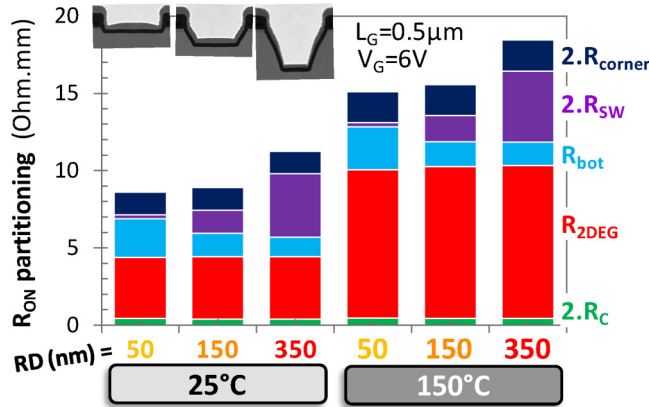


FIG. 23. Determination of the five contributions of the R_{ON} ($2R_c + R_{2DEG} + R_{bottom} + 2R_{SW} + 2R_{corner}$) for a L_G of $0.5\mu m$, based on extracted resistances (Figs. 10, 14, and 15) and effective lengths (L_{corner} , L_{SW} , $L_{G,bot}$).

angle and surface damage inside the trenches would lead to greater gate leakage current.

VI. R_{ON} OPTIMIZATION

In Fig. 23, the R_{ON} partitioning [Eqs. (2) and (4)] is summarized for the three RDs at 25 and 150 °C for a L_G of $0.5\mu m$. R_{ON} is found to be lowered with shallower RDs due to a reduced R_{SW} contribution attributed to a shorter L_{SW} and despite the rising contribution of R_{bottom} in reason of a larger $L_{G,eff}$. The dependency between R_{ON} and RD is not simply a geometrical relationship (L_{SW} , $L_{G,eff}$), but require to account for the experimental differences in terms of mobility around the cavity. Indeed, the R_{ON} difference

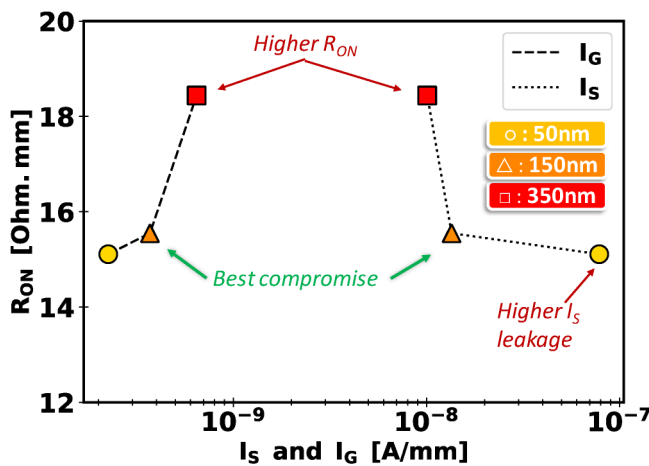


FIG. 24. R_{ON} at 6 V vs I_S and I_G leakage current values at 150 °C, extracted at $V_D = 650$ V.

between R_{DS} is explained by a reduction of the sidewall resistance for shorter RDs, which is purely geometrical (L_{SW}) since μ_{SW} and μ_{corner} are assumed independent of the RD, and above a nonlinear contribution of the R_{bottom} . The improved μ_{bottom} is found for the RD of 150 nm. Concerning the temperature dependency, the $R_{channel}$ is weakly impacted (increase by a factor 1.2) due to the low degradation observed in the electron mobility compared to the access resistance (R_{2DEG}) where a factor above 2 is reported. As reported, in Fig. 24, by considering both results in forward (R_{ON}) and in blocking mode (I_G , I_S) and comparing the three RDs for a given L_G of $0.5\mu m$, an optimum is found at 150 nm recess depth. Indeed, the RD of 150 nm shows comparable R_{ON} and I_G with the 50 nm RD and the comparable I_S with 350 nm RD.

VII. CONCLUSIONS

In this study, we evaluated the DC performances of the MOS-HEMT in terms of R_{ON} , channel mobility, and leakage currents (blocking mode), for three RDs values: 50, 150, and 350 nm, at 25 and 150 °C. We report that R_{ON} is the result of different resistance contributions: R_{2DEG} and R_c corresponding to the access regions and which are independent of the etching process and $R_{channel}$ which is strongly impacted. To estimate the effect of the RD and determine the regions around the gate cavity subject to the highest mobility degradation, a methodology based on STEM images, $I_D(V_G)$, and $C(V_G)$ measurements has been proposed. A stronger degradation for the transverse region of the gate compared to the bottom ($\mu_T < \mu_{bot}$), as well as a dependence with RD of the transverse mobility are demonstrated. μ_T is found more degraded for the shallowest RD. To take account of this observation, the assumption of a weighting contribution of μ_{corner} with respect to μ_{SW} ($\mu_{corner} < \mu_{SW}$) was introduced and validated by TCAD $I_D(V_G)$ simulations. Finally, R_{ON} is improved for shallower RDs (50 and 150 nm) due to a reduced impact of R_{SW} (lower L_{SW}), and despite the larger contribution of R_{bottom} (increase in $L_{G,eff}$ and μ_{bot} , $50\text{ nm} < \mu_{bot, 150\text{ nm}}$), emphasizing the importance of considering all gate regions (sidewall, corner, and bottom) for the R_{ON} optimization. To conclude, with regard to blocking characteristics at 150 °C, improved electrostatic control of the gate (lower I_S leakage) is reported for the deeper RD, highlighting an optimum in terms of R_{ON}/I_S for the 150 nm RD value.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

C. Piotrowicz: Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **B. Mohamad:** Methodology (equal); Supervision (equal); Writing – review &

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editing (equal). **N. Malbert:** Methodology (supporting); Supervision (equal); Writing – review & editing (equal). **S. Bécu:** Methodology (supporting); Writing – review & editing (supporting). **S. Ruel:** Investigation (supporting). **C. Le Royer:** Methodology (supporting); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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