Associative Memory Demonstrated By a Simple Design of Spiking Neural Network with an Ionic Synaptic Transistor

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***Abstract*—Nanoscale ionic synaptic transistors (SynTs) have been actively investigated for neuromorphic computing applications owing to their excellent overall performance with high resistive switching precision, ultralow operation power, and linear conductance modulation. In this work, we proposed an all-analog neural network circuit with SynT as an artificial synapse to simulate the associative memory, exemplified by Pavlov's experiments.**

Keywords—neuromorphic computing, synaptic transistor, Spiking Neural Network (SNN), Leaky Integrate and Fire (LIF), Artificial Neural Networks (ANN), associative memory.

I. INTRODUCTION

Artificial synaptic devices are employed to constitute novel neuromorphic computing systems that can perform data-intensive calculation tasks. Recently, there has been a temptation to look for approaches to build neural networks that are able to emulate neuromorphic and cognitive properties of the brain, so-called spiking neuron networks (SNNs). The SNN employs the concepts of spiking events: the information is encoded in the timing or frequency of the spikes. One of the important biorealistic learning mechanisms demonstrated with SNNs is associative memory, which has been biologically verified by Pavlov's dog experiment [1]. There are four steps involved in this experiment:

(I), (II) Salivation of the dog's mouth is set by the sight of food (unconditioned stimulus - US), and the dog does not salivate upon hearing the sound of the bell (neutral stimulus – NS).

(III) Then, during the conditioning period in which the sight of food is accompanied by a bell sound over a certain period, the dog learns gradually to associate/link the sound to the food.

(IV) After conditioning, the bell sound alone can trigger its salivation (conditioned stimulus – CS) without the intervention of vision.

This behavior has been intensively reproduced in artificial neural networks as a first important step in obtaining functionalities that resemble those of the human brain [2]–[5]. Pavlov's dog experiment can be modeled by a neural network circuit composed of two synapses and a neuron (Fig. 1 top panel). Here, the sight of food (US) and the sound of a bell (CS or NS), outputs of previous independent neurons, are modeled by electrical pulses sent to synapses 1 and 2 respectively. If the circuit is subjected to both input US and NS events, then after a sufficient number of occurrences, the output neuron starts to "salivate" upon the reception of CS only.

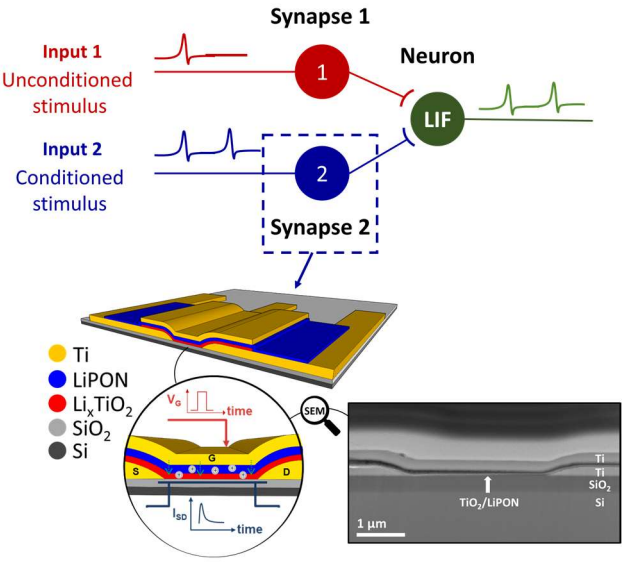

Fig. 1: Simple neural network model for Pavlov's dog experiment, in which the "Synapse 2" is modeled by a Li_xTiO_2-based electrochemical synaptic transistor. Bottom right inset illustrates the SEM cross-section view of the elaborated device. Adapted from REF [7].

To build artificial neural circuits, standard CMOS technology faces several difficulties (e.g. insufficient scalability and low power efficiency [6], [7]). To overcome such challenges, memristors are considered as promising devices to emulate synapses, which can be integrated to develop fully functional electronic circuits [6]. Emulating the Pavlov's Dog behavior has been already reported in literature. It was demonstrated mainly with two-terminal memristors: the proposed complete circuits (synapses + neuron) involve op-amps [8], computing devices [9] or microcontrollers [2]. Such Pavlovian conditioning was also demonstrated with three-terminal synaptic transistors, which allow several advantages over two-terminal memristors (eg the shape of the pulses applied during the write step can be chosen quite independently from the read pulses). However, the proposed circuits also include computer interface [3] or op-amps [10], which adds complexity to the circuit system.

This is why our main objective here is to propose a demonstration of the associative memory behavior by using a developed 3-terminal synaptic transistor, connected to a simple all-analog circuit (involving neither op-amps, nor

computer interface). Specifically, we simulate the change connection strength in one of the synapses (synapse 2 in Fig. 1) with a developed Li_xTiO_2-based synaptic transistor [11], denoted SynT (whose memristive behavior has been studied using pulses of different amplitudes), and propose the design and the simulation of a simple *all-analog* spiking neural network electronic circuit, which reproduces very well the development of associative memory via training.

II. NEURAL NETWORK CIRCUIT

A. Two synapses and one LIF Neuron model

The neural network model in the Fig. 1 is represented with a circuit design as shown in Fig. 2. In the proposed circuit, the neural signals of "food sight" (connected to synapse 1 – red box) and "bell sound" (connected to synapse 2 – blue box) are simulated by voltage sources which provide voltage pulses. The two synapses are connected to the LIF neuron circuit, through a "current mirrors" interface stage (grey box, components not shown), which allows to sum up (and amplify: gain K ~1000) the currents which flow through the two synapses.

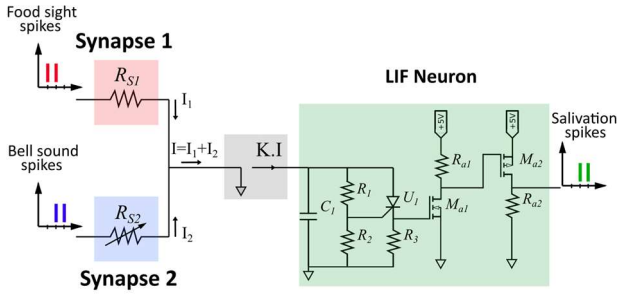

Fig. 2: Circuit with two synapses (a resistor in red and a variable resistor in blue), and the LIF neuron circuit in green.

Toward the electronic implementation of the artificial neural network, we employ a LIF neuron model designed with analog components reported in [12]. The neuron model allows us to simulate the "leaky integrate-and-fire" and "axon signal transmission" functions which is analogous to that of a biological neuron.

In principle, the conductance of synapse 1 will be designed to be high enough, so that the current (I_1) stimulated by a "food sight" signal can trigger alone the LIF neuron to fire a "salivation" spike. On the other hand, the current signal (I_2) from "bell sound" alone cannot result in a spike from the neuron output due to the initial too low conductance of synapse 2. Nevertheless, this conductance may gradually be increased by training, using the component described below.

B. Li_xTiO_2-based electrochemical synaptic transistor

To achieve the aforementioned goal, an electrochemical transistor models the varying weight of synapse 2 with its synaptic plasticity characteristics. The bottom panel of the Fig. 1 shows an illustrative view and a cross-section view of the reported micro-fabricated SynT device [11]. The transistor is a vertical stack consisting of an ultra-thin Li_xTiO_2 channel (10nm thick), a solid-state electrolyte (gate dielectric) made of amorphous LiPON, and a top gate made of Ti. The all-solid-state structure of our SynT device [11] allows better wafer scale integration possibilities compared to other types of three-terminal synaptic devices which include liquid or solid polymer gate dielectrics [10], [13], [14].

The inset of Fig. 1 shows a schematic cross-section of the transistor. Square-shaped voltage pulses applied to the gate mimic the biological impulses of the pre-synaptic neurons. The change conductance under Li^+ intercalation is captured by electrically sampling the current flowing between the drain and source electrodes (I_{DS}).

The effect of Li^+ intercalation on channel conductance was verified by an IV sweep.

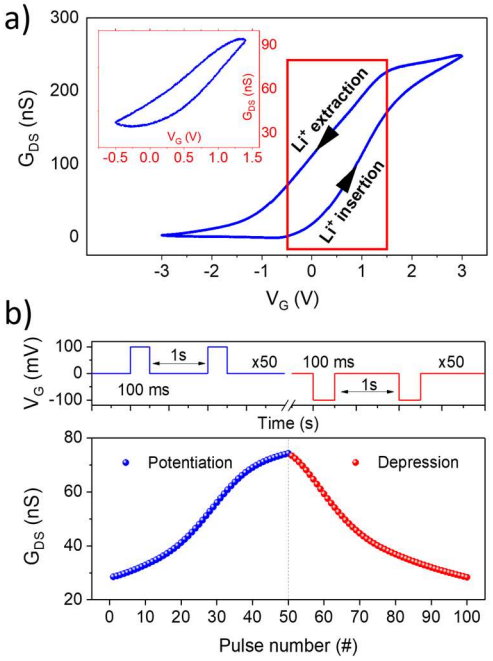

Fig. 3: a) Charge transfer curve (channel conductance G_{DS} as a function of gate voltage V_G) with a gate sweep of 50 $mV.s^{-1}$ in the potential range [-3 V, 3 V] (inset: Focused working window of [-0.5 V, 1.5 V]). b) Long-term plasticity demonstration with 100 states of potentiation and depression programmed by ±100 mV, 0.1 s pulses.

Fig. 3.a depicts the evolution of the channel conductance G_{DS}, by application of a bidirectional sweeping gate voltage from -3.0 V to 3.0 V. Initially, G_{DS} was very low ($G_{DS} \leq 20$nS at $V_G = 0$ V). Then G_{DS} increased up to a 100 times higher value, reaching 250 nS, due to the intercalation of Li^+ ions into the TiO_2 channel. For the backward sweep (Li^+ extraction), G_{DS} decreased gradually back to its low conductance state. The [-0.5 V, 1.5 V] potential window (inset of Fig. 3.a) was selected to develop the SynTs and avoid saturation change at the ends of the sweep. As shown in Fig. 3.b, emulation of neuromorphic behaviors, such as long-term potentiation (LTP) and long-term depression (LTD) was achieved by alternatively programming the SynT with 50 identical pulses. The conductance states were modified in an analog way from a low conductance level of 30 nS to a high conductance level of almost 75 nS, which corresponds to a ~1 nS increase from one state to the next. These functionalities are simulated with a SPICE compact model, which will be described in the following section.

C. A SPICE model of SynT

We model the SynT behavior with a combination of three components (Fig. 4.a): a small capacitor (C_{SynT} = 1 nF) can be charged up by the incoming spikes, to simulate the behavior of SynT gate stack. This capacitance is estimated based on the measured capacitance of Pt/LiPON/Pt and Pt/TiO_2/LiPON/Pt structures [15], [16], taking into account the active area and

the thickness of the transistor's gate stack. Besides, A resistor with a high value (R_{SynT} = 10 GΩ) is used to mimic the high leakage resistance of the gate stack. Finally, we use a transistor U in which the current I_{DS} can be controlled by the gate voltage V_G to model the conductance evolution: from the experimental measurement of the channel conductance as a function of gate voltage (Fig. 4.b), we fit the I_{DS} of the component U with a linear function as follows:

$$I_{DS} = G_{DS} \times V_{DS} \quad (1)$$

with $$G_{DS} = G_{Low} + ((G_{High} - G_{Low}))/1.5V \times V_G \quad (2)$$

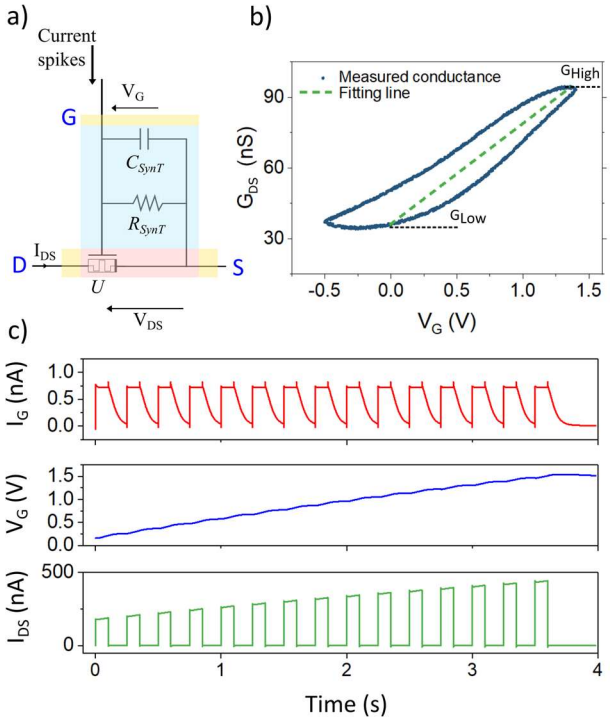

Fig. 4: a) Synaptic transistor compact model. b) Implementing the measured conductance as a function of the gate voltage. c) Simulation of the SynT response (Top) The writing current pulses. (Middle) The increase of gate potential (simulated by the potential across C_{SynT}). (Bottom) The channel current I_{DS} of SynT.

The response of the synaptic transistor model to a train of current pulses is simulated in Fig. 4.c. Current pulses (I_G) of around 0.7 nA and 100 ms duration are injected into the gate (equivalent to 70 pC charge per pulse: this is approximately equivalent to the actual charge needed to switch experimentally between adjacent states of the electrochemical synaptic transistors). This leads to a gradual increase of the gate potential V_G (blue curve), thus to an increase of the G_{DS} conductance, and to an increasing magnitude of the current spikes I_{DS} (green curve) flowing across the SynT channel. Such evolution of G_{DS} will contribute to the associative memory behavior that will be simulated in the next step.

III. Simulation Results

Fig. 5 illustrates the neural circuit design used for the demonstration of the associative memory. For the fixed weight value of Synapse 1, we used a resistor (10 MΩ). On the other hand, the SynT, with its synaptic plasticity, is

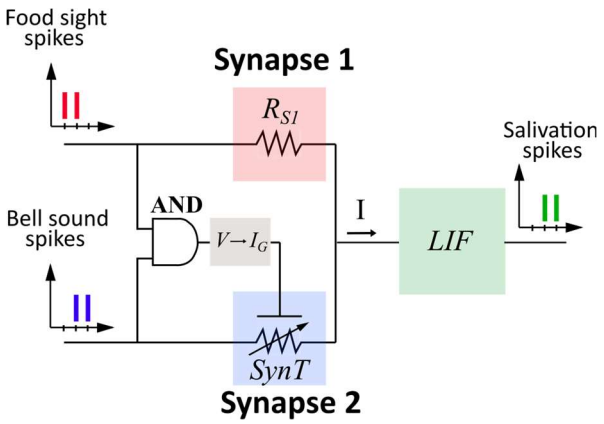

Fig. 5: Schematic of the circuit used for the simulation of the associative memory development.

adapted to become synapse 2. Both sources (V_{FOOD} and V_{BELL}) are connected to an AND logic component: when they arrive simultaneously to the AND component, the latter delivers a 5V output voltage, which is converted to a current (through an interface circuit composed of a resistor to control the gate current and a Mosfet current mirror, not shown). This current is injected into the gate of the SynT (Synapse 2) which allows the SynT conductance to increase gradually (during the conditioning period). With the components described above we reproduced Pavlov's dog experiment with our neural network circuit: the results are illustrated in Fig. 6.

In the first step, applying "food sight" stimuli triggers the "salivation", whereas the "bell sound" stimuli do not induce any effect (step II). Electronically speaking, the output neuron fires because the currents through synapse 1 are high enough to get the neuron potential over the threshold (due to the resistance R_{S1} = 10 MΩ, which corresponds to a 100 nS conductance) while the current pulses sent to the neuron via Synapse 2 are too low (the initial conductance of the SynT is only 30 nS).

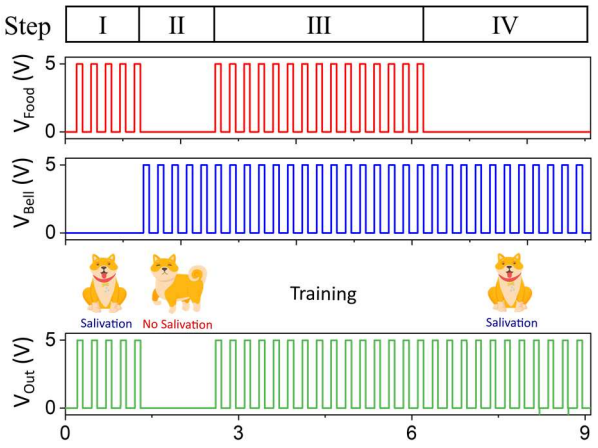

Fig. 6: Simulation of the development of the associative memory, with a neural network circuit composed of SynT as a synaptic element.

In the training phase (step III), stimulus voltages are sent simultaneously to both synapses. As a direct result of "food sight," the "salivation" neuron fires correspondingly. At the same time, the overlap between two sources of stimulus pulses facilitates the potentiation of the synaptic transistor via a train

of current pulses. Thus, conductance of synapse 2 increases gradually: an association between "food sight" and "bell sound" signals develops progressively.

Finally, in step IV, a train of signals of "bell sound" only is applied to the neuron: salivation still occurs, thereby proving clearly the associative learning ability of the circuit.

IV. Conclusions

In this work, we demonstrated the development of associative memory using the simulation of an all-analog neural network circuit, composed of a resistor, an electrochemical synaptic transistor and a leaky integrate-and-fire (LIF) neuron. The training phase of Pavlov's dog experiment under the synchronous stimuli from "food sight" and "bell sound" was simulated by the potentiation process of the SynT's conductance. After the training period, the circuit was successfully trained to react to "bell sound" stimuli by firing potential spikes out of the neuron.

Such a simple neural network works in a hardware way without any interface with a software control machine. This interesting feature may give insights towards future embedded networks, which could be beneficial to real-world applications such as healthcare, or other robotic sensing and reasoning by linking the realistic stimuli detected from sensory systems.

References

[1] R. E. Clark, "The classical origins of Pavlov's conditioning," *Integr. psych. behav.*, vol. 39, no. 4, pp. 279–294, Oct. 2004, doi: 10.1007/BF02734167.

[2] Y. V. Pershin and M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks," *Neural Networks*, vol. 23, no. 7, pp. 881–886, Sep. 2010, doi: 10.1016/j.neunet.2010.05.001.

[3] O. Bichler *et al.*, "Pavlov's Dog Associative Learning Demonstrated on Synaptic-Like Organic Transistors," *Neural Computation*, vol. 25, no. 2, pp. 549–566, Feb. 2013, doi: 10.1162/NECO_a_00377.

[4] K. Moon *et al.*, "Hardware implementation of associative memory characteristics with analogue-type resistive-switching device," *Nanotechnology*, vol. 25, no. 49, p. 495204, Dec. 2014, doi: 10.1088/0957-4484/25/49/495204.

[5] S. G. Hu *et al.*, "Synaptic long-term potentiation realized in Pavlov's dog model based on a NiO_x-based memristor," *Journal of Applied Physics*, vol. 116, no. 21, p. 214502, Dec. 2014, doi: 10.1063/1.4902515.

[6] D. V. Christensen *et al.*, "2022 roadmap on neuromorphic computing and engineering," *Neuromorph. Comput. Eng.*, vol. 2, no. 2, p. 022501, Jun. 2022, doi: 10.1088/2634-4386/ac4a83.

[7] S. D. Ha and S. Ramanathan, "Adaptive oxide electronics: A review," *Journal of Applied Physics*, vol. 110, no. 7, Art. no. 7, Oct. 2011, doi: 10.1063/1.3640806.

[8] M. Ziegler *et al.*, "An Electronic Version of Pavlov's Dog," *Adv. Funct. Mater.*, vol. 22, no. 13, pp. 2744–2749, Jul. 2012, doi: 10.1002/adfm.201200244.

[9] C. Sun, C. Wang, and C. Xu, "A full-function memristive pavlov associative memory circuit with inter-stimulus interval effect," *Neurocomputing*, vol. 506, pp. 68–83, Sep. 2022, doi: 10.1016/j.neucom.2022.07.044.

[10] S. D. Ha, J. Shi, Y. Meroz, L. Mahadevan, and S. Ramanathan, "Neuromimetic Circuits with Synaptic Devices Based on Strongly Correlated Electron Systems," *Phys. Rev. Applied*, vol. 2, no. 6, p. 064003, Dec. 2014, doi: 10.1103/PhysRevApplied.2.064003.

[11] N. Nguyen *et al.*, "An Ultralow Power $Li_x TiO_2$-Based Synaptic Transistor for Scalable Neuromorphic Computing," *Adv Elect Materials*, p. 2200607, Sep. 2022, doi: 10.1002/aelm.202200607.

[12] M. J. Rozenberg, O. Schneegans, and P. Stoliar, "An ultra-compact leaky-integrate-and-fire model for building spiking neural networks," *Sci Rep*, vol. 9, no. 1, p. 11123, Dec. 2019, doi: 10.1038/s41598-019-47348-5.

[13] C. S. Yang *et al.*, "A Synaptic Transistor based on Quasi-2D Molybdenum Oxide," *Adv. Mater.*, vol. 29, no. 27, Art. no. 27, Jul. 2017, doi: 10.1002/adma.201700906.

[14] J. Zhu *et al.*, "Ion Gated Synaptic Transistors Based on 2D van der Waals Crystals with Tunable Diffusive Dynamics," *Adv. Mater.*, vol. 30, no. 21, Art. no. 21, May 2018, doi: 10.1002/adma.201800195.

[15] V. Sallaz, S. Oukassi, F. Voiron, R. Salot, and D. Berardan, "Assessing the potential of LiPON-based electrical double layer microsupercapacitors for on-chip power storage," *Journal of Power Sources*, vol. 451, p. 227786, Mar. 2020, doi: 10.1016/j.jpowsour.2020.227786.

[16] V. Sallaz *et al.*, "Hybrid All-Solid-State Thin-Film Micro-supercapacitor Based on a Pseudocapacitive Amorphous TiO_2 Electrode," *ACS Appl. Energy Mater.*, vol. 6, no. 1, pp. 201–210, Jan. 2023, doi: 10.1021/acsaem.2c02742.