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A ferroelectric based non volatile SRAM optimized for critical embedded systems

Lucas Rhetat, Jean-Philippe Noel, Bastien Giraud, Laurent Grenouillet, Julie Laguerre, Cédric Marchand, Ian O'Connor

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Abstract SRAMs are the fastest and most energy-efficient commercial memories. However, they are volatile, which means that data must be transferred to a non-volatile (NV) memory before power-off, which is both time-consuming and energy-intensive. NVSRAMs overcome this problem by finely integrating non-volatile storage elements (FeCAPs here) directly into SRAM bitcells. In this work, several design parameters are optimized to ensure error-less data transfer from SRAM to FeCAPs and vice-versa. A previously developed fast-erase system has been integrated for countering cold-boot attacks and improving the reliability of these data transfers. This circuit would therefore be capable of operating in ultra-low power or critical systems with non reliable supplies.

Environment details The circuit is designed in ST 130nm HCMOS9A technology and SPICE simulations are carried out with Synopsys XA with a VerilogA Preisach model for the FeCAPs.

Applications and Memory architecture

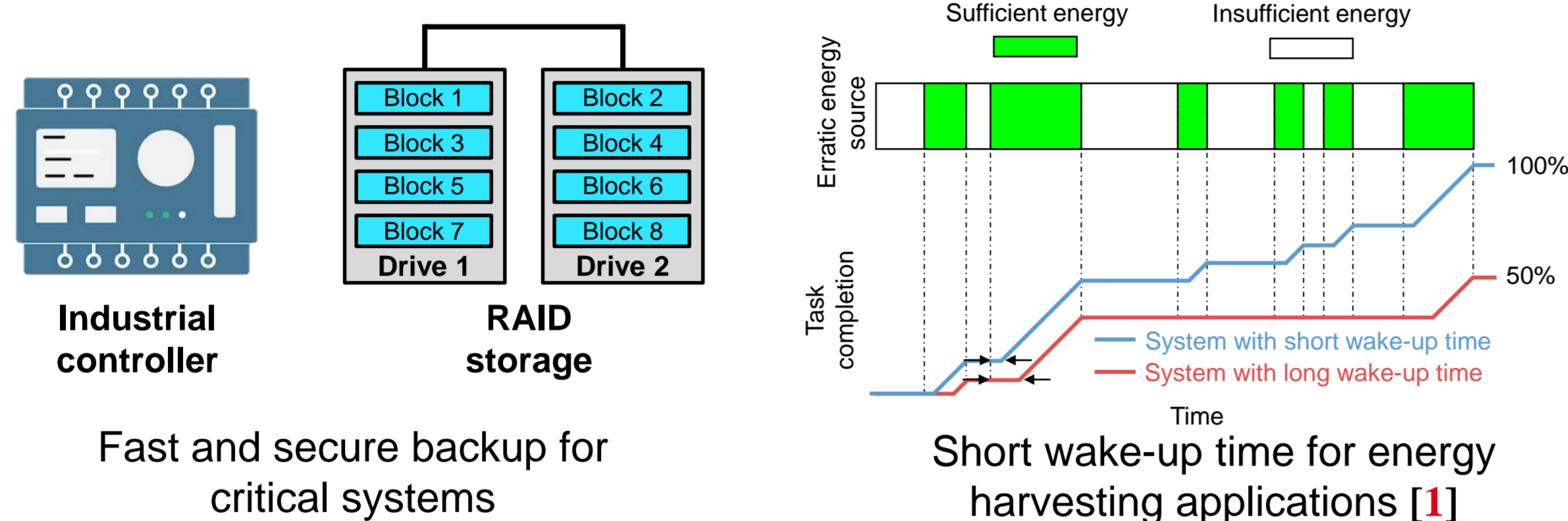


Fig 1. NVSRAMs are suitable for critical systems managing important or secret data or for energy harvesting systems using erratic energy sources.

Reference	This Work	Infineon WhitePaper 2016 [2]	VLSI 2015 [3]	ISSCC 2023 [4]
CMOS bitcell technology	6T 130nm	10T 40nm	7T 90nm	6T 22nm FDSOI
NVM technology	4C BEOL HZO	2T SONOS	IR BEOL HfO ₂	2 Charge-Trap Transistors
SRAM ops. after STORE	Yes	No	No	No
Cold-boot immunity	High (Fast-Erase)	Low	Low	Low
Physical attack cost	High	Medium	High	High
Technology scalability	High	Low	High	High
Endurance	High	Medium	Medium	Low
STORE energy	fJ/bit	nJ/bit	fJ/bit	nJ/bit
STORE time	ns	ms	ns	ms
RECALL time	ns	us	ns	Not specified

Fig 2. Comparison table with existing NVSRAM circuits.

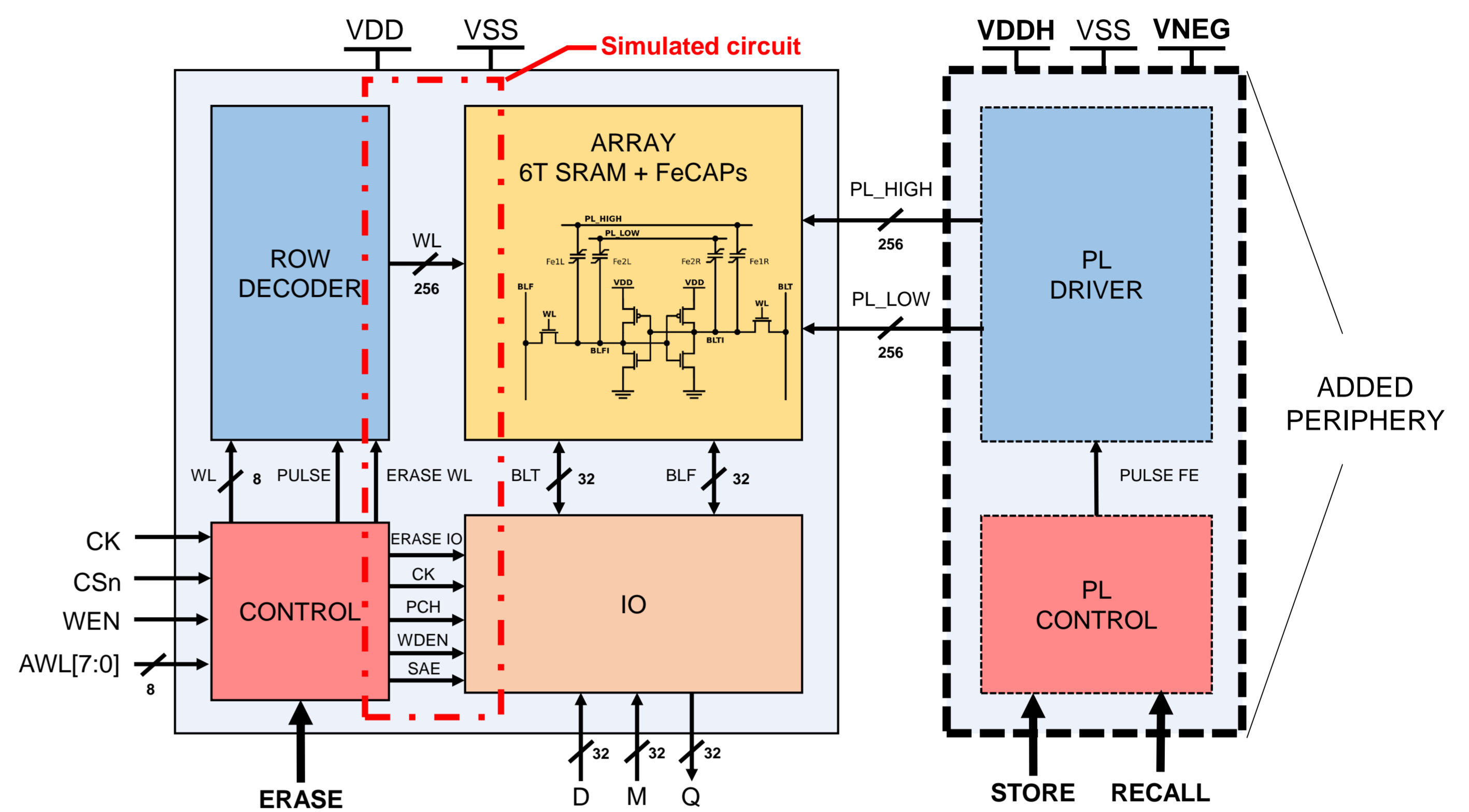


Fig 3. FeCAP-based NVSRAM architecture composed of a modified initial SRAM (left block) and the control of the non-volatile part (right block).

Design optimization

$$A_{FeX} = \text{electrode area of the FeCAP } X$$

$$A_{tot} = A_1 + A_2$$

$$A_1 = A_{Fe1L} + A_{Fe1R} \quad \leftarrow \text{Connected to } PL_{HIGH}$$

$$A_2 = A_{Fe2L} + A_{Fe2R} \quad \leftarrow \text{Connected to } PL_{LOW}$$

$$R = \frac{A_1}{A_1 + A_2}$$

Technology and layout [5]

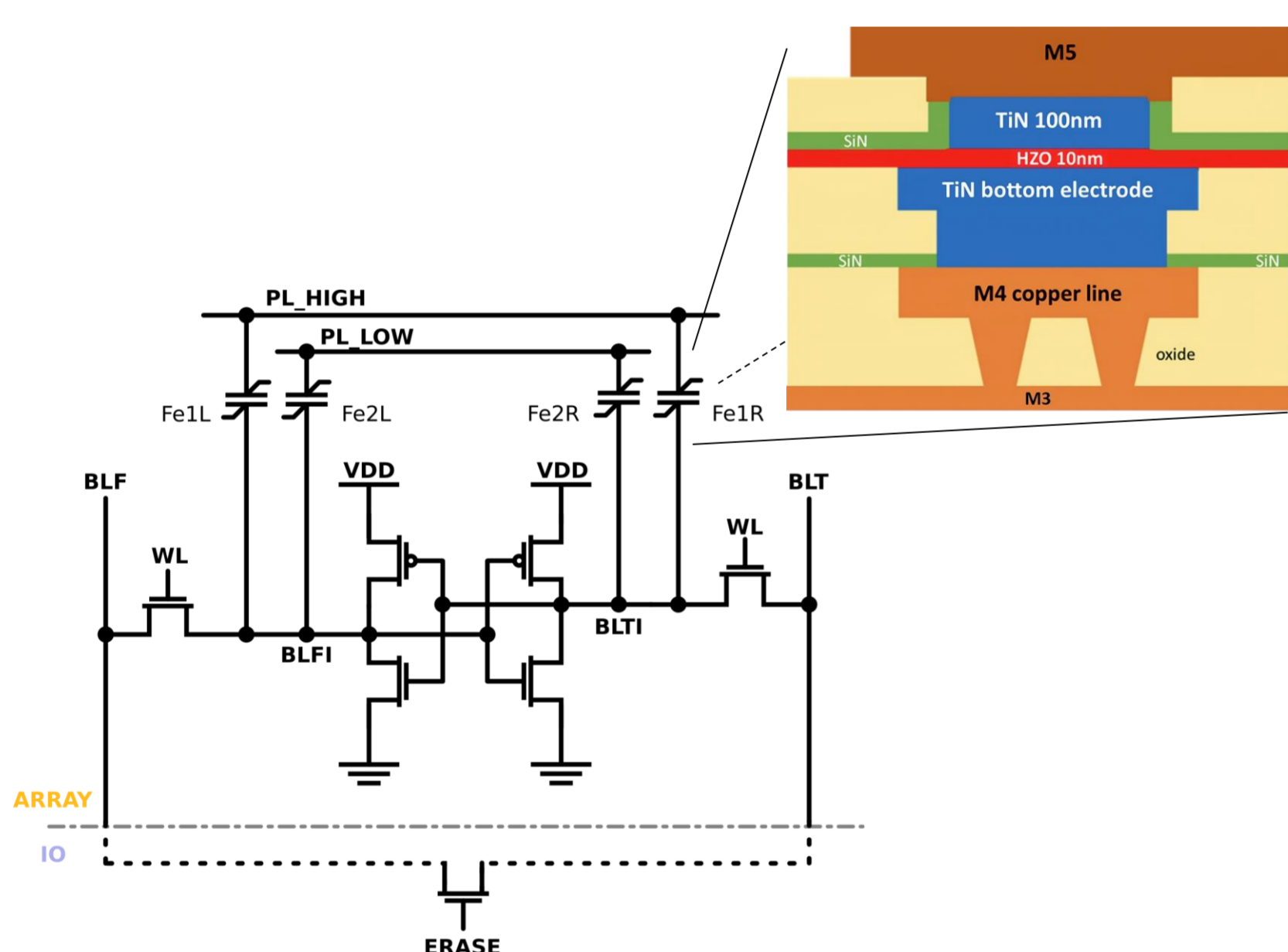


Fig 4. Schematic view of the 6T4C bitcell and cross section of TiN/HZO/TiN MFM capacitors integrated between M4 and M5 layers.

Timing diagrams and Fast-Erase benefits [6]

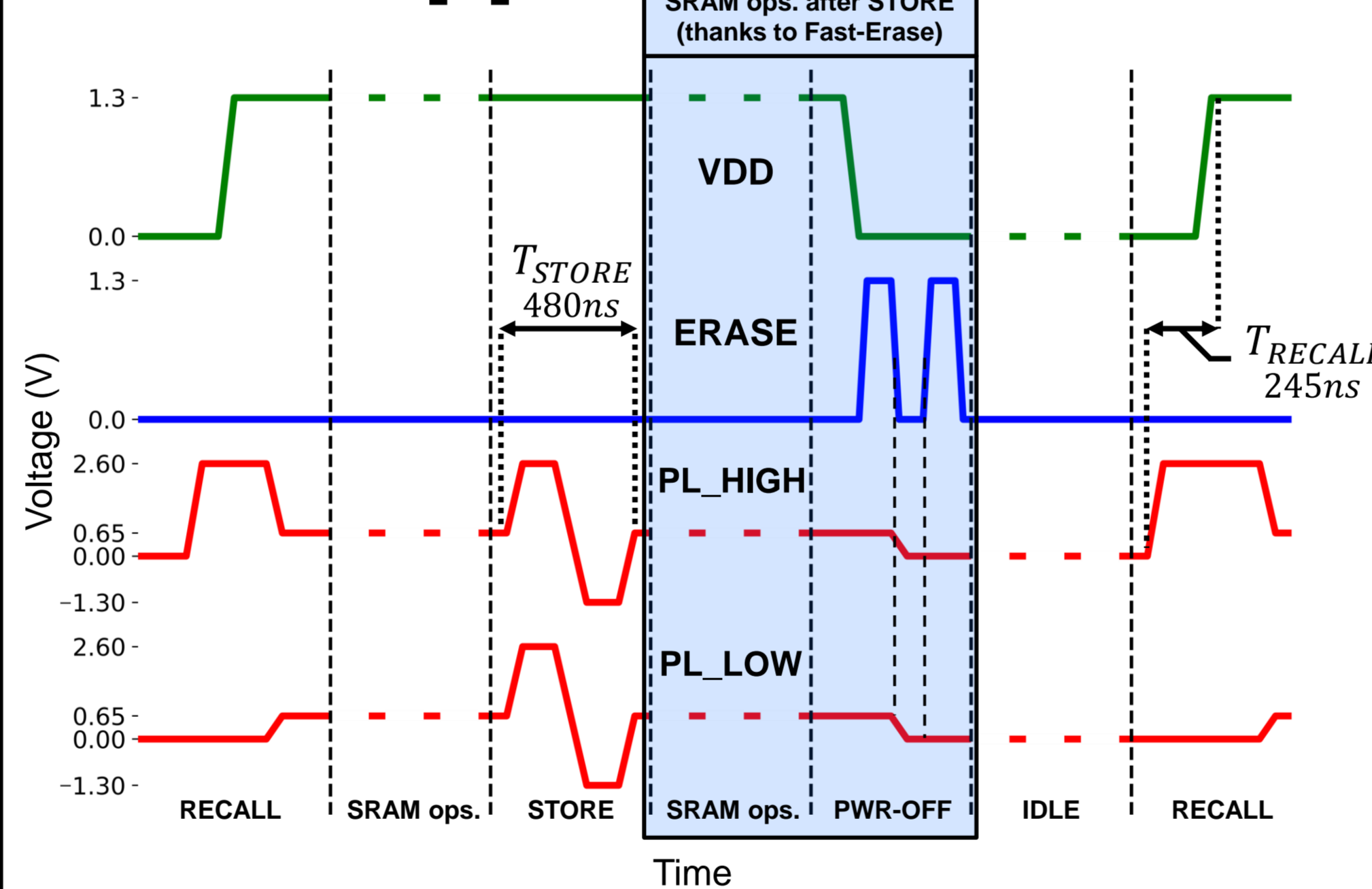


Fig 6. Chronogram of NVSRAM operations. SRAM ops. after the STORE op. enable new applications like SRAM PUF, periodic backups and reduced reboot time.

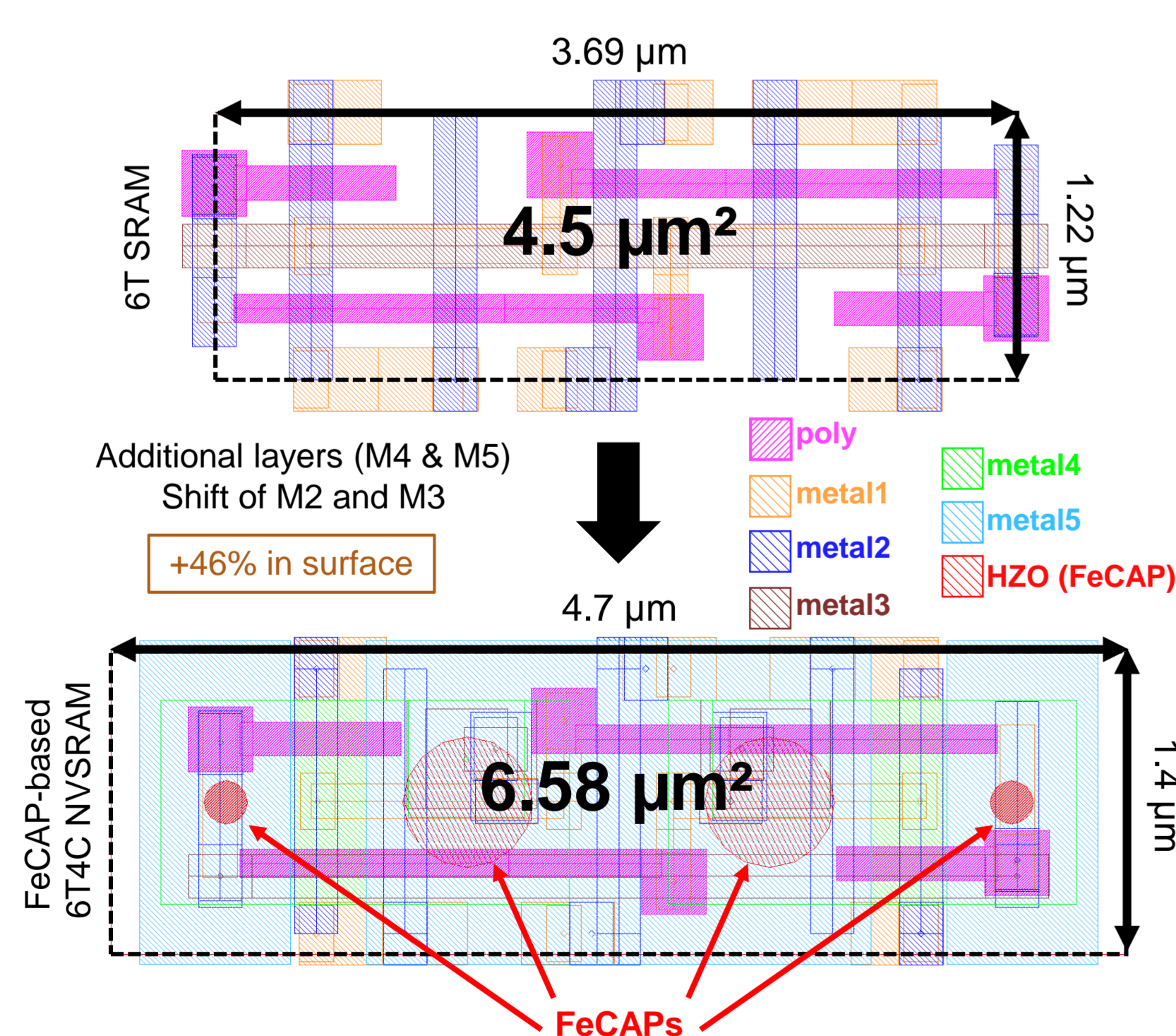


Fig 5. Layout view of conventional 6T SRAM bitcell vs FeCAP-based 6T4C SRAM bitcell in 130nm node, with $A_{tot} = 6e-13m^2$ and $R=0.1$.

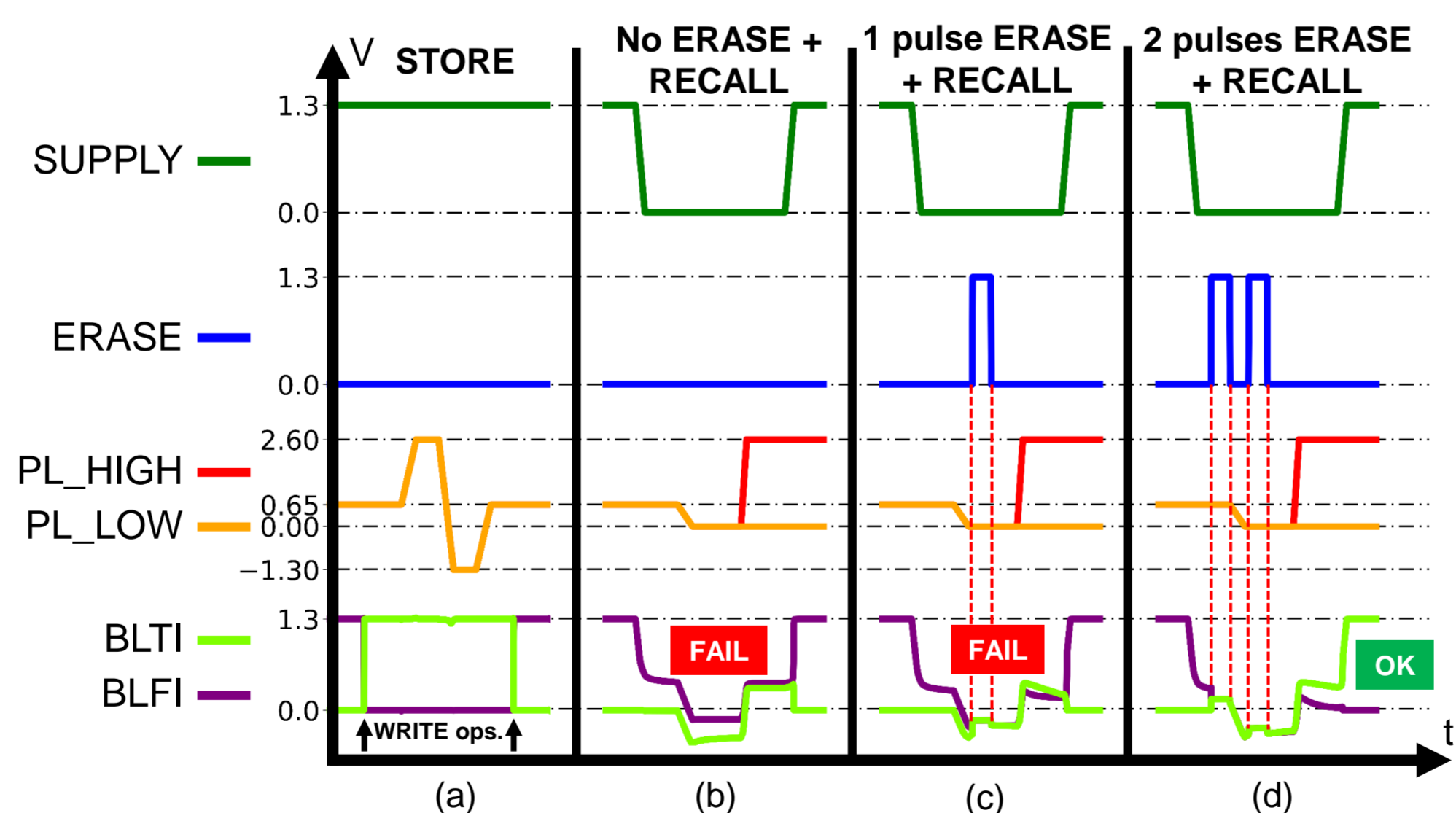


Fig 7. Comparison of the waveforms of SRAM internal nodes, with stored data in (a), between RECALL without ERASE pulse (b), with one ERASE pulse (c), with 2 ERASE pulses (d).

6T4C bitcell exploration [7]

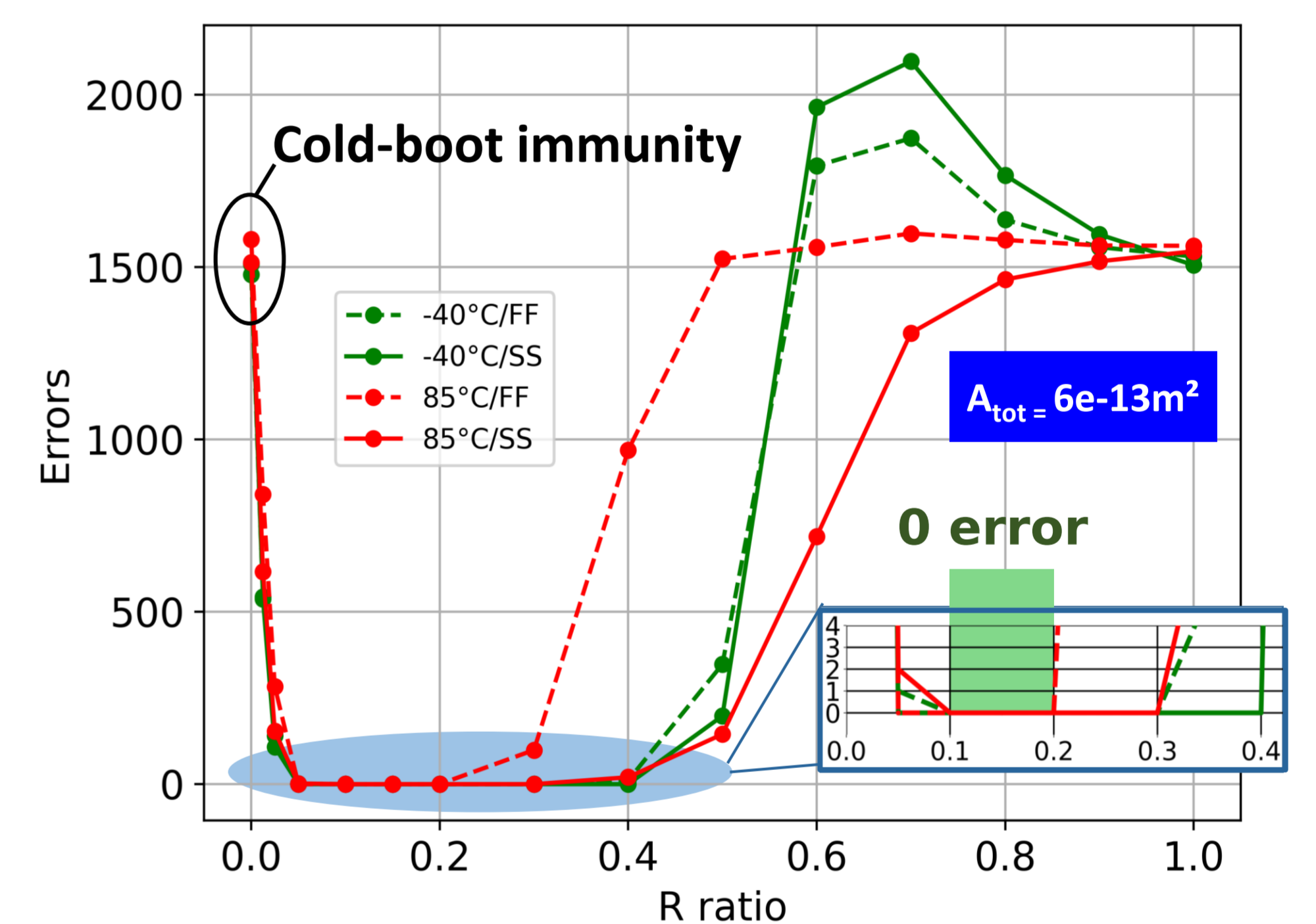


Fig 8. Number of errors on 100 Monte-Carlo runs as a function of FeCAPs area ratio (R). A 0 error configuration is achieved for $R \in [0.1; 0.2]$.

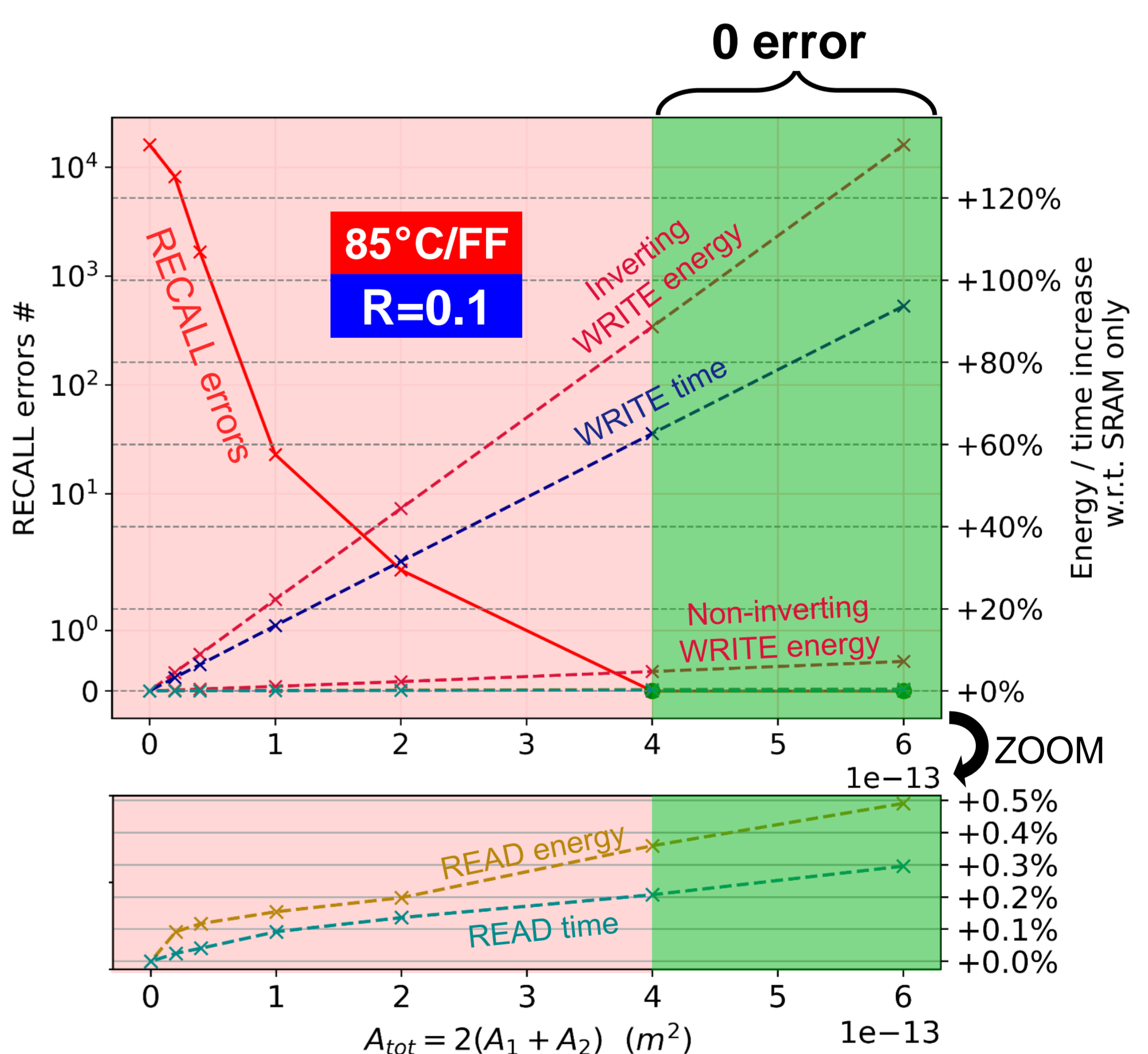


Fig 9. Number of errors for 1000 Monte-Carlo runs as a function of FeCAPs total area (A_{tot}) and corresponding impact on SRAM operations.

Summary

6T4C bitcells and the Fast-Erase circuit are advantageously combined in an efficient and secure NVSRAM memory. 0 error-rate was found for particular ranges of A_{PL1} and A_{PL2} , for SS, TT and FF corners from -40°C to 85°C. The presented 6T4C bitcell presents STORE and RECALL energies of 161fJ/bit and 27fJ/bit, respectively, and STORE and RECALL times of 480ns and 245ns, respectively. The integration of FeCAPs increases the bitcells area of 46% and their impact on SRAM ops. is also evaluated.

Future works

- These ideas will then have to be silicon proven on 130nm technology.
- Potential implementation in 22nm FDSOI technology with 3D FeCAPs.
- Circuit design exploration with FeMFET technology.
- Side-Channel analysis, study of the SRAM PUF use-case, etc.

[1] F. Su et al., "A Ferroelectric Nonvolatile Processor with 46 μ s System-Level Wake-up Time and 14 μ s Sleep Time for Energy Harvesting Applications" in IEEE Transactions on Circuits and Systems, 2017.

[2] R. Prakash, Nonvolatile SRAM (nvSRAM) Basics, Cypress Semiconductor Corp., 2016.

[3] A. Lee et al., "RRAM-based 7T1R nonvolatile SRAM with 2x reduction in store energy and 94x reduction in restore energy for frequent-off instant-on applications" in VLSI Circuits, 2015.

[4] S. Nouri et al., "An 8T eNVRAM Macro in 22nm FDSOI Standard Logic with Simultaneous Full-Array Data Restore for Secure IoT Devices" in ISSCC, 2023.

[5] T. Francois et al., "Demonstration of BEOL-compatible ferroelectric Hf_{0.5}Zr_{0.5}O₂ scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications" in IEDM, 2019.

[6] J.-P. Noel et al., "A Near-Instantaneous and Non-Invasive Erasure Design Technique to Protect Sensitive Data Stored in Secure SRAMs" in ESSCIRC, 2021.

[7] K. Takeuchi et al., "A Feasibility Study on Ferroelectric Shadow SRAMs Based on Variability-Aware Design Optimization" in JEDS, 2019.