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# Die-Level Nano-topography Metrology to characterize the stress-induced In-Plane Distortion contribution to overlay

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## ABSTRACT

In the field of semiconductor manufacturing, the precise alignment of patterns on a wafer die is critical for the proper functioning of the resulting integrated circuit. However, various factors can cause deformation of the die, which can result in overlay errors and negatively impact device performance. In this work, we focused on the development of die nano-topography metrology, which is used to investigate the topography evolution of several dies over several process steps. Impact of manufacturing steps as film deposition, annealing and CMP on die shape deformation produced by different pattern densities is measured using optical interferometry. We show that full-die nanotopography measurement is able to detect stress-induced in-plane die distortion as effect of different annealing processes on SOI or silicon-bulk substrates.

**Keywords:** Nano-topography, metrology, interferometry, distortion, overlay

## INTRODUCTION

The modern Integrated Circuits (IC) manufacturing process consists of a complex series of many process steps. Photolithography is one of the most critical steps in this process and is also executed repeatedly. It is well-known that non-lithography processes may impact the eventual yield and device performance by deteriorating the lithographic pattern quality. For example, IC manufacturing steps like thin film deposition, etching and annealing may induce non-uniform stress variations over the wafer and within the exposure field. This can lead to in-plane distortions (IPD) that may have an impact on the layer-to-layer overlay performance [1-2]. Furthermore, process steps like Chemical Mechanical Planarization can produce topography defects, which may lead to focus issues [3].

Optical profilometry based on interferometry was shown to be able to measure in-process patterned wafers and investigate process-induced focus and overlay problems [4]. While this technique is very useful for a global view at the wafer scale, there is a need for a more accurate view at the die scale. In CEA Leti, we developed a methodology for full-die topography characterization by optical interferometry [5-7]. This technique allows us to acquire more than 50 million of surface topography points and obtain an accurate image of the die-level topography, with a nanometric z-resolution and micrometric lateral (x, y) resolution. Figure 1 shows an example of full die, high-precision topography mapping acquired by using a Bruker Contour-GT-X 3D optical profiler.

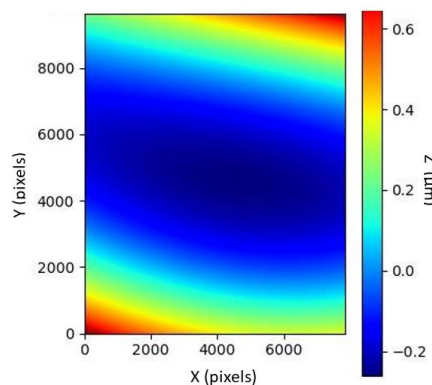


Figure 1: Contour GT-X full die topography mapping

The goal of this work is to study process induced localized die level distortions, in order to relate die residual stress to pattern density over different manufacturing steps.

## EXPERIMENTAL DETAILS

The test layout used is based on CMOS 28nm node design including pattern density variation at die-level as represented in Figure 2.

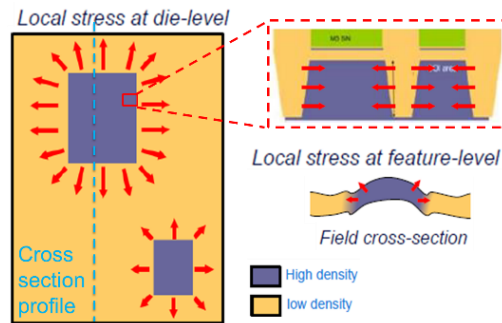


Figure 2: Pattern density variation induce local stress at feature and die-level

The integration flow follows a standard STI process, where critical steps such as thermal oxidation and gap fill deposition, annealing or CMP were characterized by Contour GT-X (Bruker) metrology. For study needs only, two types of substrates were used: silicon bulk wafer and SOI wafer and various annealing process conditions.

Three splits were applied on the wafers:

- POR furnace anneal, further identified as LTA;
- Laser annealing, further identified as LSA, with energy applied just below the SOI top Si layer melting point;
- “Cold” process such as used for 3D monolithic integration.

Process flow is schematized in Figure 3



Figure 3: Schematised process flow used in this study, with metrology steps inserted and different technological steps

Wafer expansion and overlay were measured on ASML NXT platform and YieldStar optical metrology system, respectively. For the optical profilometry measures, part of the wafers was metallized thanks to Ti deposition of 25 nm layer. Full die topography mappings were acquired on 5 dies over wafer radius: obtained data was then averaged (see Figure 4). Second degree polynomial form was extracted considering wafer long range deformation.

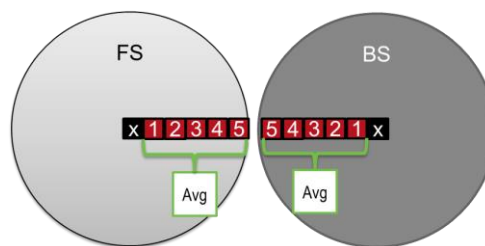


Figure 4: Average die topography was obtained by measuring full die topography on 5 dies over wafer radius

On the remaining residuals, Y-axis cross section profile was extracted through different pattern density, as shown in Figure 2. Further, cross section profiles were fitted with a 3<sup>rd</sup> degree polynomial in order to separate the pattern induced topography from die deformation.

## RESULTS AND DISCUSSION

The wafer expansion and overlay obtained values are represented Figure 5. One can see that technological steps highly influence these two parameters: highest impact is shown for annealing step. Indeed, clear impact of laser annealing (LSA) and furnace annealing (LTA) is observed at Metro 3 for overlay values, reference (cold anneal), in agreement with wafer expansion results. Therefore, the anneal process can be used as a knob to modify stress

global but also local scale. One very interesting observation is that the effect induced by the annealing drops significantly after CMP; both overlay and wafer expansion show quite similar values for the different annealing splits. Concerning the substrate, the wafer expansion values show little difference between silicon bulk and SOI wafers.

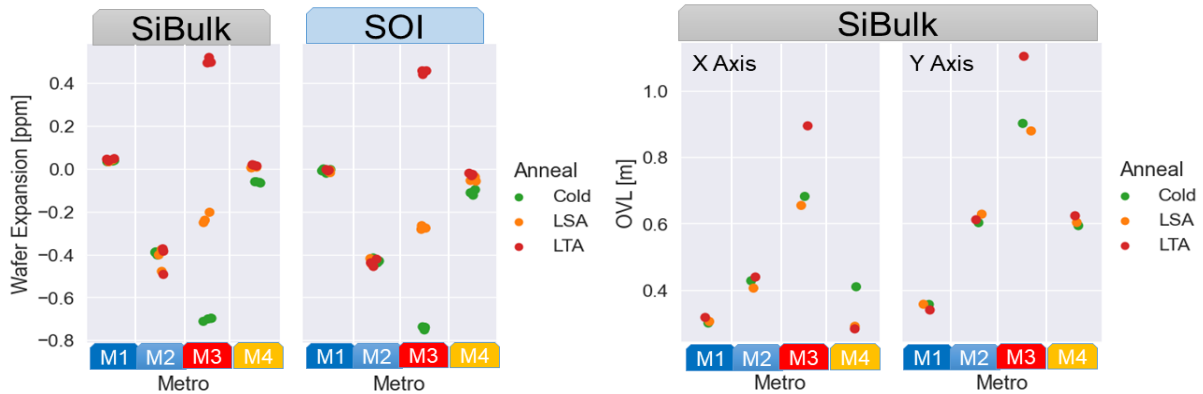


Figure 5: Influence of technological steps and annealing process split on wafer expansion (left) and overlay (right)

Stepping forward to optical profilometry measurements, y-axis extracted profiles and, also, die shapes are shown here below, in Figure 6. Starting with frontside measurements, comparing Metro 1 to Metro 2 one can see there is no significant changes in die shapes but double parabola amplitude changes due to gap-fill step. This double parabola shape indicates local stress induced deformation due to alternating low/density/high density pattern areas over the die. On the other side, it is very important to note complete change of die shape after annealing, for both laser (LSA) and furnace (LTA) anneal. Also, double parabola amplitude is higher for LTA split, in line with overlay and wafer expansion observations.

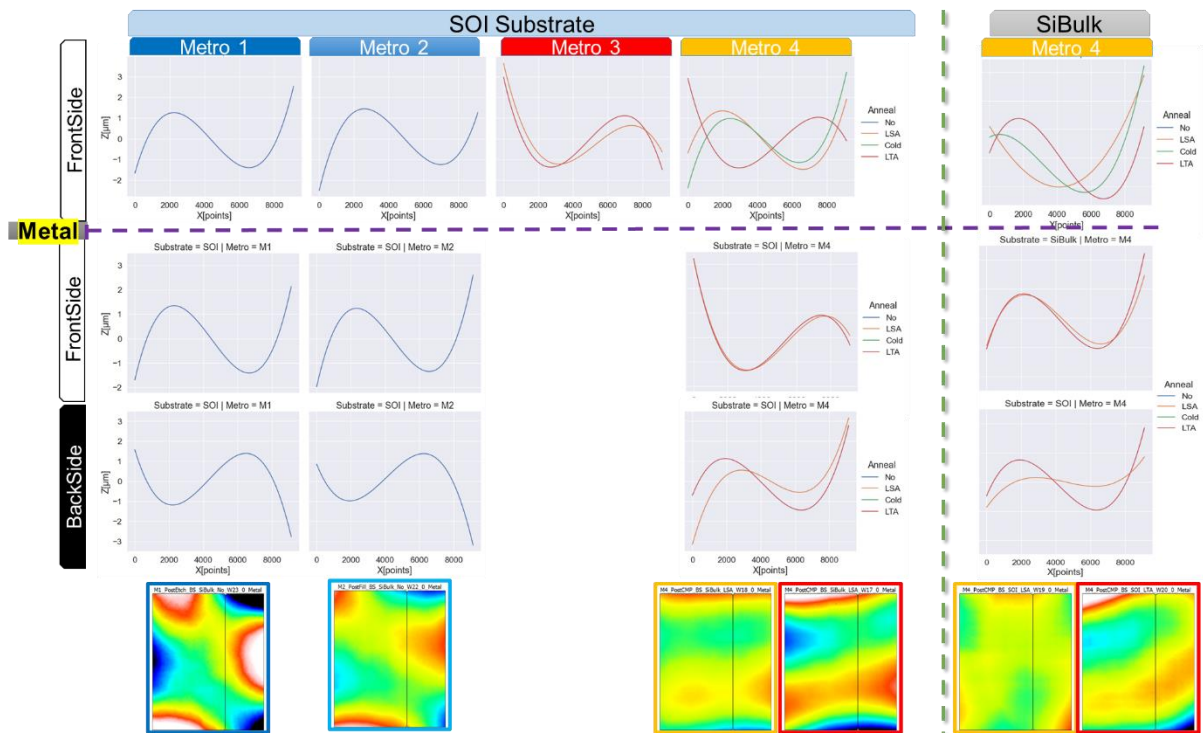


Figure 6: Y-axis extracted profiles from averaged dies measured by optical profilometry over different technological steps. On the bottom side, die-shapes from backside measurements.

Looking at the results obtained after CMP planarization there are several observations to note. While for LTA anneal there is an amplitude reduction, for LSA annealed wafer die shape reverses and have same shape as for “cold” annealing. On the other side, for SiBulk substrate all three shapes are reversed compared to SOI wafers in the same conditions. It seems that higher energy furnace anneal stabilizes more the die deformation, so its shape while dies annealed in LSA or “cold” conditions return to original shape before annealing. Moreover, very

surprisingly, after Ti metallization LSA annealed die shapes change again and are aligned with LTA ones, (while keeping reversed shape between SOI and SiBulk) somehow as the metallization would stabilize the shapes in their post-annealing form.

Finally, in order to confirm the observations made on the frontside of the wafers we did backside measurements of die topography. The cross-section y-axis profiles extracted from these backside measurements are in very good agreement with front-side ones.

## SUMMARY

In this work, we focused on the development of die-scale nano-topography metrology, which is used to study the topography evolution of several dies over several process steps. We investigated impact of areas with different pattern densities on local stress variations at the die-level, for different process steps. Die shape characterization by nano-topography metrology allowed to detect and estimate in-plane distortions induced by different annealing conditions. Obtained results were in agreement with wafer expansion and overlay measures and showed that annealing conditions can be used to influence the local deformations caused by pattern density. These very encouraging exploratory study should be continued by more refined investigation of the pattern density on in-plane die distortions across manufacturing steps.

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