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RESEARCH

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Channel-bonding CMOS transceiver for 100 Gbps wireless point-to-point links



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Abstract

5G systems and networks are expected to provide unprecedented data-rate to final users and services, in combination with increased coverage and density. The traffic generated at the edges of the network should be hauled through high capacity data-conveyors. Extremely high data-rate links able to provide optical-fiber like performance in the order of 100 Gbps are required to reduce the cost and increase the flexibility of the network infrastructure deployment. This paper presents a full transceiver architecture based on a channel-bonding radio-frequency front-end operating at millimeter-wave frequencies and digital baseband processing units able to provide such data-rates with a feasible implementation in low-cost CMOS technologies. The baseband section of the receiver includes digital compensation algorithms that allow to cope with some of the radio front-end impairments. The main functionalities of the proposed transceiver architecture are validated in hardware.

Keywords: Millimeter-wave CMOS integrated circuits, Radio transceivers, Phase noise, Digital-baseband impairments compensation, High-data rate wireless links

1 Introduction

Several millimeter wave (mmW) frequency bands located from 24 GHz up to 40 GHz, depending on the country, are currently under consideration according to 3GPP Release 15 on 5G-NR standard, to provide enhanced mobile broadband (eMBB) access services, but also for backhaul and fronthaul point-to-point links and for internet to the home deployment. However, the available bandwidth at those frequencies will not allow the optical-fiber compatible data rates required to support the increase in data traffic that is expected from 5G and beyond-5G networks. Low installation costs can be achieved by using short and medium-range wireless links able to provide 100 Gbps rank data rates that can compete with optical fiber. Currently, several agencies such as ETSI, FCC, and MICI [1] are considering the bands beyond 95 GHz in order to provide such class of high-data rate for short and medium distance fixed links.

There exist only a few ways to increase the data rate of a wireless link when considering just the electronic transceiver (i.e., in spite of using spatial and/or polarization diversity): increasing the signal bandwidth, increasing the modulation order, improving

to a certain extent the signal to noise ratio (SNR), or a combination of these factors. The SNR at the receiver is governed by the transmit power, the channel path loss, the antenna gains (at transmitter and receiver), and the noise figure of the receiver. Going up in carrier frequency allows to access larger portions of the available spectrum. However, for a given carrier frequency, it is difficult to implement power-efficient radio frequency (RF) electronics having more than 20% of relative system bandwidth (BW). Taking this constraint into account, Fig. 1 presents the maximum capacity as dictated by Shannon-Hartley information theorem on channel capacity for a set of reasonable link parameters in terms of transmit power at the input of the antenna, receiver noise figure and transmit (Tx), and receive (Rx) antenna gains. The figure shows the peak data rates that can be achieved for three distances (10 m, 50 m, and 100 m) considering a line-of-sight path loss model, an additive white Gaussian noise (AWGN) channel and data rates achievable with several modulation types for 20% relative BW. Below the peak, the channel capacity is limited by available BW, and beyond the peak it is limited by the noise. The raw data rate that is provided by each modulation type is shown as well. For 100 m links, 100 Gbps data rate is the maximum achievable for the set of parameters displayed in the inset; it requires a carrier frequency of 125 GHz with 25 GHz of available BW. The position of the peak data rate at a given distance depends on the link parameters. For example, if the Tx power is increased by 10 dB, 240 Gbps at 100 m are theoretically possible using 60 GHz BW around 300 GHz. Interestingly enough, the peak data-rate is achieved always for 4 bits/Hz modulation schemes, such as 16

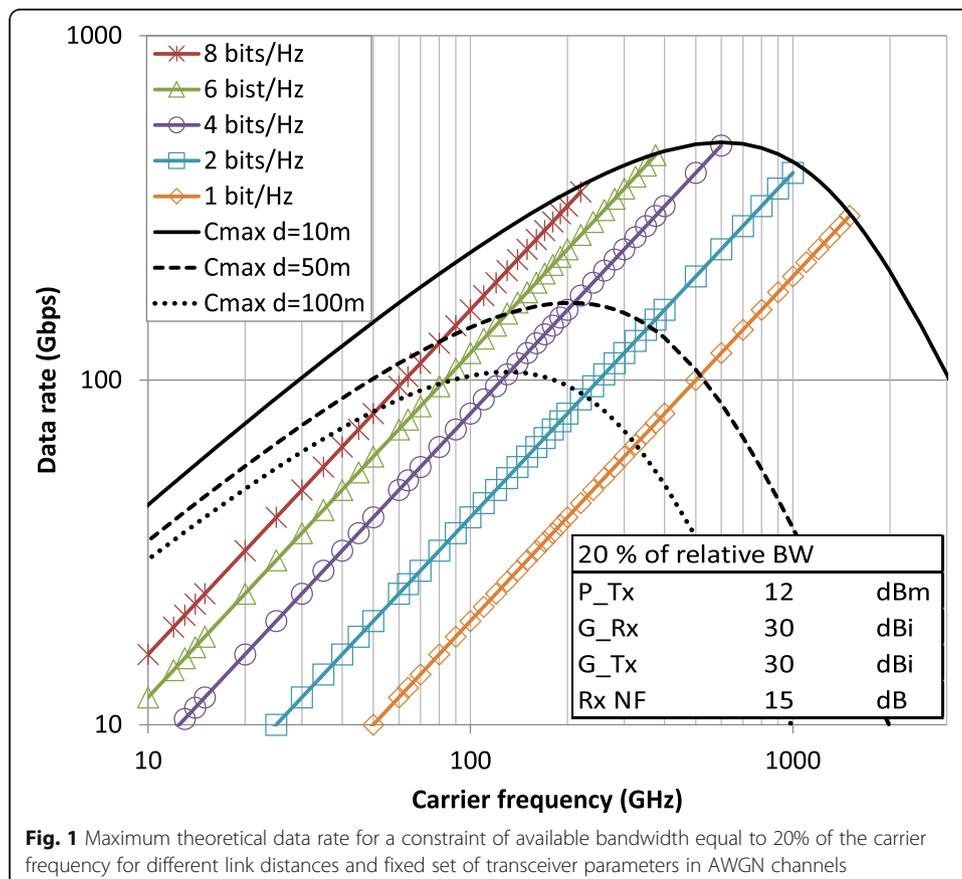


Fig. 1 Maximum theoretical data rate for a constraint of available bandwidth equal to 20% of the carrier frequency for different link distances and fixed set of transceiver parameters in AWGN channels

quadrature amplitude modulation (QAM). Another important conclusion is that in order to achieve 100 Gbps and beyond data rates, carrier frequencies in the range 120-300 GHz need to be used with RF link bandwidths in the order of a few tens of GHz.

The challenges of providing several tens of Gbps wireless links have been addressed by the scientific community following two different implementation approaches. The main characteristics of recent III-V [2–10], complementary metal-oxide semiconductor (CMOS)/bipolar CMOS (BiCMOS) [11–21], and photonic based [22, 23] mmW multi-Gbps wireless transceivers are shown in Fig. 2. The advantage of III-V technologies is based on their higher f_{max} compared to CMOS or BiCMOS technologies. With this technology a large amount of RF bandwidth in a single RF channel is typically used

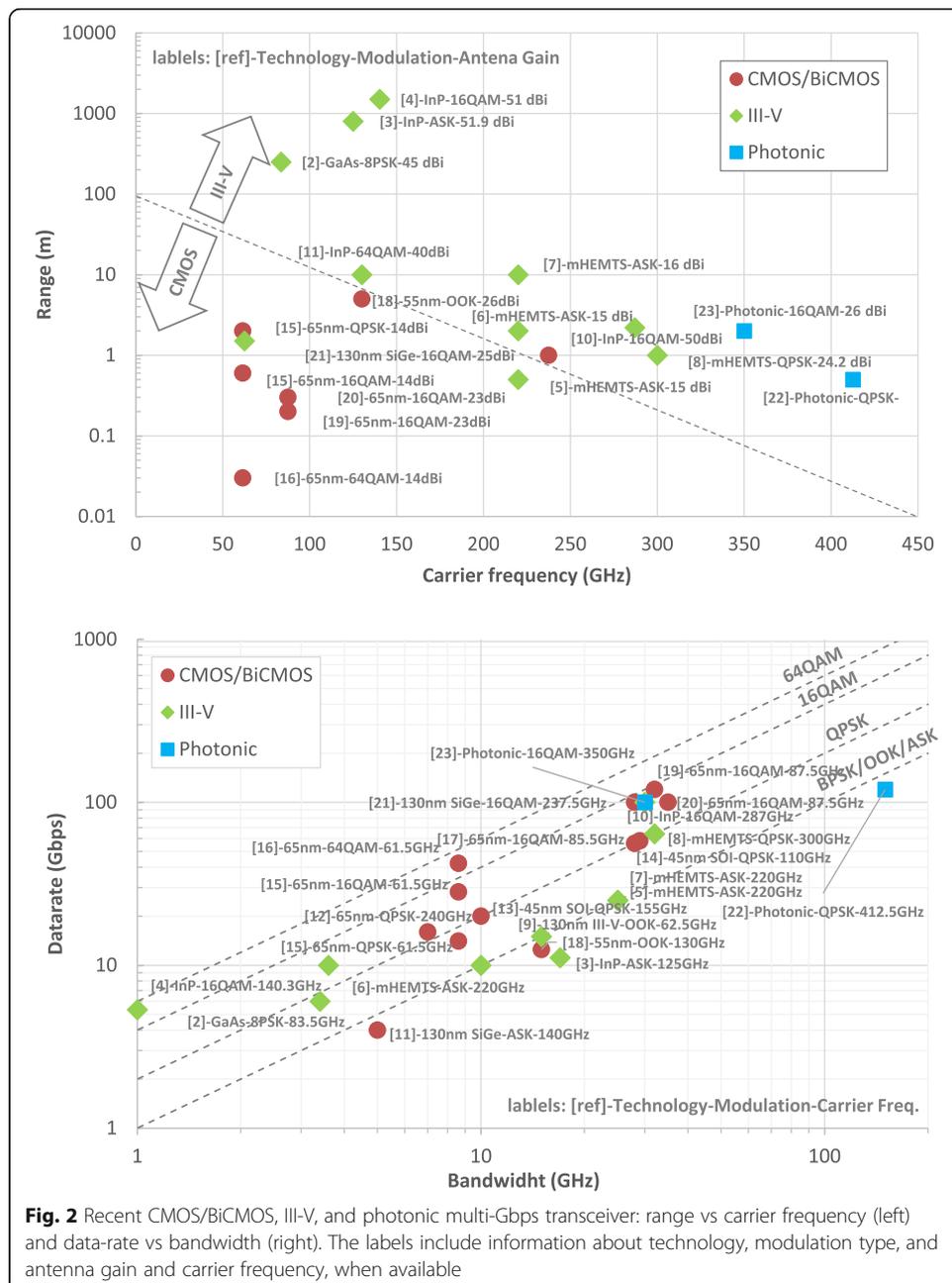


Fig. 2 Recent CMOS/BiCMOS, III-V, and photonic multi-Gbps transceiver: range vs carrier frequency (left) and data-rate vs bandwidth (right). The labels include information about technology, modulation type, and antenna gain and carrier frequency, when available

with simple modulation schemes such as amplitude-shift keying (ASK)/binary phase-shift keying (BPSK) which allow for digital-less demodulation. Such transceivers have been demonstrated for carrier frequencies up to 300 GHz and achieve communication in the range of 1 m up to 1 km using high gain antennas, as shown in Fig. 2. The second approach is based on CMOS or BiCMOS technologies that are limited to lower frequencies and bandwidths. They compensate the limited BW by exploiting higher-order modulations such as quadrature PSK (QPSK), 16QAM, or even 64QAM. This second type of transceivers have demonstrated high data rates at lower carrier frequencies, comparable to those of much larger bandwidth III-V or photonic based transceivers, as shown in Fig. 2. Provided that perfect synchronization and channel equalization is achieved, the optimal modulation appears to be 16QAM for a system exploiting a BW of 20% of the central frequency on AWGN channels, in agreement with the theoretical result shown in Fig. 1. It shall be mentioned that although the AWGN condition over 20% bandwidth is very unrealistic below 10GHz, recent channel measurements have shown that the channel is hardly affected by multipath at very high frequencies [24].

One characteristic that the most efficient state-of-the art CMOS transceivers have in common is the use of multiple parallel RF channels (i.e., channel-bonding) in order to relax the signal bandwidth vs the operating frequency [16, 17, 19, 20], a characteristic that is shared with some of the photonic-based transceivers [22]. Indeed, even though high sampling frequency data converters exist to interface multi-GHz BW front-ends with their digital baseband processing units, their power consumption increases exponentially with sampling frequency beyond 0.5-1 Gsample/s, as shown in [25]. Digital baseband systems data-rate processing capabilities are somehow limited to a few Gbps, and are also bonded by power consumption. Hence, a reasonable trade-off needs to be done between each individual channel bandwidth and the overall number of channels required to cover the full RF band and provide the desired total throughput.

The paper describes an investigation on a multi-channel transceiver architecture able to provide 100 Gbps data rate by bonding several base-band (BB) channels of reasonable bandwidth. Section 2 presents the overall architecture detailing a suitable frequency plan, the radio front-end, and the base-band processor. Section 3 describes the main impairments of large-bandwidth channel-bonding radio front ends, such as phase noise, intra-channel interferences, I/Q imbalance, non-linearities, and the mitigation mechanisms that can be implemented in the BB to compensate such RF imperfections. The methodology used to investigate the effectiveness of the proposed compensation mechanisms based on link-level simulations and measurements on a hardware implementation of the transceiver on a laboratory validation platform is presented in section 4. This study allows to derive reasonable values for the RF front-end (RFFE) imperfections that can be compensated digitally by the BB section. The main lessons learned from this study are summarized in section 5 that concludes the paper.

2 Transceiver architecture

With the goal of implementing fully integrated 100 Gbps transceivers, multi-channel (or channel-bonding) architectures are considered in this paper as the best option to achieve a large overall RF bandwidth with moderately complex modulations (i.e., 16QAM) along with reasonable baseband analog and digital bandwidth.

2.1 Frequency plan

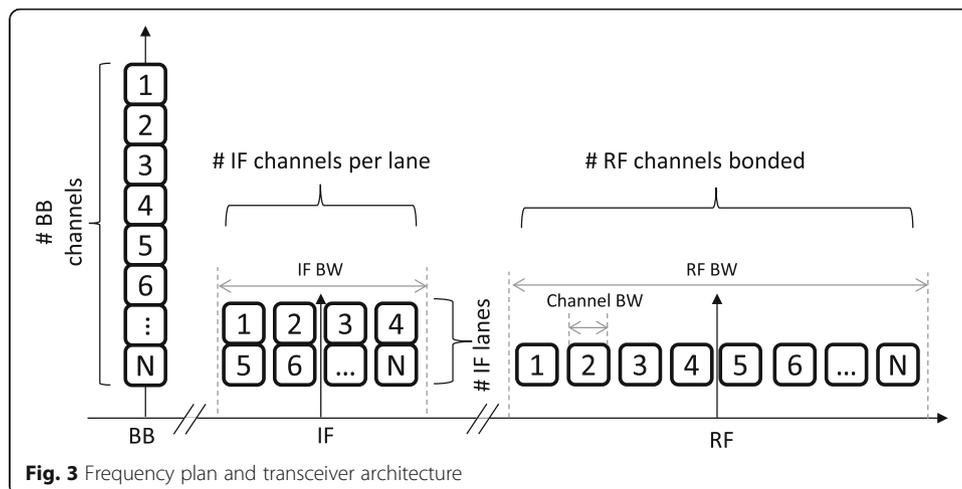
Figure 3 illustrates a channel bonding strategy offering N channels at RF. Two-step frequency conversion is considered in order to avoid offset problems conveniently distribute the gain across the various transceiver stages. Channel-bonding is applied both at an intermediate frequency (IF) and at RF, in order to optimize the frequency plan and the number of local oscillator signals required.

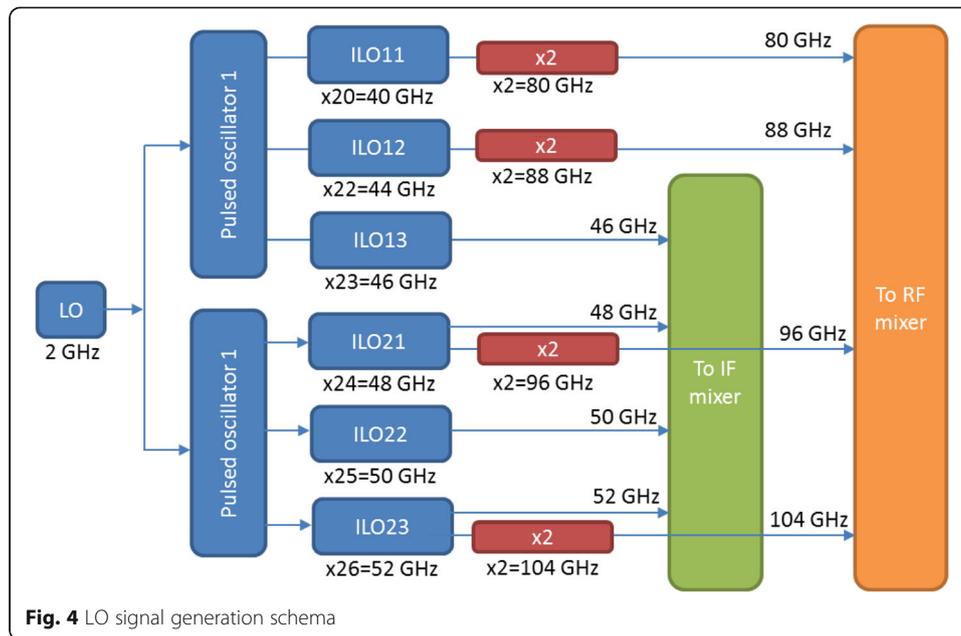
One of the biggest challenges of channel-bonding architectures is the generation of the several required local oscillator (LO) signals. In the example shown in Fig. 3, for a N channel-bonding transceiver, if there are K channels in each IF lane, a total of N/K lanes are required, so that K LO frequencies are needed for up and down conversion from/to BB to/from IF and N/K LO frequencies are needed for the IF to RF (or vice versa) conversion. In the proposed RFFE architecture, detailed in the next section and shown in Fig. 5, it has been chosen $N = 16$ and $K = 4$, which results on 8 different LO frequencies.

A frequency plan, shown in Fig. 4, is proposed in this work to allow all the LO frequencies to be generated from a single common clock reference using high order frequency multiplication. This technique is based on pulsed oscillators followed by injection-locked oscillators (ILOs) that filter out the desired single tone LO signal as explained in [26]. In the proposed architecture, the IF LO frequencies are {46; 48; 50; 52} GHz. They are generated using multiplication by {23; 24; 25; 26} from a 2 GHz input signal. The RF LO frequencies are {80; 88; 96; 104} GHz, and are generated using frequency multiplication by {20; 22; 24; 26} from the same 2 GHz input signal followed by, for example, a push-push based frequency doubler added after the filtering ILOs. The 2 GHz frequency value corresponds as well to the channel spacing, since all LO frequencies are integer multiples of this value. Note that the overall link consists of 16×2 GHz channels, resulting in 32 GHz of RF bandwidth centered around 141 GHz.

2.2 Link budget and RFFE architecture

Figure 5 shows a proposed super-heterodyne channel-bonding RFFE architecture based on the abovementioned frequency plan and the resulting 16 channels spaced by 2 GHz.





The useful bandwidth per channel is considered to be of 1.6 GHz (400 MHz of guard-band is left between adjacent channels to alleviate channel filters and non-linearity constraints). In the transmitter, the 16 BB channels are grouped into sets of four. Each of the BB channel of a set is up converted to a different IF. Then the channels are bonded together in the band 45-53 GHz. The four IF lanes share the same four LO frequencies for BB to IF up conversion. Then, the four IF bundles are up converted to D band using a different LO frequency for each one. After this second frequency conversion, the four up-converted IF lanes are combined in RF frequency resulting in a total of 16 bonded channels at D band (125-157GHz). The receiver is organized in a complementary way, as shown in the figure. This two-step mixing strategy allows to relax the gain and bandwidth constraints for the RF circuits. At the transmitter side, power amplifiers operating at IF have 14% relative BW and those on sub-bands at RF have 6% relative BW. At the receiver side, a single full-band low noise amplifier (LNA) is placed at the antenna port with limited gain to optimize the noise figure, following by RF and IF amplifiers with reduced BW constraints. Because the LNA receives the full bandwidth, the 20% carrier frequency assumption of Fig. 1 is preserved.

A link budget calculation was done (see Table 1) for the link considered in this work, using the following assumptions on Tx and Rx building blocks based on existing CMOS circuit data:

The four power amplifiers (PA) operating in D band shall provide 10.5 dBm output 1 dB compression point (OCP1dB) over their 6% relative bandwidth. This level of output power is reported in [27].

The antenna scheme shall provide 33 dB gain in the 32 GHz bandwidth. For this purpose, a transmit array antenna of 40×40 elements (panel of 25 cm^2) can be used [28], assuming 40% transmission efficiency.

At the receiver side, the LNA shall provide at least 12 dB gain over 32 GHz bandwidth and a noise figure of 9 dB. The total noise figure of the receiver can be then limited to 12 dB. One LNA fulfilling this requirement can be found in [29].

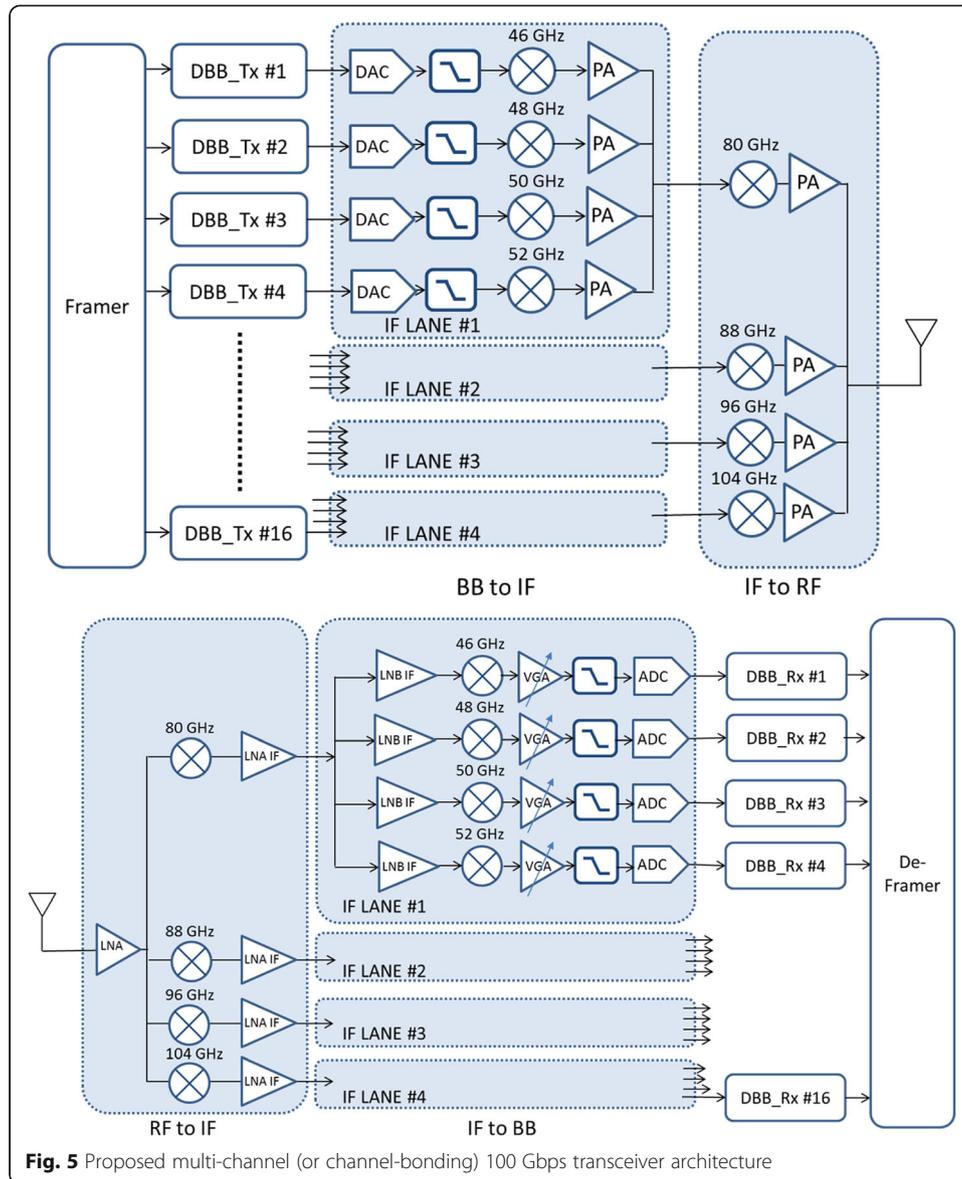


Fig. 5 Proposed multi-channel (or channel-bonding) 100 Gbps transceiver architecture

The IF stages at both the transmitter and the receiver shall tackle the same constraints in terms of power, gain, bandwidth, linearity as the 60 GHz transceivers developed for WiGig applications [30].

On-chip combiners/splitters are required able to combine up to four D band channels with reasonable insertion losses. One possible implementation of this type of combiner/splitter has been recently reported in [31].

According to the results shown in Table 1, a raw data rate of 102.4 Gbps can be achieved at a maximum of 50 m by using 16QAM modulation.

2.3 Digital baseband architecture

Single carrier (SC) waveform with frequency domain equalization (FDE) [30] is one of the possible candidate signals for the multi-channel transceiver. It has been selected

Table 1 Link budget calculation (most numbers are per BB channel)

Element	64QAM	16QAM	QPSK	BPSK
Emitter				
RF BW (GHz)	32	32	32	32
Number of bonded channels	16	16	16	16
Single channel BW (GHz)	1.6	1.6	1.6	1.6
Per PA OCP1B (dBm)	10.5	10.5	10.5	10.5
Per ch. OCP1 dB (dBm)	4.5	4.5	4.5	4.5
Back off (dB)	7	5	3	3
Average power @PA out (dBm)	3.5	5.5	7.5	7.5
Per channel Tx av. Pout (dBm)	-2.5	-0.5	1.5	1.5
Interconnection losses (dB)	2	2	2	2
Antenna gain (dBi)	33	33	33	33
EIRP (dBm)	28.5	30.5	32.5	32.5
Channel				
Range (m)	25	50	120	150
Attenuation coefficient	2	2	2	2
Carrier frequency (GHz)	156	156	156	156
O ₂ & rain attenuation (dB)	0.80	1.60	3.84	4.80
Path loss (dB)	-105.06	-111.88	-121.73	124.63
Receiver				
Antenna gain (dBi)	33	33	33	33
Interconnection losses (dB)	2	2	2	2
Power per channel (dBm)	-44.6	-49.5	-57.3	-60.2
Power at LNA input (dBm)	-32.6	-37.5	-42.3	-48.2
NF (dB)	12	12	12	12
Implementation loss margin (dB)	4.2	2.5	1.2	1.3
SNR @ ADC in (dB)	25.3	20.5	12.7	9.8
SNR for PER 10 ⁻⁵ (dB)	21	18	11.5	8.5
Raw data-rate (Gbps)	153.6	102.4	51.2	25.6

due to its low peak to average power ratio at the transmitter and by the ease of correction of phase rotations at the receiver. Furthermore, FDE allows for inter-symbol interference mitigation with a complexity similar to orthogonal frequency division multiplexing (OFDM).

The structure of the frame is illustrated in Fig. 6. This structure is mainly motivated by the need for time synchronization and RF impairments estimation. Time synchronization uses a known preamble made of N_S repetitions of a given sequence. An autocorrelation and peak detection process allows to find the synchronization sample with very low probabilities of non-detection and false alarm. This preamble also aims at measuring the carrier frequency offset (CFO) (see below). The second preamble is made of M repetitions of a known sequence. It is dedicated to the IQ mismatch estimation in the time domain (see below). The third preamble allows for channel estimation. The payload is made of a number of symbols (the length of a symbol corresponds to the fast fourier transform (FFT) size of the frequency domain equalizer) where pilots (known samples) are distributed.

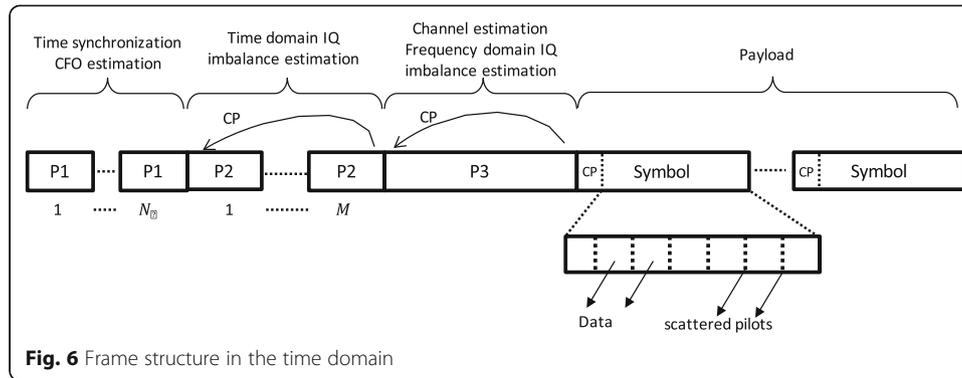


Fig. 6 Frame structure in the time domain

3 RFFE impairments modeling and compensation

The feasibility of the proposed channel-bonding architecture relies on implementing BB digital compensation techniques able to compensate the “imperfections” from the RFFE, alleviating in this way the performance required for the various high-frequency building blocks. A comprehensive model of the full transceiver composed of the BB processor and the RFFE for the Tx and the Rx, along with a realistic channel model derived from experimental measurements [32], is used to validate the transceiver. In this section the main impairments of the RFFE are reviewed. For each one, the way it is included in the link-level model of the transceiver and the numerical values of the different parameters involved are presented and then the compensation mechanism is briefly described.

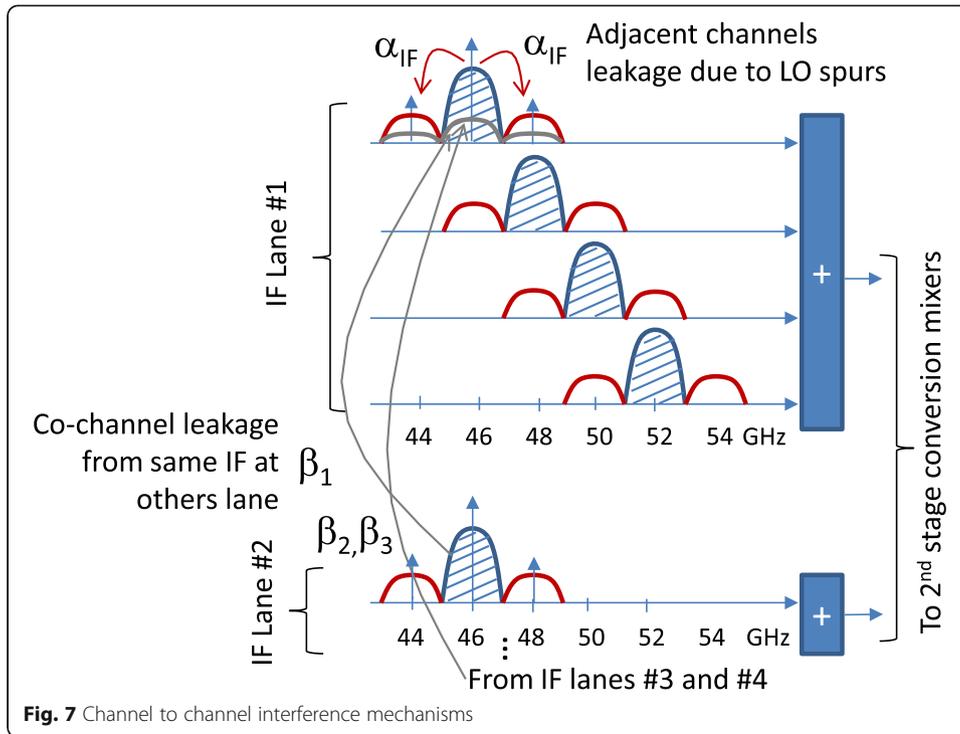
3.1 Channels interferences and LO leakage

Channel to channel interferences are a serious concern in channel-bonding transceivers. In the case of the proposed architecture, the situation is exacerbated because each BB channel shares the same IF frequency as three other BB channels. This is modeled through three coupling coefficients ($\beta_1, \beta_2, \beta_3$), one for each of the interfering IF channel. Furthermore, the technique used to generate the LO from a lower frequency signal that matches the channel spacing is also prone to generating LO spurs at the adjacent channel LO frequencies. Figure 7 illustrates these two channel-to-channel interference mechanisms that happen in the IF section of the transceiver. In the RF section, LO spurs in adjacent channel frequencies could be a source of channel-to-channel interference as well. All such interferences are modeled with coupling coefficients. The coefficients for adjacent channel leakage (α_{IF}, α_{RF}) are calculated considering LO spurs of -20 dBc at the adjacent channel frequencies both for the IF and RF LO signals. For the co-channel interferences, the coupling coefficient β_1 for the closest IF lane (in terms of layout floorplan) is larger than those of the other ones (β_2, β_3). In this paper it is considered that they range from -20 to -26 dB.

3.2 Phase noise

3.2.1 Modeling

Phase noise (PN) is modeled according to the model proposed in [33]. Parameters that describe the phase noise spectrum are illustrated in Fig. 8: (i) $1/f^2$ phase noise at F_{ref} (the spectrum shape at this point decreases by 20 dB per decade); (ii) PLL cut-off frequency; (iii) phase noise floor, i.e., the white phase noise (WPN) floor of the oscillator. Phase noise and white phase noise occur at each stage of the transmitter and receiver



where mixers are involved, i.e., at the output of each ILO and $\times 2$ multiplier in Fig. 4. In the link-level simulations, the $1/f^2$ (bilateral) phase noise of the 2 GHz LO is -130 dBc/Hz (at $F_{ref} = 1$ MHz). The WPN of the 2 GHz LO is found to be limited to -154 dBc/Hz for 16-QAM. The WPN at the output of ILOs and at the output of $\times 2$ multipliers is set to -124 dBc/Hz. The PLL cut-off frequency is selected to be 250 kHz.

3.2.2 Compensation

Phase rotations due to phase noise and residual CFO are estimated and corrected in the receiver thanks to distributed pilots in the time domain, see Fig. 6. The phase of the known pilots is estimated at pilots' positions and interpolated at all the constellation symbols positions. Constellations symbols are then de-rotated according to the opposite of the estimated phase.

3.3 I/Q imbalance

3.3.1 Modeling

IQ mismatch (also called IQ imbalance) arises when a mixer does not respect the amplitude balance or the orthogonality between the I and Q branches. The signal r_{IQ} impacted by IQ mismatch can be written as $r_{IQ} = \alpha r + \beta r^*$, with r as the signal without IQ mismatch, $\alpha = \cos(\Delta_\phi) + j\sin(\Delta_\phi)$, $\beta = \epsilon \cos(\Delta_\phi) - j\sin(\Delta_\phi)$, Δ_ϕ is the phase imbalance and ϵ is the gain imbalance. In the simulations $\Delta_\phi = 5^\circ$ and $\epsilon = 1$ dB.

3.3.2 Compensation

The estimation of IQ mismatch is closely related to CFO. Indeed, CFO degrades the estimation of IQ mismatch and vice-versa. Therefore, in the receiver, the algorithm in

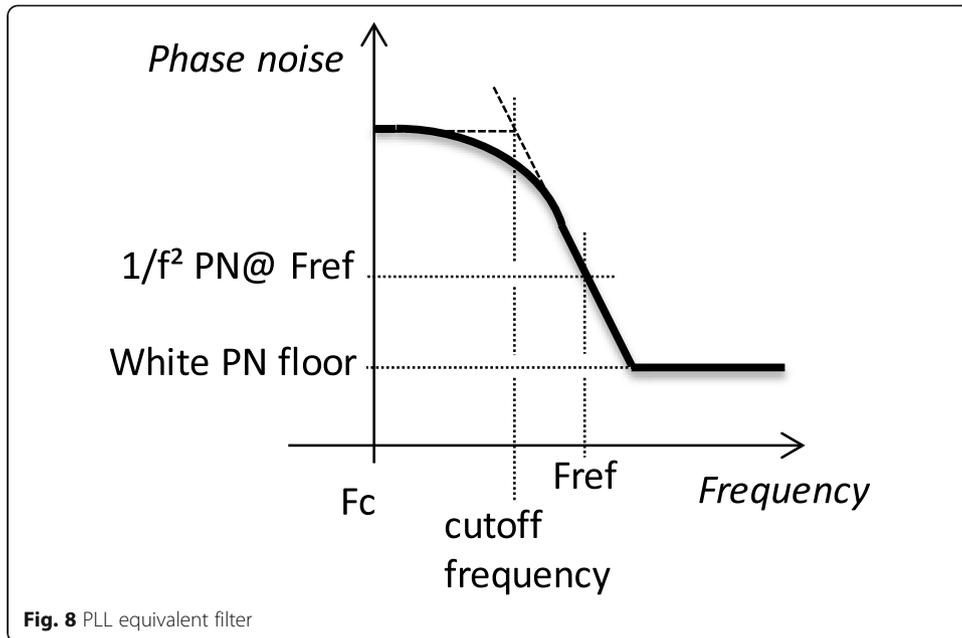


Fig. 8 PLL equivalent filter

[34] has been implemented, as shown in Fig. 9. This algorithm estimates the IQ mismatch either in time domain or in the frequency domain, depending on the estimated CFO value. Furthermore, as IQ mismatch is a slowly varying impairment, it is possible and useful to use the IQ mismatch estimation computed at frame n to correct the time synchronization preamble at frame $n + 1$.

3.4 Non-linearities

The RF components that may introduce non-linearities are mixers, power amplifiers, LNA, and LNB. Non-linearity of a component may cause signal saturation and therefore a packet error rate (PER) increase. For link-level simulations, the gain and the

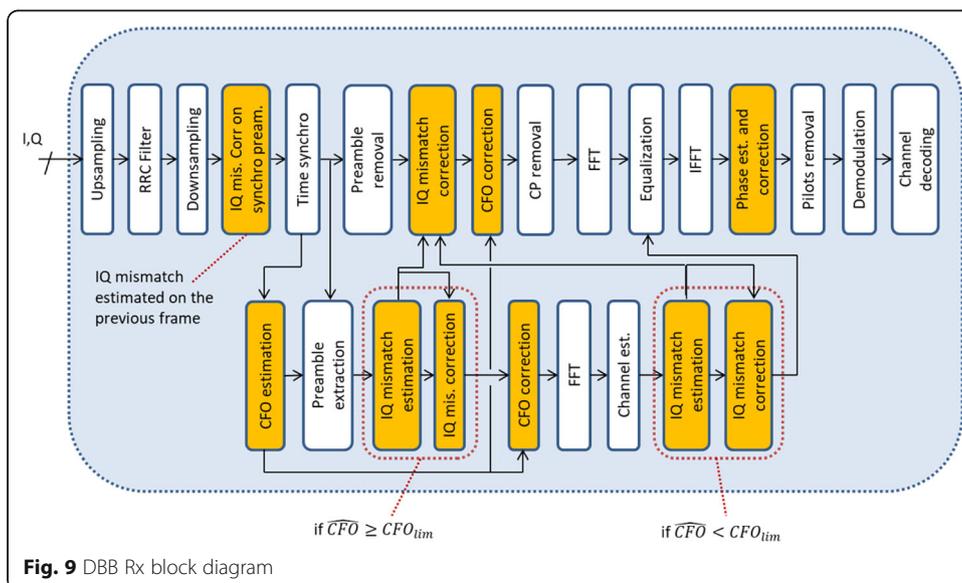


Fig. 9 DBB Rx block diagram

third-order input interception point (IIP3) (or the 1 dB compression point, P1dB, for the PA) of components are taken into account to model their imperfect response. The parameters, extracted from previous experience [35], are summarized in Table 3 along with other system parameters.

3.5 Carrier offset

3.5.1 Modeling

CFO is due to the mismatch between carrier frequencies of the transmitter and the receiver. The CFO is expressed in Hz (CFO_{Hz}) or in parts per million (CFO_{ppm}), with $CFO_{ppm} = CFO_{Hz}/F_c \cdot 10^6$. In the link-level simulations, CFO is modeled by a frequency shift of $2CFO_{Hz}$ (times 2 in order to model the maximal error between transmitter and receiver) in each mixer of the receiver with $F_c = \{80, 88, 96, 104\}$ GHz for the conversion to RF and $F_c = \{46, 48, 50, 52\}$ GHz at IF.

3.5.2 Compensation

The CFO estimation algorithm relies on the time domain synchronization algorithm because the CFO results in a ramp of phase in time, an estimation is given by the phase of the autocorrelation at the detection point. With such an algorithm, the maximum CFO that can be estimated, $CFO_{ppm} = 20$, hereafter, is limited by the length of the autocorrelation window (128 samples). Residual CFO is corrected by time-domain distributed pilots.

3.6 Channel estimation

FDE requires an estimation of the channel in the frequency domain. The algorithm is based on a known transmitted preamble [36] shown in Fig. 6 (the channel is considered invariant during the frame). The channel estimate is obtained by the element-wise division of the received preamble by the known transmitted preamble. Low pass filtering of the frequency domain estimation improves the performance by reducing the contribution of channel noise and white phase noise.

It must be noted that CFO and IQ mismatch estimations have a role to play in the channel estimation process:

- If the estimated CFO is higher than a pre-determined threshold, the IQ mismatch is estimated before channel estimation, thanks to the dedicated preamble. CFO and IQ mismatch are compensated on the channel estimation preamble before channel estimation.
- In the other case, only the CFO is compensated on the channel estimation preamble before channel estimation. The IQ mismatch is estimated in the frequency domain, using the channel estimate: the IQ mismatch parameters that minimize the mean square error between consecutive IQ mismatch corrected channel coefficients are selected. Indeed, the algorithm is based on the information that the corrected channel response should be smooth.

4 Results and discussion

4.1 Methodology

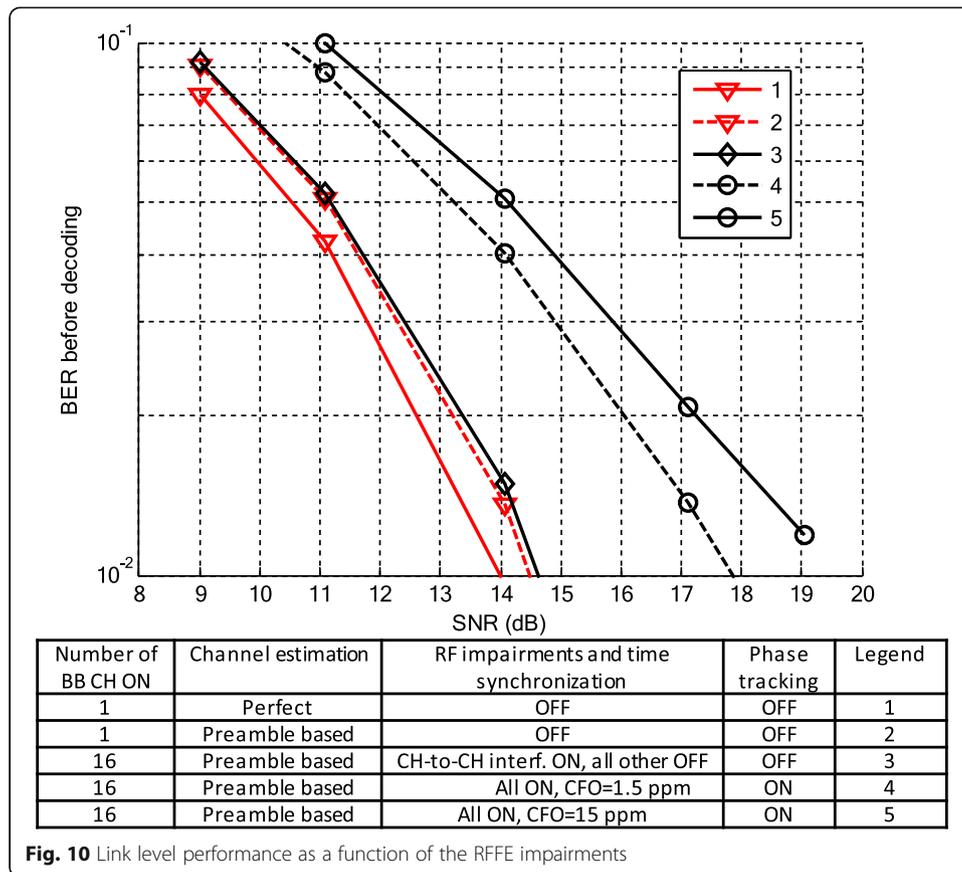
The study presented in this paper relies on a combination of software and experimental equipment-based simulations. The different elements of the transceiver architecture

presented in the previous sections have been implemented in a software simulation chain (run with Matlab), including baseband equivalent models for the radio sections. The models for the analog sections of the radio transceivers include non-idealities such as mismatches between the I and Q branches of mixers, non-linearity in the amplifiers, sideband spurs, and phase noise on the oscillators, etc., as previously described. A realistic model for the wireless channel is also implemented based on previously measured propagation characteristics at D band. The simulation methodology is as follows: the full transceiver software is run on a PC and the non-idealities parameters are varied in order to investigate their impact on the link-level performance. The highest frequency section of the radio is next implemented on a laboratory bench using commercial equipment and the same tests of link-level performance are repeated with a combination of software running the digital signal processing sections of the transceiver and actual equipment implementing the radio section and the propagation channel.

4.2 Analyses of the different RF impairments on the link budget

The model of the link implemented on the simulator includes the digital BB Tx, a model of the RFFE Tx, a realistic model of the channel at D-band derived from the measurements reported in [24], a realistic model of the Rx RFFE including imperfections as well as the Rx digital BB. The software description of the transceiver model constitutes a link-level simulation platform. It has been used to validate the impact of the various system impairments and the ability of the compensation algorithms to correct them and achieve the target error rate. The link-level simulation platform is also used to switch ON or OFF some of the modeled impairments and assess their impact in terms of bit error rate (BER) or PER for the target SNR range considered in the link budget calculation of Table 1. Some results are shown in Fig. 10 for 16QAM modulation and typical link parameters are shown in Table 1. Two imperfections are analyzed in this example: the impact of going from 1 to 16 channels, which allows to investigate the impact corresponding to channel-to-channel interference explained in sub-section 3.1, and CFO that is varied from 1.5 to 15 ppm and used to validate the phase tracking capabilities of the Rx digital BB (DBB) synchronization algorithms. Note that a CFO of 1.5 ppm is the worst case, because this value is close to the CFO_{lim} defined in Fig. 9. BER curves are traced for these cases and compared to the reference scenario in which no impairment is considered and the channel estimation of the Rx is perfect. The overall implementation loss when all impairments (and the corresponding compensation algorithms) are ON results in 6 dB for a BER before decoding of 10^{-2} . Channel interferences, for example, account for less than 0.5 dB of implementation loss.

In order to gain insight on the rest of impairments, a more exhaustive analysis is done by comparing how much of the total implementation loss is due to a given impairment. This is done by turning OFF that particular impairment and leaving ON all the others. The results of this study are summarized in Tables 2 and 3 summarizes the numeric values of the various non-idealities considered in the transceiver architecture. Please note that one must carefully take conclusions from considering some of the impairments individually, since some have a correlated effect. For example, the impact of phase noise is affected by the CFO and the I/Q mismatch, so that turning OFF I/Q mismatch may reduce as well the impact of phase noise on the demodulator performance. The conclusions of



this analyst nevertheless give some clues about the dominant impairments from a qualitative point of view, but no quantitative conclusion can be definitively extracted from them. The results shown in Table 2 indicate that non-linearities on the Tx RF PAs and phase noise of the LO signals have a dominant contribution to the implementation loss, whereas other impairments such as LO spurs and channel-to-channel interferences at IF play a relatively minor role on the transceiver performance degradation.

4.3 Validation using a real D band link and separate Tx and Rx LO generators

Additionally, a proof of concept hardware platform shown in Fig. 11 has been set up for validating the signal processing and RF compensation algorithms on a real D band

Table 2 Implementation losses for PER = 10⁻⁵ when turning off individual impairments

Impairment	Implementation loss
ALL ON	6.0 dB
PAs non-linearities OFF	4.25 dB
Phase noise OFF	4.5 dB
LNAs and Mixers non-linearities OFF	5.0 dB
CFO and I/Q mismatch OFF	5.25 dB
LO spurs and channel-to-channel coupling OFF	5.5 dB
Time synchronization OFF	5.5 dB
ALL OFF	0 dB

Table 3 Summary of transceiver and impairments parameter values

Transceiver parameters		
Number of BB channels	16	
Sampling frequency	2.64 GHz	
Frame duration	30.3 μ s	
Signal bandwidth	1.6 GHz per BB channel, 32 GHz in total	
Modulation	16 QAM	
Channel estimation	Preamble based	
Time scattered pilots	1 pilot every 16 samples	
Cyclic prefix	32 samples	
Shaping filter	RRC, roll-off 0.17 order 30	
Channel	Derived from [24]	
Impairments parameters		
	ALL OFF	ALL ON
Time synchronization	Perfect	Preamble based
Tx power amplifiers	Linear	Gain 25 dB, P1 dB 12 dBm Sat. power 15 dBm
Tx power amplifiers IBO	N/A	5 dB
Rx LNA RF	Linear	Gain: 12 dB, IIP3: -25 dBm
Rx RF mixers	Linear	Gain: 2 dB, IIP3: -28.6 dBm
Rx IF LNAs	Linear	Gain: 16 dB, IIP3: -25 dBm
Rx IF LNAs	Linear	Gain: 14 dB, IIP3: -15 dBm
Rx IF mixer	Linear	Gain: 6 dB, IIP3: -4.5 dBm
Total Rx NF	N/A	10 dB
LO spurious	N/A	$\alpha_1 = -20$ dB, $\alpha_2 = -20$ dB
Ch. to Ch. coupling at IF	N/A	$\beta_1 = -20$ dB, $\beta_2 = -23$ dB, $\beta_3 = -26$ dB
Phase noise model	N/A	Input ref (2GHz): $1/f^2$ PN @ 1 MHz offset = -130 dBc/Hz Phase noise floors: Input ref = -150 dBc/Hz IF LOs = -120 dBc/Hz RF LOs = -120 dBc/Hz

*See section 3.1

**See section 3.2

transmission and with hardware imperfections. The above-described signal processing DBB algorithms, shown in Fig. 9 for the Rx part, are simulated by a software (run with Matlab) and run on a PC that interfaces the instruments. The algorithms in the DBB Rx compensate some of the RF imperfections of the setup such as slow varying phase noise of the LO generators and CFO between the Tx and Rx LO generators, as well as channel equalization due to non-uniform gain across the signal bandwidth of the up and down converter heads and other RF elements (cables, attenuator between Tx and Rx, etc.).

The DBB Tx generates the waveform that is sent to an arbitrary waveform generator (AWG), and frequency up-converted to D band by a sub-harmonic mixer VDI WR6.5, fed by a dedicated signal generator around 20 GHz (6th order harmonic mixing). The RF signal is sent through an attenuator connecting the Tx and Rx (as shown in Fig. 11) or over the air using 10 dBi horn antennas. The received signal is down converted by another sub-harmonic mixer to IF frequency using a separated LO generator. The signal is then sampled at IF by the oscilloscope and sent back to the DBB Rx code that carries out off-line processing on the received digitized signals.

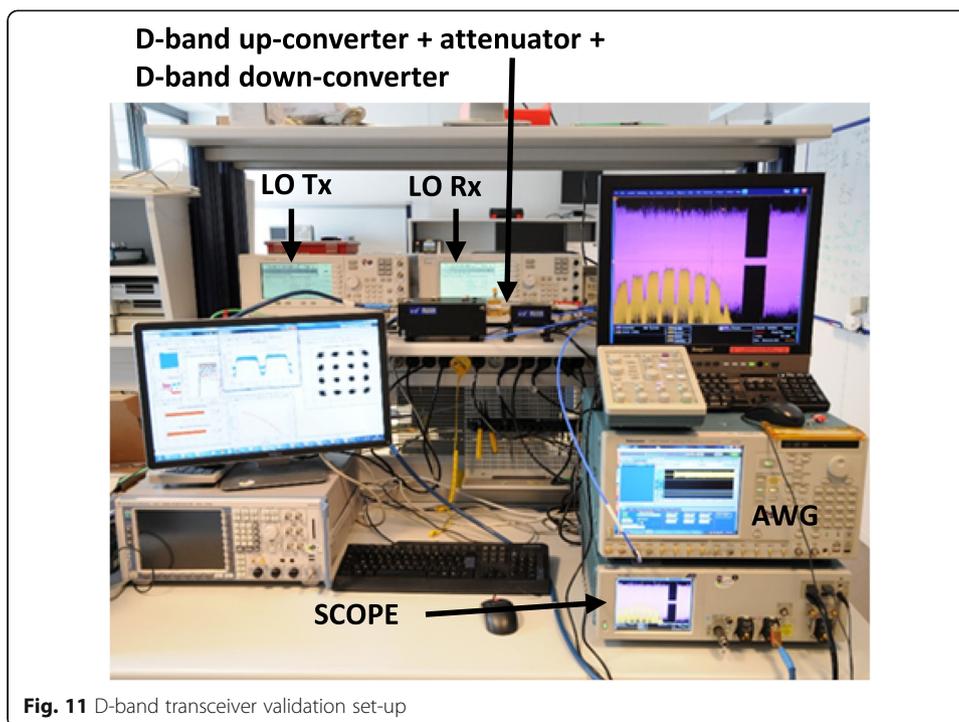


Fig. 11 D-band transceiver validation set-up

The digital to analog converters (DAC) in the AWG behave as a sinc filter, which limits the generated signal bandwidth. In the used AWG Tektronix 70001 offering 50 Gsamples/s, the first Nyquist zone occurs at 20 GHz, which allows to generate 8 channels of 2 GHz. The baseband signal computed in the simulation chain is first upsampled at the AWG sampling rate and digitally up converted at IF to become a real waveform centered into the AWG band. The data format is then converted to binary and exported to the AWG. The mean amplitude signal is set so that it optimizes a trade-off between the clipping and quantization noise of the AWG DACs on 10 bits. At the receiver side, the oscilloscope Tektronix DPO7000SX triggers on the first incoming frame, and acquires the signal at high sampling frequency (up to 200 Gsamples/s). The signal dynamic is optimized to fit the analog to digital converter (ADC) scale on 8 bits. The sampled signal is recorded and sent back to the software simulation chain for processing. The data is first digitally down converted from the receiver IF to baseband and down sampled to the simulation chain rate. The simulation chain provides the received signal constellation after synchronization, RF impairment compensations and channel equalization for every channel. The constellations shown in Fig. 12 are given as

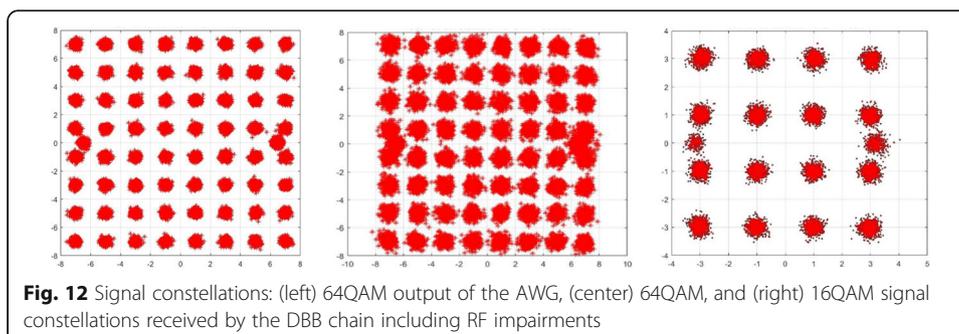


Fig. 12 Signal constellations: (left) 64QAM output of the AWG, (center) 64QAM, and (right) 16QAM signal constellations received by the DBB chain including RF impairments

example for 64QAM, which is a worst case compared to the baseline, and 16QAM modulations. The received 64QAM constellation is compared with the ideal constellation from the simulation chain at the Tx side (generated by the AWG).

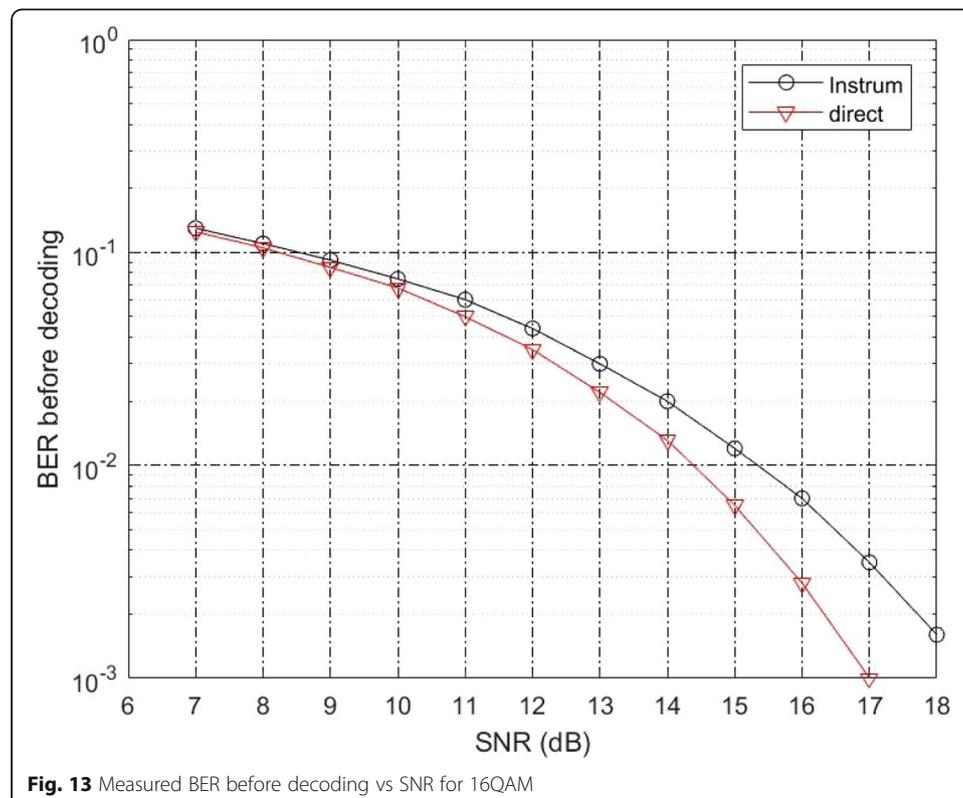
The received constellations exhibit a small rotation due to residual CFO and slow-varying phase noise. They have extra noise compared to the Tx modulation due to clipping, quantization, and channel overlapping. In all the figures, the BPSK modulated pilots are also visible on the constellation diagrams. For the 16QAM constellation, the impairments of the hardware platform degrade the SNR by 1.5 dB at BER before decoding of 10^{-3} , compared to the ideal simulation chain without any impairment as shown in Fig. 13. No noise floor is observed at BER lower than 10^{-5} .

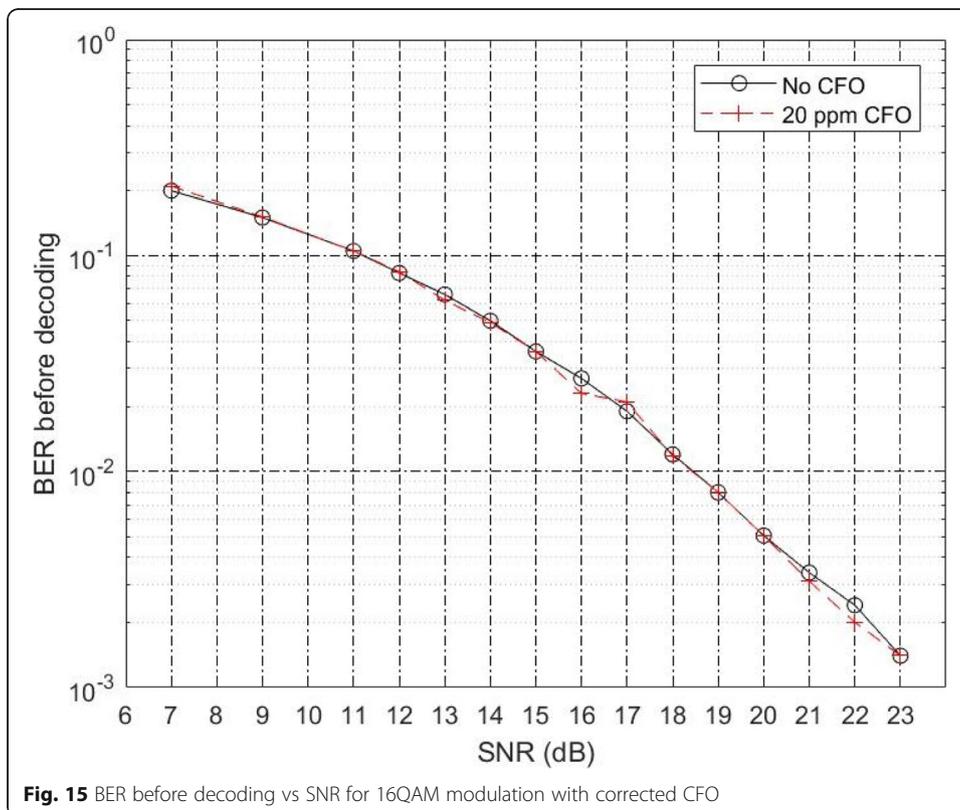
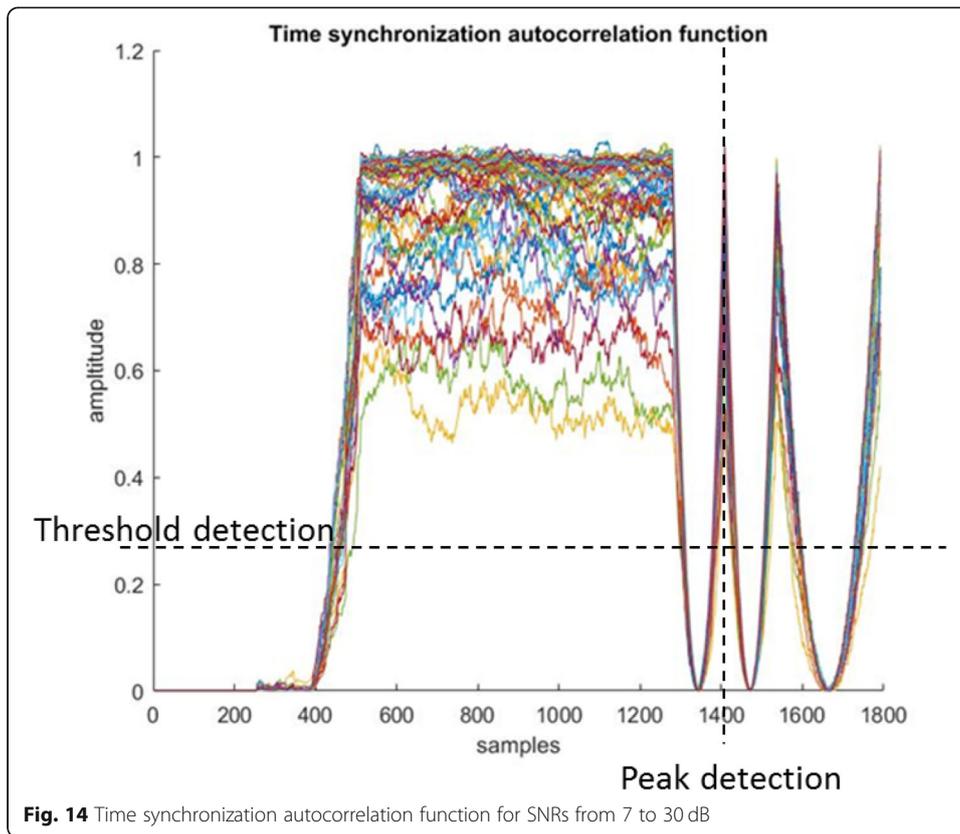
The function of autocorrelation used for time synchronization is shown in Fig. 14 for various SNR values from 7 to 30 dB. The algorithm achieves good time synchronization and coarse frequency estimation throughout all this range of SNR.

The estimation and compensation of the CFO is tested by changing the sub-harmonic up mixer LO frequency with respect to the down-converter mixer LO frequency. The algorithm achieves good estimation up to 20 ppm CFO (which is the maximum CFO that can be corrected), with better than 0.5 ppm precision (for SNR better than 7 dB) and achieves perfect de-rotation and phase tracking as illustrated in Fig. 15.

5 Conclusions

This paper presents a 16 RF channel-bonding transceiver architecture operating in D band able to provide 100 Gbps of raw data rate for 50 m range. 16QAM modulation and digital baseband processing including RFFE impairments compensation has been





demonstrated. The RFFE is based on a double conversion architecture with multiple parallel lanes, and features a reduced number of LO frequencies. A full link-level simulation platform including a realistic model of the channel has been developed and used to investigate the feasibility of the proposed architecture and to assess the performance of the DBB compensation algorithms. Phase noise and PA non-linearities have been found to be the most impacting non-idealities. Nevertheless, regarding phase noise, the proposed phase synchronization algorithm is able to cope with LO phase noise derived from an input signal at 2 GHz with up to -130 dBc/Hz @ 1 MHz offset and a noise floor of -154 dBc/Hz that translate to -93 dBc/Hz and -127 dBc/Hz at 140 GHz, respectively. Other performances such as CFO compensation and time synchronization have been also validated both using the link-level simulation platform with a realistic channel model and a hardware implementation, showing for example, that CFO between Tx and Rx of up to 20 ppm can be tolerated without significant degradation. Both test beds (simulation and hardware) have been used to assess that channel-to-channel interferences and LO leakage at adjacent channels are not a limiting issue for this type of highly parallel RF architectures, paving the way to extremely large bandwidth mmW transceivers using relatively low base-band bandwidth.

Abbreviations

5G: 5th generation; ADC: Analog-to-digital converter; ASK: Amplitude shift keying; AWG: Arbitrary waveform generator; AWGN: Additive white Gaussian noise; BB: Base band; BER: Bit error rate; BiCMOS: Bipolar-complementary metal-oxide-semiconductor; BPSK: Binary phase shift keying; BW: Bandwidth; CFO: Carrier frequency offset; CMOS: Complementary metal-oxide-semiconductor; DBB: Digital base band; dB: Decibel; dBc: Power level in decibels relative to the carrier; dBi: Gain of antenna with respect to an isotropic source; dBm: Power units in decibel normalized to 1 mW; EIRP: Equivalent isotropic radiated power; eMBB: Enhanced mobile broadband; ETSI: European telecommunications standardization institute; FCC: Federal communications commission; FDE: Frequency domain equalization; Gbps: Gigabits per second; GHz: Gigahertz (10^9 hertz); I/Q: In-phase and quadrature; IF: Intermediate frequency; IIP3: 3rd order input intercept point; ILO: Injection locked oscillator; kHz: Kilohertz (10^3 hertz); LNA: Low noise amplifier; LO: Local oscillator; MHz: Megahertz (10^6 hertz); MICI: Ministerio de Comercio e Industrias; mmW: Millimeter wave; NF: Noise figure; OCP1dB: 1 dB output compression point; OFDM: Orthogonal frequency division multiplexing; P1dB: 1 dB compression point; PA: Power amplifier; PAPR: Peak to average power ratio; PER: Packet error rate; PLL: Phased locked loop; PN: Phase noise; Pout: Output power; PSK: Phase shift keying; QAM: Quadrature amplitude modulation; QPSK: Quadrature phase shift keying; RF: Radio frequency; RFFE: Radio frequency front-end; RRC: Raised rooted cosine; Rx: Receiver; SC: Single carrier; SNR: Signal to noise ratio; Tx: Transmitter; WiGig: Name of a 60 GHz standard for wireless gigabit; WPN: White phase noise

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Authors' contributions

JLG-J and DN have coordinated the work, JLG-J, C.D., and A.S. have contributed with the modeling of the radio section and the experimental set-up, N.C., Y. D, A.dD., and V.S. have contributed with the design and implementation of the digital signal processing section of the transceiver, and A.C. and R.D'E have contributed with the air interface and channel modeling. All authors read and approved the final manuscript.

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Availability of data and materials

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

Competing interests

The authors declare that they have no competing interests.

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