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Normally-OFF 650V GaN-on-Si MOSc-HEMT Transistor: Benefits of the Fully Recessed Gate Architecture

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Abstract— In this paper we present a detailed performance status of AlGaIn/GaN MOS channel High Electron Mobility Transistors (MOSc HEMTs) with fully recessed gate architecture on 200mm Si substrates. We report a wide range of wafer and package level results. ON state resistance is studied through three aspects: *i*) R_{ON} partitioning with analysis of its four components, *ii*) R_{ON} temperature dependence, *iii*) cumulative dynamic R_{ON} under stress. For accurate power assessment we characterize packaged devices and compare the typical figures of merit (gate charge, switching tests) to state of the art references (especially pGaN gate HEMTs). We highlight the benefits offered by this technology for 650V applications, such as very low I_{GSS} leakage even at 150°C, and better switching performances, $t_{d(on)}$, $t_{d(off)}$.

Keywords—Power, GaN-on-Si, AlGaIn/GaN, MOSc HEMT, fully recessed gate architecture, 200mm Si substrates, ON state resistance, 650V application, packaged devices

I. INTRODUCTION

For power transistors [1-11] the three main general requirements are a high breakdown voltage, normally-OFF operation and a low ON state resistance (R_{ON}). Wide bandgap materials such as GaN have high critical electrical field, making GaN HEMTs especially adapted to reach the high breakdown voltage requirement. Different approaches have been considered to achieve GaN HEMTs normally-OFF operation. The two most promising concepts are the pGaN gate (today's commercial solution [3-4]) and the recessed gate MOSc-HEMT [1-2], [8-11], which is the scope of this paper.

In this paper, we first present our latest integration process and new in-line gate cavity characterizations (**Part II**). Then we focus on R_{ON} studies and on the advantages offered by recessed gate MOSc-HEMT (**Part III**). Finally we extend these analysis to packaged devices (**Part IV**).

II. TECHNOLOGY AND DEVICE DESCRIPTION

A. Normally OFF Recessed AlGaIn/GaN MOSc HEMT flow

Normally OFF Recessed AlGaIn/GaN MOS-HEMTs on 200mm Si substrates are fully fabricated in our clean rooms. The device structure is illustrated in **Fig. 1a**, and the related process flow is described in **Fig. 1b**.

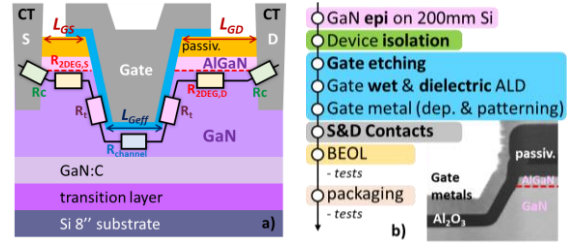


Fig. 1. a) Schematics of the fabricated GaN-on-Si MOSc-HEMT with fully recessed gate. The four R_{ON} components (Fig. 4) are also indicated. b) Summary of the developed process flow for 200mm GaN-on-Si E-mode MOS channel HEMT, with fully recessed gate (+TEM image).

After growth by MOCVD of transition and GaN:C layers on Si the epi stack ends with an unintentionally doped (uid GaN) channel, AlN spacer, AlGaIn barrier and in-situ SiN passivation layer. The gate structure is formed by AlGaIn/GaN dry etching (fully recessed gate), followed by adapted GaN surface conditioning, dielectric (30nm ALD Al_2O_3) and metals depositions. The ohmic source-drain contacts are formed with full-recess etching and low temperature Ti/Al process. The wafer process finishes with three levels Back-End Of Line (M3) and in-line electrical characterizations. After dicing, 30A-650V calibrated transistors are packaged for final electrical assessments

B. New in-line 3D characterization method for gate cavity

An in line CD-SEM measures 2D distances between edges. For 3D pattern metrology we developed an original and efficient technique based on eTilt SEM imaging [6]. By tilting the primary electron beam, sidewalls of patterns become visible and measurable for single line edges, or for multiple line edge statistics. To deconvolve sidewall angle from pattern thickness variation, two images with different eTilt (α_1 , α_2) were taken on the same target extracting the AlGaIn/GaN Edge Width CD (**Fig. 2**).

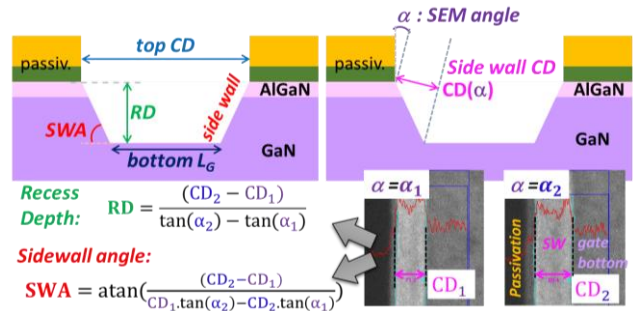


Fig. 2. Gate cavity in-line measurements. Recess Depth, RD, and Sidewall angle, SWA, are calculated using two off-angle CD-SEM measurements.

This technique was applied to measure the etched gate recess depth (RD) and sidewall angle (SWA) and developed on short-loop wafers with four different etching processes. **Fig. 3** shows an example of sidewall angle values obtained with this technique, and the correlation with bottom CD values. This methodology was validated by different comparisons (RD & SWA from TEM) and **Fig. 3** shows the self-consistency of the technique (top L_G , bottom L_G , SWA and RD).

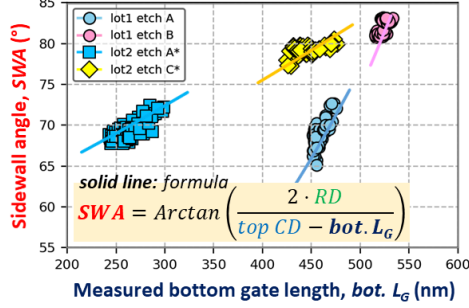


Fig. 3. Illustration of in-line characterizations (SWA vs. bottom L_G) from shortloop wafers. Model based SWA calculations show a good matching with the method data points (results from four etch conditions, two wafers per split, 41 dies per wafer, for a given device layout).

This 3D method enables us to analyze the impact of random process induced variations across the wafer and opens new opportunities for fine process/electrical correlation studies.

III. DEVICE RESULTS (WAFER LEVEL)

A. R_{ON} partitioning study

One critical aspect for device optimization is the R_{ON} minimization. It is thus essential to accurately determine its components (**Fig. 4**: $R_{ON} = 2.R_C + R_{2DEG} + 2.R_f + R_{channel}$ [5,11]) in order to optimize the related modules. TLMs are used to determine contact resistance (R_C) and 2DEG sheet resistance ($R_{sh,2DEG}$). Channel sheet resistance ($R_{sh,channel}$) is obtained from $R_{ON}(L_{G,eff})$ curves measured on transistors with different gate lengths (**Fig. 5**). It is important to point out that the effective gate length $L_{G,eff}$ to consider in recessed-gate structure is the bottom gate length described in **Fig. 2**.

Once these parameters have been extracted, one can apply this method to any device with known layout ($L_{G,eff}$, W , L_{GS} , L_{GD}) with the formulas reported in **Fig. 4**. An example of this is shown in **Figs. 5-6**.

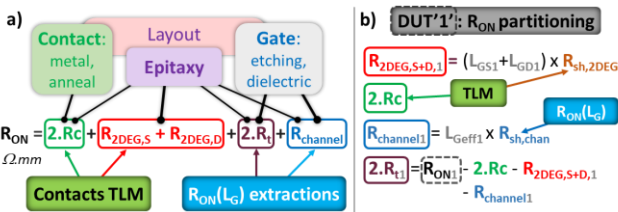


Fig. 4. **a)** R_{ON} partitioning model (with related modules). **b)** Application of the method for a given device (DUT'1'). The four R_{ON} contributions are determined for each die of a given wafer.

Fig. 5a is an example of $I_D(V_G)$ characteristics at room temperature with excellent performance: $V_{th}=+1V$, $SS=88mV/dec$. These curves illustrate the intrinsic gain of this architecture with respect to pGaN gate: gate current is very low ($I_D/I_G > 8$ decades in **Fig. 5a**, and ~ 3 decades for pGaN [3-4]). The

extracted low field mobility μ ($225 cm^2/V/s$) outperforms most published MOS channel HEMT results (see review [11]). Note that MOSc HEMT technology is capable of supporting large V_G , such as 20V (not shown here), which outperforms pGaN. **Fig. 5b** illustrates the linear $R_{ON}(L_{G,eff})$ at $25^\circ C$ and $150^\circ C$. For the smallest gate length device, we report the R_{ON} partitioning for these two temperatures (**Fig. 6a**). One can note that the 2DEG resistance is the main contributor to the total R_{ON} , and shows the largest temperature dependency (**Fig. 6b**). Therefore, for the next device generations 2DEG R_{sheet} reduction and layout (L_{GS} , L_{DG}) have to be carefully considered.

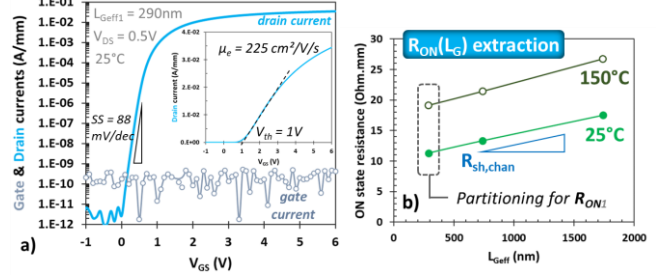


Fig. 5. **a)** Measured drain and gate currents (I_D , I_G) as function of gate voltage V_{GS} in log scale (insert: linear scale for I_D) at $25^\circ C$. **b)** Typical $R_{ON}(L_{G,eff})$ curves at $25^\circ C$ and $150^\circ C$: Measured R_{ON} (at $V_{GS}=+6V$, $V_{DS}=+0.5V$) is plotted as function of effective bottom gate length $L_{G,eff}$.

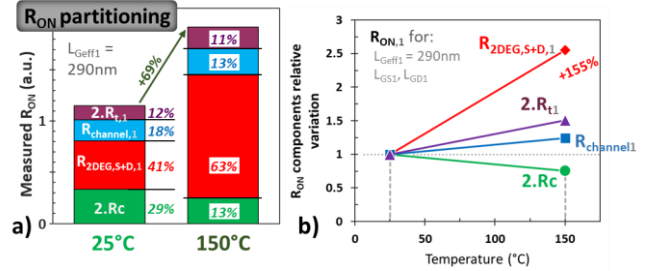


Fig. 6. **a)** Example of R_{ON} partitioning at two temperatures (cf. Fig. 6). For a given device (with fixed L_G , W , L_{GS} , L_{GD}) we determine the four R_{ON} components using the method described in Fig. 5. **b)** Illustration of the temperature relative impact on the four R_{ON} components (for the 290 nm $L_{G,eff}$ device partitioning, Fig. 6a).

B. Advantages of MOSc HEMT R_{ON} temperature behaviour

The considered architecture with fully recessed-gate MOSc-HEMT has the advantage of a smaller R_{ON} temperature coefficient compared to pGaN gate technology. This is detailed and explained in **Figs. 7-8**. We study the influence of temperature on $R_{ON}(L_G)$ and $R_{ON}(L_{GD})$ in **Fig. 7**. $R_{ON}(L_G)$ has a constant slope while $R_{ON}(L_{GD})$ has a temperature dependent slope (**Fig. 7b-c**).

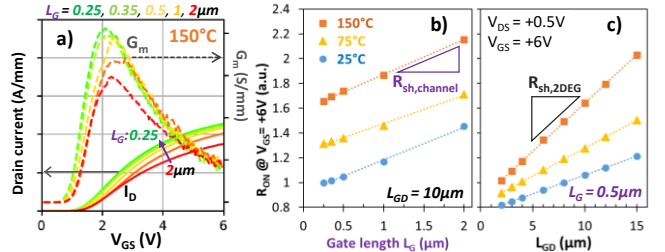


Fig. 7. **a)** $I_D(V_{GS})$ measurements with corresponding transconductance $G_m(V_{GS})$ curves, for different gate lengths L_G at $150^\circ C$ and $V_{DS}=+0.5V$. **b-c)** Impact of gate length L_G and L_{GD} on the On state resistance R_{ON} (extracted at $V_{GS}=+6V$) at $25^\circ C$, $75^\circ C$ and $150^\circ C$ (slopes = $R_{sh,channel}$ and $R_{sh,2DEG}$, see Fig. 2, Fig. 5).

The channel resistance is less sensitive to temperature compared to the 2DEG resistance. **Fig. 8** shows $R_{ON}(T)/R_{ON}(25^\circ\text{C})$ (which is linear with temperature) measured for two L_{GD} values and a comparison with pGaN data [3-4]. The higher pGaN $R_{ON}(150^\circ\text{C})/R_{ON}(25^\circ\text{C})$ ratio value (2.2) is explained by the fact that the major R_{ON} contribution is the 2DEG (no R_{channel} , no R_i) which exhibits a dramatic temperature dependence (2.55 in **Fig. 6b**).

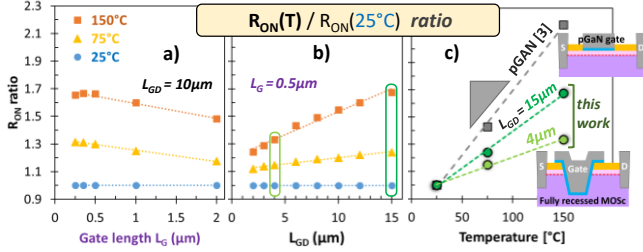


Fig. 8. Impact of gate length L_G (a) and of L_{GD} (b) on the R_{ON} ratio at 75 and 150°C (relative to 25°C), ie. normalized R_{ON} at 25°C . c) Impact of temperature on R_{ON} ratio (and comparison with pGaN gate).

C. Dynamic R_{ON}

Another aspect in R_{ON} studies that needs to be considered is current collapse due to stress. That is why we show dynamic R_{ON} results at room temperature: **Fig. 9** shows $\Delta R_{ON}/R_{ON}$ as a function of recovery time (after a $V_{DS} = +400\text{V}$ stress) for nine different DUT layout designs (**Fig. 10** at $20\mu\text{s}$). We include in these figures an example of comparison between two technological processes: this illustrates that there is a wide process window for performance optimization.

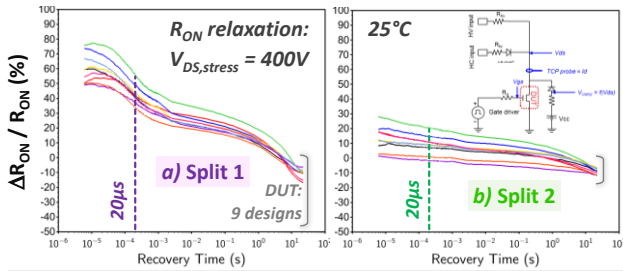


Fig. 9. R_{ON} relaxation transient ($\Delta R_{ON}/R_{ON}$ vs. recovery time, up to 10s) at 25°C for nine layout designs and two technological gate splits (one wafer per split). Insert: Set-up principle. On state conditions: $I_D=0.5\text{A}$, $V_{GS}=+6\text{V}$, pulse time = $175\mu\text{s}$; stress: $t_{\text{stress}}=10\text{s}$, $V_{DS}=400\text{V}$, $V_{GS}=-2\text{V}$.

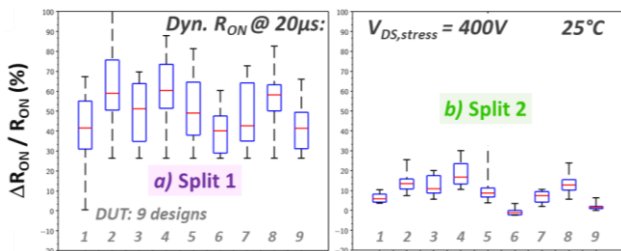


Fig. 10. Box plots for dynamic R_{ON} measurements at 25°C for a $20\mu\text{s}$ recovery time (**Fig. 10**). Nine different layout designs from two technological gate splits (one wafer per split) are compared (left, right).

IV. PACKAGED DEVICES

Once the selected power transistors have been packaged (TO247 as a first test vehicle), we conducted additional static and dynamic electrical tests for 650V applications.

A. Blocking mode, dynamic R_{ON} , capacitances

We measured blocking modes characteristics I_{DSS} and I_{GSS} at 150°C (**Fig. 11**: I_{DSS} and I_{GSS}) for two versions of the process integration. Note that similar measurements have been conducted at the wafer level, with identical conclusions. The I_D reduction (for an unmodified I_G) indicates that the carrier path of the drain leakage current is vertical. One can note that epi and flow optimizations have enabled to improve performance. Moreover this MOS HEMT technology presents similar I_{DSS} values to pGaN performance for much lower I_{GSS} ($0.4\mu\text{A}$ vs. 1mA [3], at $V_{DS}=+600\text{V}$).

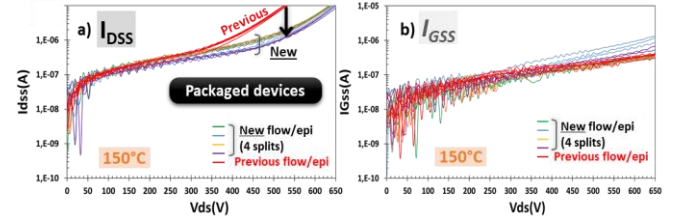


Fig. 11. Blocking mode ($V_{GS} = -2\text{V}$, V_{DS} : 0 to 650V , step 6.5V) measured on packaged past and **new** devices (TO247), I_{DSS} (left) & I_{GSS} (right) measurements at 150°C (three devices per split).

Fig. 12 shows cumulative R_{ON} dynamic measurements. At 25°C we outperform published MIS HEMT data [1], and we report results also at 150°C (which are rarely presented): the dynamic R_{ON} change is limited to $+18\%$ after cumulative V_{DS} stress up to $+400\text{V}$ for our most recent process integration.

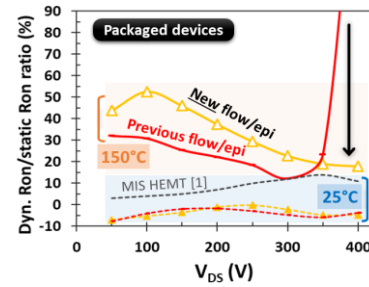


Fig. 12. Cumulative dynamic R_{ON} meas. at 25°C , 150°C for **past** / **new** (TO247 packaged) devices ($V_{GS}=-2\text{V}$, $V_{DS}=50-400\text{V}$, step $+50\text{V}$, $t_{\text{stress}}=10\text{s}$).

Figs. 13 shows the three typical capacitances (C_{ISS} , C_{OSS} , C_{RSS}). We point out the fact that layout modification (L_G , field plates) is a powerful tool to adjust the capacitances (esp. C_{RSS}) to dynamic targets.

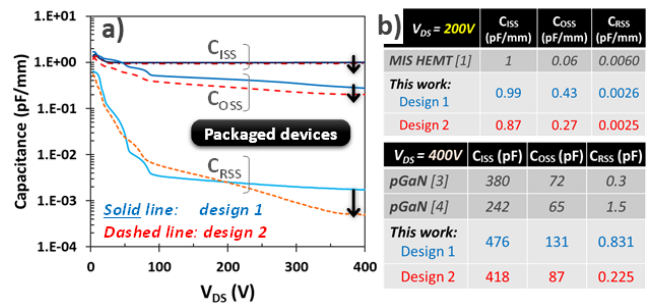


Fig. 13. a) Device C_{ISS} , C_{OSS} , C_{RSS} capacitances measured on packaged devices (TO247) for two layout configurations at 25°C , $\text{freq.}=1\text{MHz}$, $V_{GS}=0\text{V}$. Design 2 (more aggressive layout) shows strong capacitance reduction. b) Summary tables for capacitances measured at $V_{DS}=+200\text{V}$ and $+400\text{V}$ compared to pGaN/MIS HEMT ref.

The C_{ISS}/C_{RSS} ratio at 400V can thus be maximized for canceling parasitic switch ON of low side transistor in half bridge circuits. This ratio is found to be much higher than the pGaN references [3-4]: 1800 vs. 130-160. C_{ISS} corresponds indeed to gate capacitance $C_{GS}+C_{GD}$ which relates, in our architecture, to the MOS gate dielectric thickness (making this parameter an efficient tuning variable).

B. Gate charge, switching results

Relatively high C_{ISS} values implies that a large charge amount is necessary to switch the transistor ON. This effect is visible in **Fig. 14** (Gate charge measurements), and explains why Q_{Gtot} is ~ 2 times larger than pGaN references. One can note that further gate optimization can be applied (dielectric thickness increase) to solve this issue. Another benefit of such an optimization is V_{th} increase.

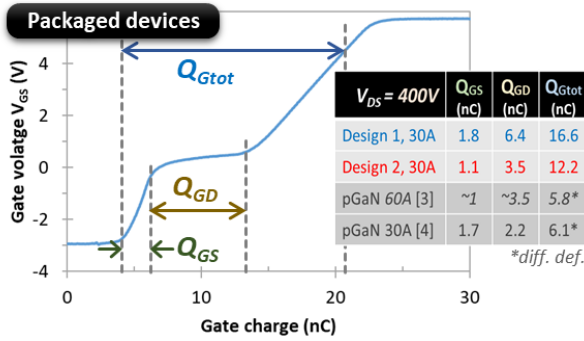


Fig. 14. Gate charge at 25°C, $V_{DS}=400V$, V_{GS} : -3 to +6 V (Q_{Gtot} calculation for 4.5 V). Table: mean values for 5 devices and 2 designs (& references).

Switching tests typically used for analyzing losses in half bridge circuits are shown in **Fig. 15a**. Turn-on switching loss energy (E_{ON}) is dramatically improved ($>63\%$) with our recent integration scheme (not shown here). The switching times $t_{d(on)}$ and $t_{d(off)}$ are also presented (for two designs) and compared to pGaN references (**Fig. 15b**) showing that fully recessed gate outperforms these commercial devices.

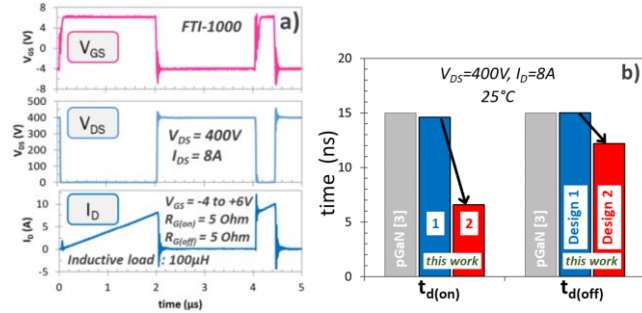


Fig. 15. Switching tests (double pulse 400V, half bridge). a) Typical example (design 1, $I_D=8A$). b) Switching times for the two designs and pGaN references.

V. CONCLUSIONS AND PERSPECTIVES

In this work we present an overview of fully recessed gate AlGaN/GaN MOS channel HEMT from process, integration, advanced characterizations (on wafer) to package level (gate charge, switching...). We investigated the R_{ON} performance through a wide range of characteristics: *i*) the R_{ON} partitioning enables us to highlight the specific role of 2DEG resistance (at 25 and 150°C); *ii*) in particular the comparison with pGaN gate architecture shows a better $R_{ON(T)}/R_{ON}(25^\circ C)$ ratio for MOSc-HEMT, which is critical for power applications. Moreover leakage currents are shown to be largely lower compared to literature: I_D (and I_G) under blocking mode, and I_G in conduction mode (this property is due to the high quality of the gate dielectrics). Packaged devices have also been evaluated for dynamic performance. We showed improved switching characteristics (especially $t_{d(on)}$ and $t_{d(off)}$) compared to pGaN gate devices. All these elements show that MOSc-HEMTs can lead to more efficient and compact power systems.

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