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Design of a small pitch (7.5µm) MWIR MCT array operating at high temperature (130K) with high imaging performances

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ABSTRACT

SWAPc (Size, Weight And Power-cost) is a strong trend in IR imaging systems. It requires focal plane arrays with smaller pixels, operating at high temperatures. For MW systems, the full spectral band (up to 5μ m) shows a strong advantage over the blue band (4.1μ m) as it maximizes the number of incoming photons from a room temperature scene. Few years ago, LETI and Lynred have been developing 7.5µm pitch MCT arrays in MW full band. The first version of this technology was based on n/p diodes operating at 110K maximum temperature. Switching to p/n using extrinsic doping allows today an important gain in dark current, enabling operating temperature up to 130K or even higher. This paper will describe our latest results in the design and fabrication of such HOT small pitch arrays, starting with test chip arrays, followed by the full the characterization of 1280x1024 7.5µm pitch arrays. First order figure of merit (dark current, QE...) are of course considered, but second order figure of merit will also be discussed such as noise tails.

Keywords: IR detector, HgCdTe, small pixel pitch, MWIR, HOT

1. INTRODUCTION

Today's standard mid wave infrared red band (MWr) imaging detector at LYNRED is a TV format (640x512 pixels) with 15µm pixel pitch resulting in a 1cm² class sensor chip. During last years, this pixel pitch has been scaled down to 10µm at Lynred with the outcome of the Daphnis product family [¹] in order to improve spatial resolution. First demonstration of 7.5µm pitch imaging has also been shown at LETI in the last years [²]. When using HgCdTe (MCT), the material cut-off is tailored to get the MW red (MWr) full spectral band $\lambda \in [3; 5]µm$. In that case, the detector operating temperature is usually equal or below 110K for standard technology using mercury vacancies doping (VHg). Indeed, the dark current becomes important at high temperature due to the low minority carrier lifetime of this technology. However, more than the dark current itself, it is the apparition of excess noise pixels that limits the operating temperature of the array: noise defectivity tends to increase at high temperature [³], degrading the image quality of the array. This excess noise is affecting dark current. A first option to improve diode performances is to switch from n/p VHg process to p/n extrinsic doping to gain in dark current due to the improvement in lifetime [⁴]. However, noise distribution tails remain limiting at high temperatures. Moreover, pixel pitch reduction highly constrains the p/n diode process

Infrared Technology and Applications XLVIII, edited by Bjørn F. Andresen, Gabor F. Fulop, Lucy Zheng Proc. of SPIE Vol. 12107, 121070U · © 2022 SPIE · 0277-786X · doi: 10.1117/12.2618852 in terms of alignment, but also in terms of composition and doping profiles management within the collecting junction.

To solve this issue, LETI and LYNRED have been developing a new generation (NG) of p/n MCT diode in order to improve both noise performance and manufacturability to go toward small pixel pitches. This project, supported by French MOD (DGA) and DEFIR joined laboratory aims specifically at developing a technology for small pitch HOT MCT imaging in MWr. The targeted pitch is 7.5µm, for arrays operating at 130K with low noise distribution tails, high stability. Last but not the least, the process offers also a significant gain in manufacturability.

2. BRIEF TECHNOLOGY DESCRIPTION

Broadly speaking, this NG technology is somehow very similar to the previous LETI p/n technology [⁵]. Starting from home made CdZnTe (CZT) 46x48 mm substrates; we grow the absorbing layer by liquid phase epitaxy lattice matched to the substrate in order to ensure an optimal material quality. During the growth, the absorbing layer is N doped in the 1e15 to 1e16 /cm³ range introducing In in the melt. The pn junction is then formed by implanting As, activated with a high temperature bake [⁶]. As usual, the layer is also passivated in order to manage interface recombination [⁷]. Altogether, the NG final diode ends very close to a p/n classical planar diode. It is however much more suitable to small pixel pitch and is expected to exhibit a better behaviour in terms of low frequency noise and noise distribution tail.

3. LAYER CHARACTERIZATION

The first phase of technology optimization consisted in the definition of the process window in terms of absorbing layer properties (material composition, doping level, and passivation). This process window had to be sufficiently robust to allow the fabrication of small pitch high performance diodes (in terms of dark current and quantum efficiency) at a large scale, compatible with a full array. First fabricated test diodes allowed to assess basic detection properties. For instance, Figure 1 shows normalized spectral responses measured on such test diodes at 130K, when rear illuminated through the substrate. The mid response cutoff appears well adjusted to 5µm at 130K as expected. Moreover, the triangular spectral shape (in units homogeneous to A/W) suggests a uniform QE onto the whole MWr spectral band. Due to experimental issues with our QE test bench, the precise measurement of QE was not possible to date with a good precision for those small diodes. However, the level of signal together with the spectral shape suggest a high QE, probably higher than 70%.

Going further, IV-RV performed on some of those diodes shows very comfortable polarisation plateaus at 130K (several volts), as shown in Figure 2 under illumination conditions. This figure shows also clear differences between the eight different diode flavours investigated here. Some designs exhibit leakage current at lower biases than others flavours, thus suggesting a weaker process point. The plain lines stand for diodes in array configuration whereas dashed lines stand for isolated diodes, using the same design as array diodes but with no neighbouring pixels. As can be easily seen, the current obtained in this configuration is ten times higher than array diode. Such a large difference between isolated diode and confined diodes suggests a large lateral diffusion length, i.e. au long minority carrier lifetime, as expected from MCT extrinsically doped material.

Figure 3 gives an analysis of the level of dark currents measured on such test diodes in 7.5µm pixel pitch arrays. The different colours stand for four diode flavours as previously. The dark line also

represents the well-known rule07 while dashed lines stand for the uncertainty associated with rule07. This rule is used as a reference for dark current well-designed MCT diodes [⁸].

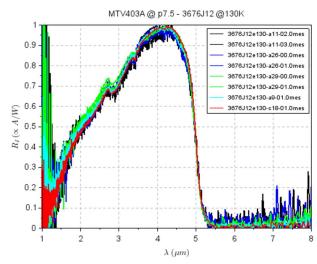


Figure 1 : Spectral responses measured on 7.5µm pitch diodes at 130K

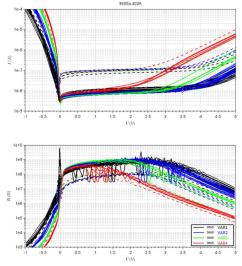


Figure 2 : IV-RV performed on test diodes 7.5µm pitch with different diode flavours (130K under flux)

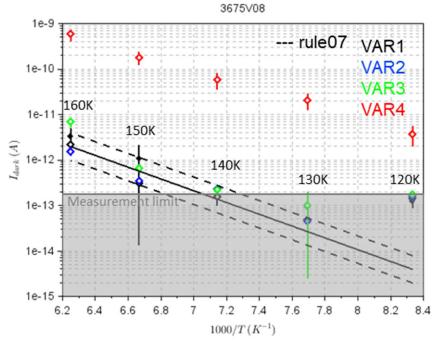


Figure 3 : Dark current measured on 7.5µm test diodes from four different flavours.

Clearly, one diode design appears not optimal, while the other three sit within the rule07 limit. Note that the measurement bench limit is estimated around 0.2pA (shaded area on Figure 3). Given the small size of the diodes test array, the current is very low and measurement are therefore not relevant at temperature 130K and lower.

4. 1ST TEST-ARRAY CHARACTERISATION.

The second phase consisted in the fabrication of arrays using available 15 μ m pitch ROIC (CL258, VGA format 640x512): each ROIC entry was connected the 2x2 super-pixels using classical production hybridization. This allowed the validation of the NG technology for small pixels before the availability of the 7.5 μ m pitch ROIC with p/n polarity. This ROIC is a classical direct injection (DI) input stage used here with a large capacitance (13.6Me-) because initially designed for the LW high flux band. The 2x2 binning is carried out using an extra metal deposition level as depicted in Figure 4.

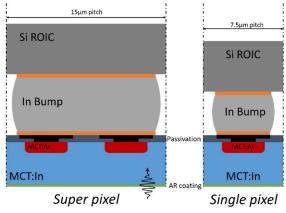


Figure 4 : Super-pixel approach schematic

This approach was very convenient to accelerate the development of the small pitch diode technology. We kept on investigating different diode design with multi-variant hybridized arrays. Figure 5 shows indeed an example of such a study array exhibiting 16 sub-arrays with 8 different diode design investigated. Each design is duplicated two times in a 4x4 chess pattern in order to track eventual non-homogeneities at array level. In details, Figure 5 shows a NETD mapping measured at 130K, F/4 with 20 and 35°C black body exposition. The integration capacitance being very large, the integration time was very long (50ms) to get mid dynamic conditions.

Consequently, the mean NETD is very low, between 7 and 8mK, as expected from a high QE and low noise imaging device in those conditions. Such a long integration time is also interesting here because it highlights any 1/f noise that might appear at high temperature [⁹].

Each sub-array distribution is then extracted and cumulated histograms are plotted separately with different colours (bottom plot in Figure 5). Such a representation allows a quick comparison of the different distributions. Mean distributions are identical, very close to normal distributions. However, the different designs differ in terms of distribution tails: some designs (blue lines) exhibit tails whereas

others show far lower tails (pink and red), in some cases even close to no distribution at all (designs in green).

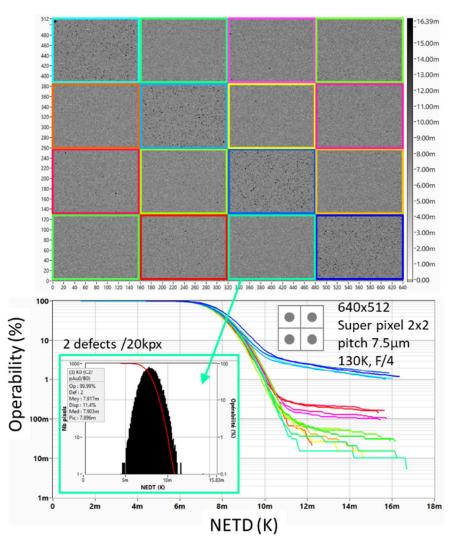


Figure 5 : Example of a NETD mapping performed on a super-pixel array.

Enclosed plot in Figure 5 focuses on the best variant in terms of distribution tail (ie defectivity). With our classical operability criteria, (a pixel is considered as defective if its NETD is larger than the mean NETD by 100%), we get only two defects over 20 000 pixels. This represents a 99.99% operability in NETD at 130K F/4, which is an excellent result at this early stage of development: the noise distribution is almost tail-less at 130K using this specific diode design.

5. SXGA P7.5 CHARACTERISATION

The last phase consisted in the fabrication of a full 7.5 μ m pitch array SXGA format 1280x1024. The new dedicated ROIC will not be described here in details. In few words, it is 1cm²-class digital chip, ITR-IWR, using a DI input stage as well, with different available gains. For this work, the full well used was 1.6Me-, which is more adapted to the MWr band. 7.5 μ m pitch MCT detection circuit were connected onto this Si ROIC using our classical In bump hybridization scaled to this small pitch, already used before for 7.5 μ m pitch n/p arrays [²].

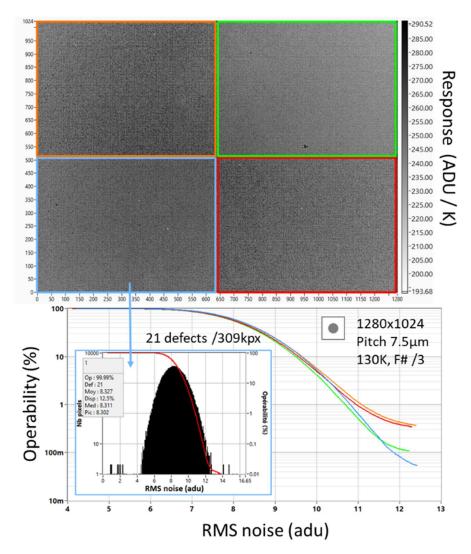


Figure 6: Example of a noise mapping performed at 130K on one of the first HOT SXGA fabricated with a 7.5µm pitch

Figure 6 shows an example of noise measurement carried out on such a SXGA array 7.5 μ m pitch at 130K F/3. This time, only four different designs were investigated, corresponding to the four quarters of the array. A quadratic subtraction of ROIC noise was performed in order to study the diode contribution alone.

As previously, each design is then extracted in order to plot the cumulated distributions and compare it using different colours in the bottom plot of Figure 6. The results are perfectly consistent with previous results from Figure 5 with the super-pixel approach: Noise histograms exhibit low distribution tails at 130K. Some design are even almost tail-free in those characterisation conditions, thus indicating that the low distribution tails measured on super-pixels are not due to tail averaging.

The best design is specifically shown in the enclosed plot of Figure 6. We get a histogram very close to a normal distribution, with a very limited tail. With 100% mean value criteria, we identify only 21 defects over 309 kpx, this time corresponding to 99.99% operability, consistent with data obtained previously on super-pixel arrays.

The same kind of characterization was performed also at 110K. The resulting noise histogram is shown on Figure 7 in log scale, superposed with the 130K noise histogram, separating the two available diode variants (Var1 and Var2, 655 kpixels per variant). In this illumination conditions (f/3 ambient black body), the noise distributions at 110K do not exhibit any tail for both variants. Moreover, this plot shows that such very good noise behaviour is maintained at 130K for Var2 whereas Var1 shows the apparition of low tail.

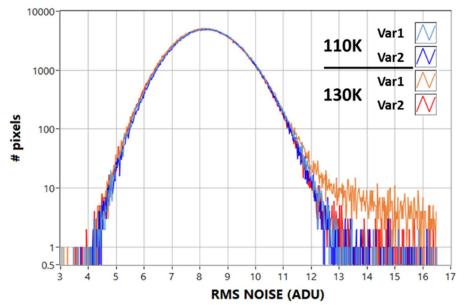


Figure 7 : Superposition of RMS noise distributions measured at 110K and 130K of a 7.5µm pitch HOT SXGA (two diode flavours separated).

The next step is then twofold. Firstly, assess the stability of those diodes, in terms of RTS and RFPN. However, instabilities are usually correlated with the presence of noise distribution tails, which allows to be reasonably optimistic. Secondly, pixel MTF has to be precisely measured. Indeed, with intrinsic doping, 7.5 μ m pitch MTF appeared close to optimum [¹⁰]. In the present case, the extrinsic doping induces longer diffusion lengths, which might slightly degrades pixel MTF for small pixel pitches.

6. CONCLUSION

LETI and Lynred are developing a new generation of MCT based HOT MWr technology, compatible with small pixels pitches. This technology makes use of extrinsic doping for low dark current with a P/N polarity. Demonstration of 7.5µm pitch SXGA is given in this paper, operating at least at 130K F/3. A special attention is devoted to noise tails usually limiting the rise of the operation temperature. In our first arrays, the best diode design exhibits virtually no noise distribution tail at all at 130K. Extra measurements at even higher temperatures (140 and even 150K) are expected in a near future to see the real limit of this technology in terms of operating temperature. The next steps will be the assessment of stability performances on such arrays (measurement of RFPN and RTS at high temperature) and measurement of MTF for such small diodes.

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