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A 7.4µW and 860µm² per channel cryo-CMOS IC for 70-channel frequency-multiplexed µs-readout of semiconductor qubits

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Large-scale quantum computing holds promise for exponentially faster computation speed to address currently unsolvable problems. Nevertheless, biasing, driving and reading numerous physical qubits operating at cryogenic temperature remains an on-going challenge. In particular, the integration of cryogenic control and readout ICs appears mandatory to overcome the wiring bottleneck [1, 2, 3]. In this regard, the promising higher operating temperature (up to 1K) of silicon semiconductor qubits offers a more substantial cryogenic power budget, which could enable addressing larger qubit arrays with integrated cryogenic CMOS electronics. In the context of 100,000 qubits at 1K, the maximum power consumption allowed by cooling capability is about 1W within a compact footprint of just a few cm², defining targets of <10µW/qubit consumption and <0.01mm²/qubit footprint. Focusing on the readout IC, the semiconductor-qubit coherence time also imposes a typical <100µs readout time, while requiring a Bit Error Rate (BER) below 10^{-3}.

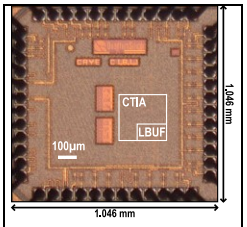
Reflectometry, in conjunction with a frequency-division multiplexing (FDM) technique, has been proposed as a potential solution [1, 2, 3]. However, the footprint of associated passive inductors and/or the need of intermediary frequencies (IF) remain impractical for addressing large-scale arrays of qubits. Additionally, the resonator quality factor introduces a strong tradeoff between spectral selection and reading time (T_i). To overcome these issues, charge-based readouts using cryogenic transimpedance amplifiers (TIA) or current integrators were proposed by [4, 5]. Nevertheless, existing implementations still face limitations in terms of gain [4] (<80dB.Ω), or are not compatible with FDM [5]. Moreover, they offer no answer to solve the wiring bottleneck issue.

Taking inspiration from [6], this paper introduces a tunable FDM-capable cryogenic capacitive feedback TIA (CTIA) in FDSOI 28nm CMOS technology for reading simultaneously up to 70 channels in a charge-readout scheme with an external direct IQ conversion.

Figure 1 depicts the circuit architecture of the proposed CTIA for FDM charge readout. The MHz range CTIA input current is either coming from co-integrated single electron transistors (SET) or from emulated current stimuli (I_{in}). In a SET configuration, the modulation of the SET gates at different frequencies, with a frequency separation (ΔF), results in On-Off Keying (OOK) sub-nA signals depending on the electrostatic charge environment reflecting the qubit state information. The sum of all OOK current signals (ISUM) is amplified and converted into a voltage (VTIA) through the CTIA. Then, the voltage is sent to RT via an integrated line buffer (LBUF). At RT, digitization and demodulation of N multiplexed frequencies yield N (I, Q) components representing simultaneously the N quantum states.

Figure 2 presents the schematics of the proposed tunable CTIA and LBUF. In contrast to [6], OPAMP1 is a two-stage opamp. The V_{CM} bias is provided by current mirrors, which also provide a DC path for the input current. As capacitive feedback does not set the DC feedback, a local common mode feedback is introduced. To drive the large M0 gate capacitance without instability, the OPAMP1 second stage is designed as a common drain stage. LBUF, on the other hand, is a two-stage opamp source follower responsible for driving the capacitance of the output wiring from cryogenic temperature to RT (typically ~300pF). Rather than relying on conventional temperature-dependent passive Miller compensation that could lead to instabilities at cryogenic temperature, LBUF has been designed to use the output wire capacitance itself as a compensation.

Figure 3 shows the CTIA performances at 4.2K measured with a 1nA input current source and facing a 40fF parasitic input capacitance.



Die micrograph.

By adjusting the tunable passives elements (C1, C2, RD) to obtain a gain of 101dB.Ω, a bandwidth of 50MHz and a noise level of 130fA/√Hz are achieved. The power consumptions of the CTIA and LBUF are 180µW and 330µW respectively. As depicted, tuning C1 and C2 allows a tradeoff between gain and bandwidth without affecting the CTIA power consumption, illustrating its flexibility for scaling and its adaptability to specific SET characteristics. RD and biasing currents are used to account for thermal effects. Besides, FDSOI allows independent NMOS and PMOS back-gate biasing (VBGN=1V, VBGP=-2.3V) in order to compensate for the temperature shifts of V_{TH}, ensuring that the targeted operating point is maintained. Unlike prior works on cryogenic integrated charge readout architectures (Fig. 5) our CTIA exhibits, >100dB.Ω gain, and <1mW power consumption, while reaching >10MHz bandwidth and achieving comparable noise performances. Thereby it meets all the necessary specifications for a FDM scalable charge-based readout.

Figure 4 illustrates the readout performances achieved with our proposed FDM readout. Given our noise level, when reading a single 1nA signal at 10 MHz, the required reading times are respectively 6µs and 8.5µs to reach a BER of 10^{-3} and of 10^{-4}. The reading time to reach a signal-to-noise ratio of 1 (t_{min}) has been extrapolated to t_{min}=125ns from our 4.2K measurements, which is 16x shorter than [1]. To study the crosstalk between channels, we introduced a second channel and measured the reached BER depending on the frequency separation ΔF between both, for a given reading time. For $\Delta F > 2/T_i$, crosstalk becomes negligible compared to the noise level and the BER decreases down to the single-channel case. While $\Delta F = 1/T_i$ could be reached according to the orthogonal FDM (OFDM) principle, we were limited by our RT demultiplexing instruments baseband filter. Two IQ constellations {1} and {2} are shown for two values of frequency spacing, highlighting the crosstalk for ΔF below the second orthogonal frequency. Our readout chain demonstrates operation near the OFDM limit, which is not attained by [1, 2, 3] due to their limited resonators Q factors. With a bandwidth of 50MHz and a reading time of 6µs to achieve a 99.9% fidelity, the proposed CTIA could read 166 channels. Our circuit is no longer limited by frequency separation and in practice the I_{IN}1dB=70nA compression point at 1dB achieved by LBUF yields 70 channels. Fig. 5 presents a frequency distribution example for an FDM readout of 12 channels with a 438kHz channel spacing (chosen to prevent FFT aliasing).

Figure 6 compares our alternative multiplexed readout with state of the art cryo-CMOS reflectometry. A first-order extrapolation of power consumption and number of channels yields a power efficiency of 7.4µW/channel, which is a 11x improvement compared to [1, 2, 3], as illustrated in Fig. 5. A footprint efficiency of 860µm²/channel has been achieved, which is a 2.3x improvement. Furthermore, our circuit eliminates bulky resonators, which constitutes a major advantage for scalable qubit readout. Our readout circuit demonstrates the capability to simultaneously read 70 channels within the aforementioned budgets of <10µW/qubit power consumption and <0.01mm²/qubit footprint, which represent a significant advancement for large-scale readout of semiconductor qubits.

Acknowledgement:

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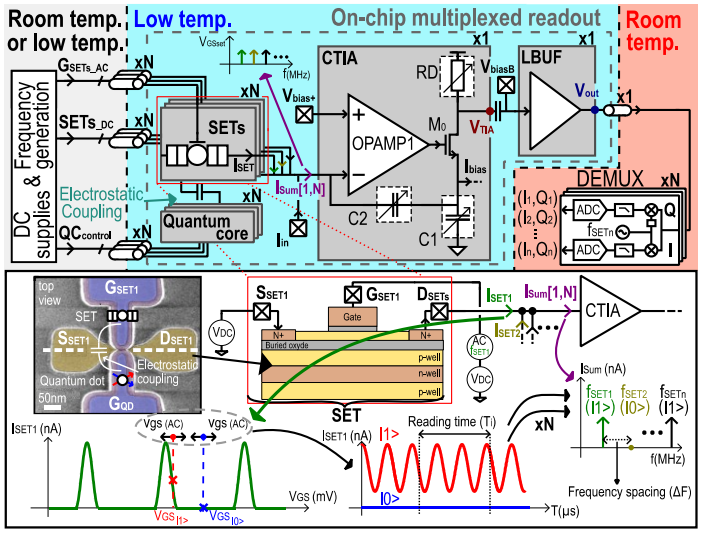


Fig. 1. Block diagram of the proposed frequency multiplexed readout, illustrating the temperature repartition of the system and the signal generation using charge sensing and SET.

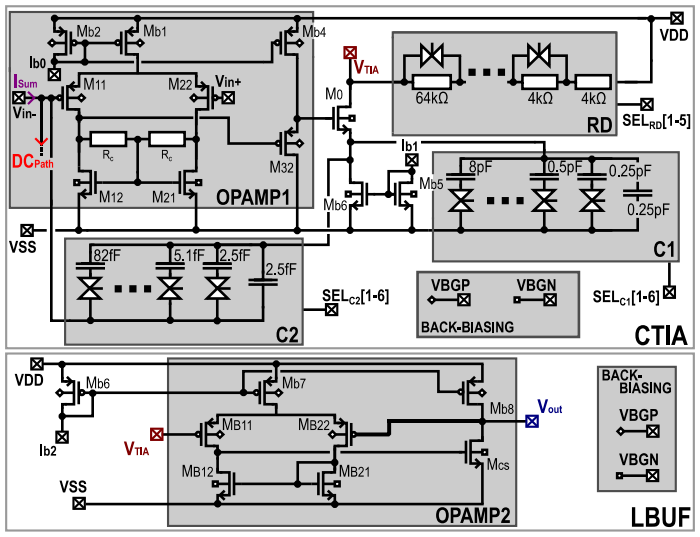


Fig. 2. Transistor level schematics of the proposed main blocks: capacitive feedback TIA (CTIA) with programmable capacitors and resistors and two-stage buffer (LBUF).

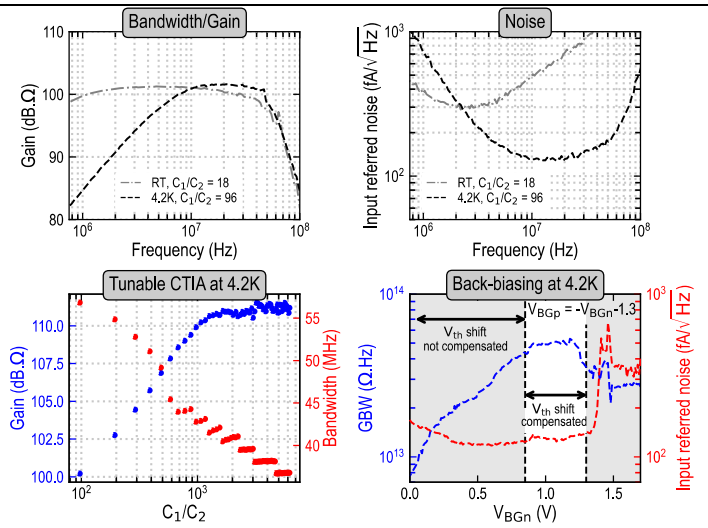


Fig. 3. Measured CTIA characteristics with I_{in}=1nA for room and cryogenic temperature (RT & 4.2K): gain and noise. Gain and bandwidth depending on programmable capacitors. Effect of the back-biasing on the GBW and input referred noise.

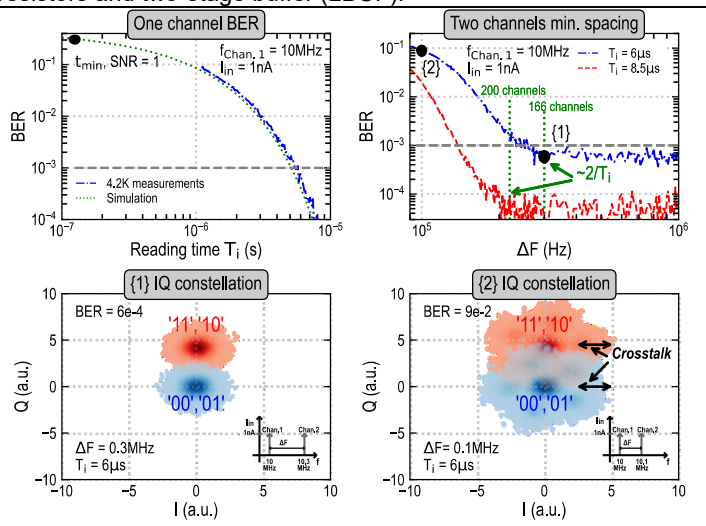
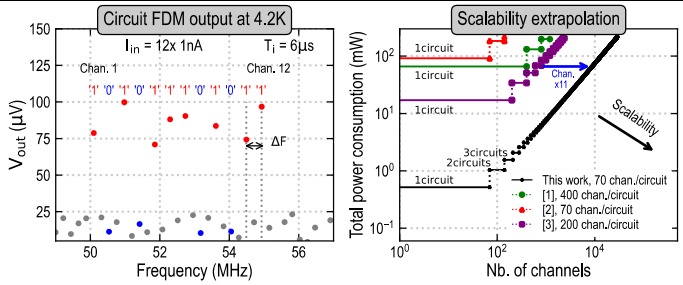


Fig. 4. Bit Error Rate (BER) measured at 4.2K depending on the reading time (T_i) and the frequency spacing (ΔF). IQ constellations of the output states for 2 values of frequency spacing with 2 channels, showing the effect of crosstalk for small ΔF.



	EDL 2019 [4]	VLSI 2022 [5]	This work	Unit
Topology	Inverter-based TIA	Integrator + CDS Amp.	Capacitive TIA	-
FDMA capability	**Yes**	No	**Yes**	-
Power	3.1	**0.064**	0.518	mW
Readout time @99.9% fidelity[c]	N. R.	**0.7**	6	μs
Bandwidth	**5,000**	1[b]	50	MHz
Gain	80	**160**[a]	101	dB.Ω
Footprint	N. R.	80,000	**60,000**	μm²

[a] Estimated with T_i = 1μs and considering the CDS amplifier. [c] For a 1nA input signal.
[b] Estimated from data.

Fig. 5. Measured output voltage of the circuit at 4.2K and predicted evolution of the addressable number of channels depending on the available power consumption for readout. Comparison table of state of the art circuits dedicated to charge readout of quantum devices.

	ISSCC 2021 [1]	ISSCC 2021 [2]	CICC 2023 [3]	This work	Unit
Reading type	Reflectometry	Reflectometry	Reflectometry	Charge readout	-
Temperature	4.2	3.5	4	4.2	K
Off-chip components at cryogenic temp.	Directionnal coupler, LNA	Directionnal coupler	Directionnal coupler	**No**	-
Architecture	Intermediate IF I/Q	Intermediate IF I/Q	Intermediate IF I/Q	**Direct I/Q**	-
Footprint	0.68[c]	2.10[c,e,f]	0.81[c]	**0.06**	mm²
Power consumption	66.0	92[e]	17.1	**0.518**	mW
Bandwidth	**2,000**	1,400	**2,000**	50	MHz
Channel frequency spacing	5	10	10	**0.3**	MHz
t_{min}[b]	1.96	N. R.	N. R.	**0.125**	μs
P1dB / I_{IN}1dB[d]	-58.4 / -	-85 / -	-81 / -	- / 70	dBm/nA
Nb. of channels limiting factor	Resonators Q factor	Resonators Q factor	Resonators Q factor	Buffer linearity	-
Channels/circuit	**400**	70	200	70 / 166[a]	-
Power/channel	0.16	1.31	0.085	**0.0074**	mW
Footprint/channel	2,000[c]+Resonator	30,000[c]+Resonator	4,050[c]+Resonator	**860**	μm²

[a] Without considering the I_{IN}1dB limitation.
[b] With t_{min} the required reading time to reach SNR = 1.
[c] Reported data that doesn't consider passive resonator footprints and discrete cryogenic electronics.
[d] I_{IN}1dB the maximal input current for a 1dB gain loss.
[e] Excluding on-chip signal generation (VCO, PLL).
[f] Estimated from chip micrograph.

Fig. 6. Comparison table of state of the art readout circuits for multiplexed-oriented qubit readout at cryogenic temperature.