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► To cite this version:

Alexis Divay, Cedric Dehos, Jasmina Antonijevic, Ismael Charlet, Joycelyn Hai, et al.. A methodology to address RF aging of 40nm CMOS PA cells under 5G mmW modulation profiles. IRPS 2024 - 2024 IEEE International Reliability Physics Symposium, Apr 2024, Dallas, United States. pp.1, 10.1109/IRPS48228.2024.10529462 . cea-04557422

HAL Id: cea-04557422

<https://cea.hal.science/cea-04557422v1>

Submitted on 24 Apr 2024

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A Methodology to address RF aging of 40nm CMOS PA cells under 5G mmW modulation profiles

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Abstract— A simplified methodology to link CW (Continuous Wave) RF stresses to complex mission profiles is presented in order to compare the lifetimes of different 40nm PDSOI Power Amplifier (PA) cells, versus bias and under different 5G-FR2 modulation profiles. The best lifetime is achieved when using the most complex 5G modulation due to output power/linearity constraints. V_T drift correction is also identified as a powerful tool to increase transistor HCI lifetime under PA operation.

Keywords— RF reliability, mmWave, 5G-FR2 modulation.

I. INTRODUCTION

RFSOI devices meet the 5G millimeter-wave performance criteria while keeping low costs and high integration compared to concurrent technologies [1, 2]. However, the reliability study of these devices under RF operation is difficult to address due to the complexity and variability of the mission profiles [3]. The standard approach based on waveform analysis requires an important SPICE modeling effort to ensure accurate waveform extraction and avoid inaccuracies in lifetime estimation [4], while other methodologies use the DC and RF interplay [5]. This paper proposes an analysis of PA cells HCI degradation at 28GHz using a simplified methodology to link RF CW stresses with 5G-FR2 mission profiles without the need for highly accurate SPICE model and lengthy stress measurements under modulation. The first part describes the PA cells performance and preliminary reliability investigations. The second part investigates transistors RF HCI degradation and a solution to increase their lifetime. The final part compares the performance/reliability trade-off of different PA cells with and without our degradation mitigation technique.

II. DEVICE AND STRESS PROCEDURE DESCRIPTION

The test structures consist in PDSOI PA cells using $W=400\mu\text{m}$, $L_g=40\text{nm}$ GO1 transistors, fabricated in *SOIMMW* technology of STMicroelectronics [1]. A stand-alone (SA) transistor and two stacked cells were analyzed (Fig. 1). All structures have a sense measurement on the output side to ensure the correction of eventual voltage drop in the measurement setup and to monitor the probe contact resistance (R_c) during stress,

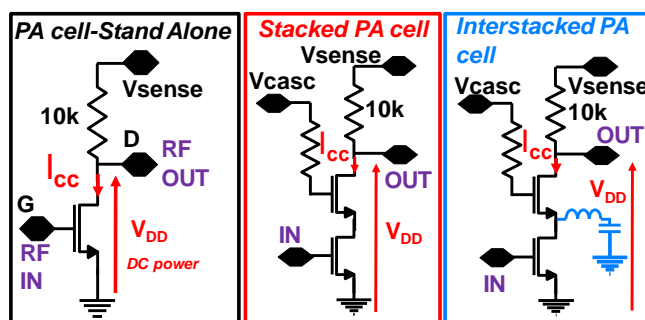


Fig. 1. PA Cells tested: Stand-Alone Common-Source transistor (SA), Stack (Two GO1 stacked) and Interstack (stacked with LC circuit).

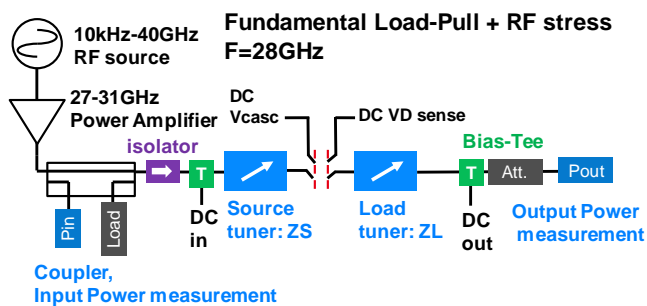


Fig. 2. Load-Pull setup used for RF CW stresses.

which is crucial for accurate RF degradation estimation [6]. The PA cells mmWave large signal measurement and RF stress was measured at $F=28\text{GHz}$ using a fundamental Load-Pull setup (Fig. 2). The DELTA tuners (from Focus Microwaves) are directly connected to the RF probes for optimal impedance coverage. The RF stresses follow a stress-measure-stress methodology: DC parameters are monitored (V_T , R_D , I_{Dsat}), probe contact resistance, 8dB back-off gain ($\text{Gain}_{BO} @ P_{out}=P_{1dB}-8\text{dB}$), as well as DC & RF parameters at stress conditions (Gain, PAE, I_D , I_G , I_{Casc} for stacked structures). A power sweep under stress bias conditions (I_{Dq} , $V_{DDstress}$) is performed before and after stress. A final power sweep is done afterwards, with an automatic I_{Dq} drift correction using V_G (V_T correction).

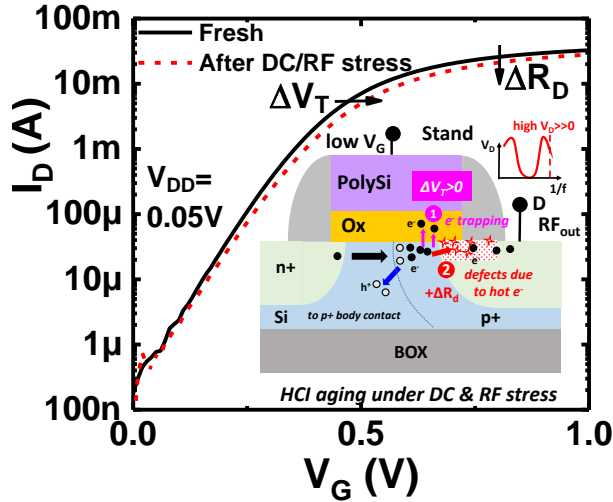


Fig. 3. Linear $I_D(V_G)$ degradation under RF CW stress: V_T and R_D increase caused by respectively electron trapping in gate oxide and defect creation in drain access area due to hot electrons.

Similar to our previous work, if a PA cell presents a contact resistance drift ΔR_C superior to 100m Ω , the test is disregarded as the measured RF degradation cannot be distinguished from the drift due to a degraded probe contact. As we have observed in our previous studies, the PA cell degradation is mostly visible in the back-off region compared to compression. Furthermore, in the 5G-FR2 modulations considered in this work, most of the PA mission profile is spent around 8dB back-off from P_{1dB} . The back-off gain is then considered as one of the critical degradation metric for our PA cells. As CW RF stresses on wafer are difficult to operate for long times (>10/20h) with minimal probe contact issues, it is even more difficult to perform RF stresses under modulation. These tests necessitate Arbitrary Waveform Generators and costly Load-Pull systems. The latter are generally not suitable when handling wideband modulation signals as the passive tuners impedance are only defined for a very narrow frequency band. Active tuners allows to perform Load-Pull measurements using modulated signals but are generally less versatile compared to passive tuners (frequency range and harmonics control for instance). Furthermore, modulated signals present a low mean power level which increases stress time. Long stresses under modulation should then be reserved to packaged chips. A simple methodology to link such RF CW stresses to a behavior under modulation would help reliability engineers to quickly assess the DUT RF degradation depending on its mission profile.

III. DATA/RESULTS AND DISCUSSION

A. Degradation modeling

To better model the device degradation, we first analyzed the Stand-Alone (SA) degradation under DC Hot Carrier stress coupled with S-parameters measurements (Fig. 3 & Fig. 4). Comparable to our previous work on 60nm devices [7], hot electrons are generated near the drain during stress and are either trapped in the oxide (ΔV_T) or will create defects responsible for R_D increase.

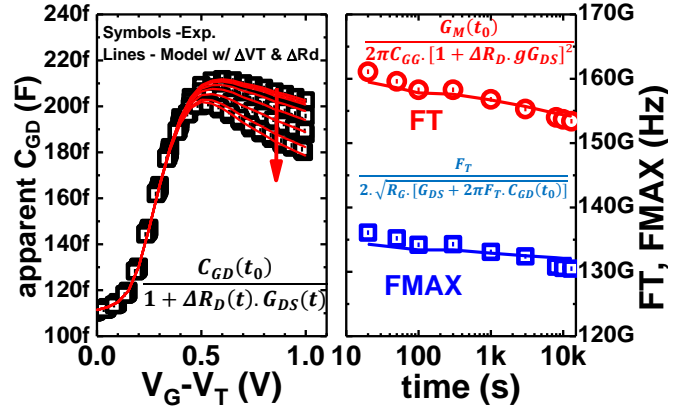


Fig. 4. Modeling of DC & RF degradation on Stand-Alone MOS device under DC HCI stress: $V_G=0.6V$, $V_D=1.5V$. All DC and RF parameter can be modeled using only ΔV_T and ΔR_D .

The apparent C_{GD} is reduced with stress (C_{GD} extracted using the standard MOSFET small-signal model) but keeping intrinsic C_{GD} constant and adapting the small-signal equivalent model to include ΔR_D models accurately the observed degradation. The key RF transistor figures of merit FT & FMAX decrease with HCI stress, especially due to the R_D rise as V_T degradation only shifts the FT(V_G) & FMAX(V_G) curves towards higher voltages. The extraction is then performed at constant overdrive $V_G - V_T(t)$. These DC parameters (V_{Tsat} , R_D) will be followed during RF stresses afterwards, to create a device aging model under PA operation. The RF stress conditions used in this study are presented in Table 1, with a combination of different V_{DD} bias and output power under CW RF stress to evaluate the performance/reliability compromise of the different PA cells. The source and load impedances (Z_S & Z_L) are optimized for each DUT and bias point in order to have the desired performance: below the 1dB compression point (P_{1dB}), Z_L is optimized to have less than 0.5dB Gain increase due to class AB operation, which is essential to avoid signal distortion under modulation.

TABLE 1. RF STRESS CONDITIONS USED IN THIS STUDY.

Structure	VDD	Stress@ P_{out}	T
Stand-Alone	0.9V, 1V, 1.1V	4 conditions, between P_{1dB} -1dBm & P_{2dB}	25°C
Stand-Alone	1.3V	Pout below parasitic bipolar triggering (RF TDDB)	125°C
Stand-Alone	1V	Duty cycle 15, 40 & 60% @14 & 16.2dBm	25°C
Stand-Alone	1.1V	14, 15, 15.7, 16.4 & 17dBm	25°C
Stack	VDD 2V, Vcasc 1.5V	17dBm (P_{2dB})	25°C
Interstack	VDD 2V, Vcasc 1.5V	16, 16.5, 17, 17.5dBm	25°C
Interstack	VDD 1.8V, Vcasc 1.35V	15, 15.2, 15.5, 15.8dBm	25°C

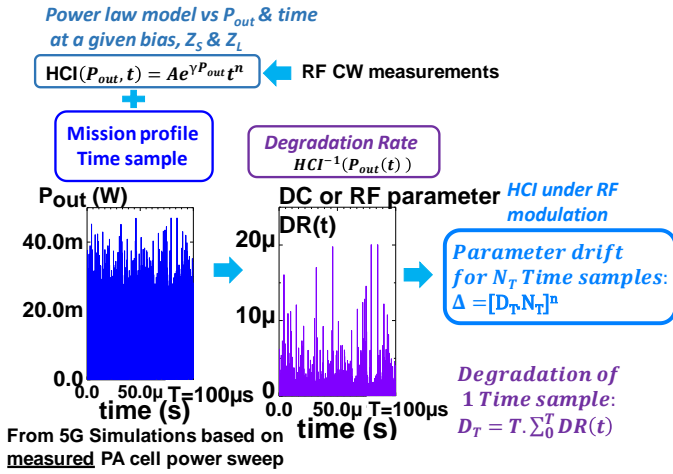


Fig. 5. RF reliability methodology, using P_{out} as principal parameter. PA cell degradation models are based on CW RF stresses. The mission profile $P_{out}(t)$ is extracted through simulation and measured power sweeps. Quasi-static approximation is finally used for DC & RF parameter drift calculation. Load-Pull setup used for RF CW stresses.

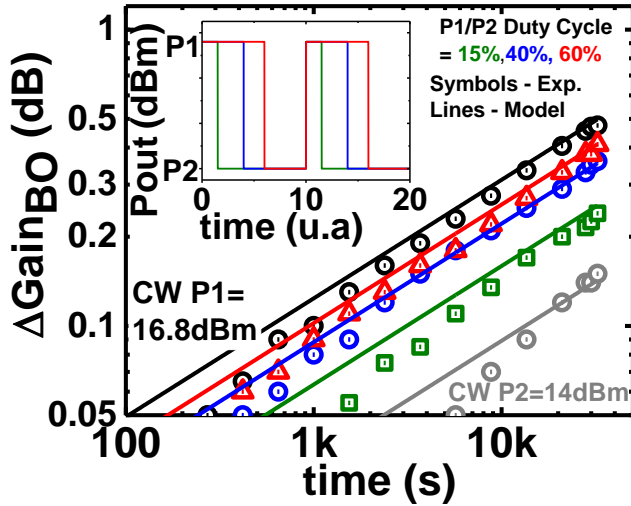


Fig. 6. Combination of RF stresses between two power levels with different duty cycles. The total degradation is well modeled using quasi-static approximation, validating the approach for more complex modulation profiles.

The common methodology to assess device RF reliability is based on (V_G, V_D) waveform extraction using SPICE simulation. This technique is very powerful as it offers the possibility to model the degradation for any bias, impedance and power level. However, as the technology node is shrinking, the HCI voltages accelerations tremendously increases. A small error in the SPICE model (a few tenth of a dB on the PA Gain for instance) will be translated to an error in the waveform and by extension to the device lifetime [4]. As the PA complexity increases, such as several stages and parallel branches, SPICE errors will stack and lifetime estimation will be even more prone to errors. We then based our degradation modeling directly on RF CW stresses (Fig. 5). Such a “Product-based” approach is straightforward, and, overcomes the main limitations of the former MHC frameworks [4,5]. Moreover, another advantage of this approach is that, it can be applied at different DUT scales, ranging from single PA cell to a complete PA product, and even at the Front

End Module level. Based on CW RF stresses, the DC and RF parameters drifts due to RF HCI are modeled using a power law versus time and an exponential model versus P_{out} (namely V_T , R_D and Gain_{BO}). The DUT power sweep (Gain & PAE vs P_{in} or P_{out}) is modeled using a spline or a polynomial and serves as a transfer function for 5G-FR2 modulation simulations. We then retrieve a 100 μ s sample of instantaneous P_{out} versus time from these simulations. This sample length is chosen to be representative of the power distribution of a given modulation profile over time, with a very fine sampling. Using the RF HCI model, we then calculate the degradation rate over the whole $P_{out}(t)$ sample and finally, the parameter drift under modulation is estimated. We validated our approach based on an Age model & quasi-static approximation, using a simple textbook case combining 2 output power levels P1 & P2 at different duty cycles (Fig. 6). Note that, so far the model parameters are only valid at a given V_{DD} and source/load impedance, but an extension is under development.

B. Stand-Alone RF stress

The Stand-Alone PA cell degradation under CW RF stress is then modeled using three distinct parameters: 8dB back-off Gain (Gain_{BO}), V_{Tsat} and R_D (Fig. 7).

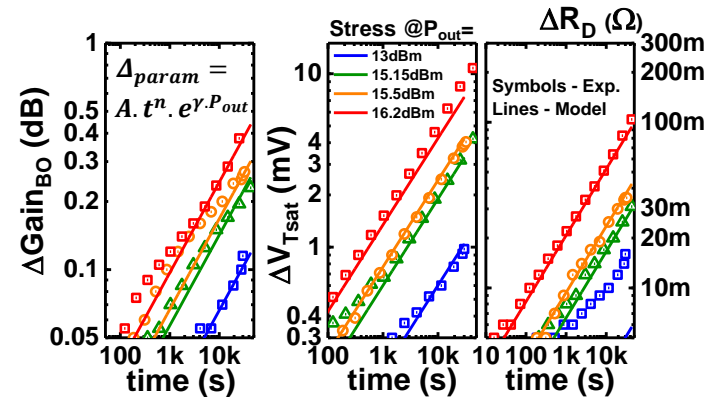


Fig. 7. Back-off gain, V_{Tsat} and R_D degradation modelling under RF CW stress versus P_{out} on SA device for $V_{DD}=1V$.

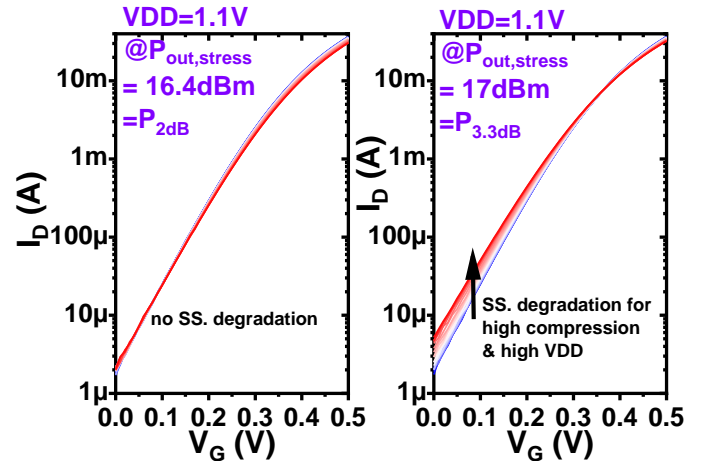


Fig. 8. $I_D(V_G)$ during RF CW stress for high V_{DD} and high power (2dB & 3.3dB compression). Large Sub-threshold slope degradation is observed above 2dB compression.

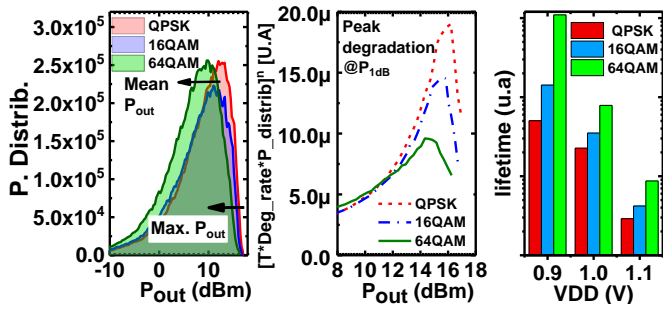


Fig. 9. a) Stand-Alone device Power distribution of the considered modulation profiles. b) Associated degradation rate based on RF CW stresses versus P_{out} , critical aging occurs around P_{1dB} . c) Estimated lifetime versus modulation profile and V_{DD} .

These three parameters are modeled accurately across the P_{out} area of interest (around $P_{1dB} \pm 1dB$) for a nominal V_{DD} and $T=25^\circ C$. The time slope is around $n \sim 0.4$. Care should be taken when specifying RF stress conditions for accurate lifetime modeling as too harsh conditions may trigger a different degradation mechanism. Indeed, at nominal $V_{DD} + 10\%$ (1.1V) and 3.3dB compression (0.5dB above the maximum P_{out} level under 5G modulation in our case), the sub-threshold slope is degraded (Fig. 8). Such effect is not observed for lower power levels, which are more compatible with 5G linearity constraints (especially for higher modulation orders). Three different 5G-FR2 modulation profiles were considered in this study with increasing modulation order & various Peak to Average Power Ratios (PAPR): QPSK, 16QAM & 64QAM. Different input power back-offs are considered depending on the modulation scheme, in order to match the Error Vector Magnitude (EVM) and spectrum mask constraints from 5G-FR2. Indeed, PA input signal is fed stronger for the lower order modulation scheme (QPSK), that has lower Peak to Average Power Ratio (PAPR) and less severe EVM constraints (Fig. 9). Indeed, the PA cannot reach too high compression, which would strongly degrade the EVM. Combining our RF HCI model with the 5G power distributions, we observe that there is a compromise between total time spent at a given P_{out} and the associated degradation rate, with a critical peak degradation around P_{1dB} . This supports the choice of our RF stress power range in our degradation modeling. QPSK presents a much higher degradation peak compared to QAM modulations as the signal can be fed at higher power level. Indeed, with 4 symbols, the EVM requirements are much less severe (15.5% maximum EVM) compared to 64QAM (8%). The difference in power distribution result in an increase in the DUT lifetime with modulation complexity, as the DUT spends more time at lower P_{out} . In our study, we have defined the PA fail condition with a -1dB drift in $Gain_{BO}$. We have modeled the SA transistor RF HCI lifetime at different V_{DD} to estimate its best performance/reliability compromise. Above nominal V_{DD} (nominal=1V), the SA lifetime is strongly reduced. If power constraints are not too high, a 10% derating on V_{DD} allows to increase its lifetime, with a large effect estimated for 64QAM modulation (combination of low mean power and low V_{DD}). Moreover, as depicted in Fig. 3, RF stress shifts V_T and R_D rises, thereby decreasing the quiescent drain current I_{Dq} and $Gain_{BO}$ accordingly.

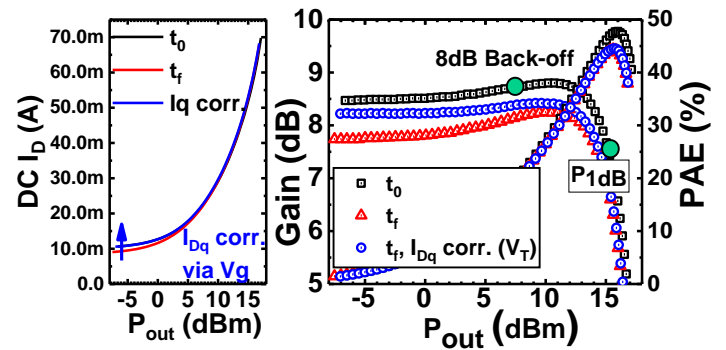


Fig. 10. Stand-Alone RF large signal performance before, after stress and using V_T correction after stress to recover part of the degradation.

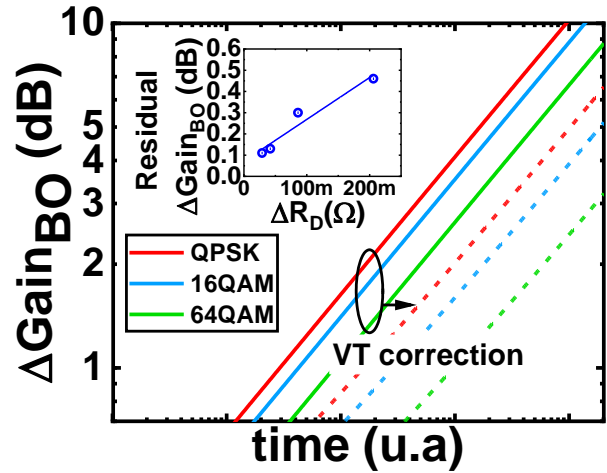


Fig. 11. Estimation of PA cell lifetime extension using V_T correction allowing a better performance/reliability compromise regarding HCI degradation.

Indeed, as I_{Dq} decreases, the PA class of operation is driven towards class B and lower gain (further apart from high g_m). Correcting the bias current to its initial value using V_G allows then to recover almost half of the gain degradation (Fig. 11). Around compression, the observed degradation is less visible as the PA is mostly driven by its output impedance. Indeed, such relatively small variation in I_{Dq} has a low effect on P_{1dB} & PAE_{max} compared to small-signal regime. These parameters degradation may still be modeled versus P_{out} in the same way as $Gain_{BO}$ but the latter is clearly identified as the critical bottleneck in this study. Moreover, as we have seen on the modulated power distributions, most of the time the amplifier is driven around its back-off level. A shift in compression will only be seen for the symbols needing high power, the overall PA performance under modulation will not be highly impacted. As ΔR_D cannot be recovered, we estimated the RF degradation that we would obtain by correcting V_T on the fly during stress, with only the R_D impact (Fig. 11). We first extracted the residual $\Delta Gain_{BO}$ using V_T correction based on the V_T -corrected power sweep after RF CW stress. We can then extract a linear dependence between ΔR_D obtained at a specific stress P_{out} and the residual RF degradation associated. By coupling this result with the estimated R_D drift under modulation, we estimated the lifetime under 5G modulation using V_T correction. This

mitigation technique demonstrates an improvement up to one decade on the DUT lifetime.

C. Stacked cells RF stress

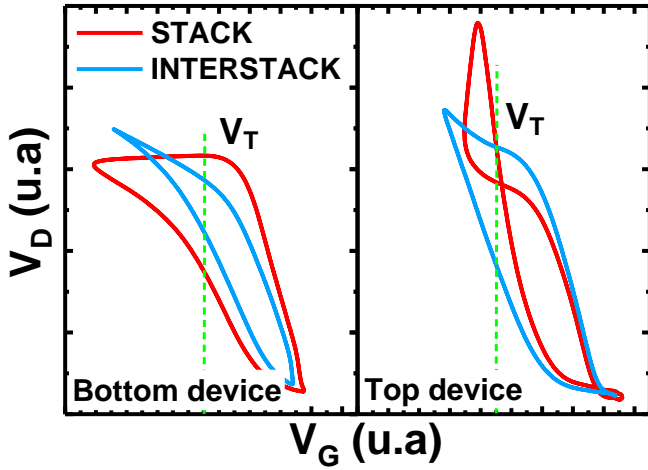


Fig. 12. Simulated waveforms for top & bottom devices @ P_{1dB} for Stack & Interstack devices. Stack cell top transistor has higher peak voltage.

The same methodology was applied on stacked PA cells (Stacked and Interstacked). The source and load impedances were chosen to obtain the same RF large signal performance between the two cells. We simulated the (V_G, V_D) waveforms for both bottom (common-source) and top transistors (common-gate), at P_{1dB} with standard V_{DD} and their optimum source and load impedances (Fig. 12) to better understand the cells core degradations (at transistor level). The stacked cell common-source transistor is showing a higher drain voltage for most of the RF cycle and the common-gate suffers a high voltage peak just below threshold. These DUT were subjected to CW RF stresses at P_{2dB} during 9 hours. During the stress, we extracted the V_T of each transistor by sweeping either V_G or V_{casc} (Fig. 13). The conventional stacked PA cell is the most degraded, especially its common-gate transistor as it is subjected to a severe peak drain voltage compared to its common-source. On the other hand, the Interstacked cell integrates a decoupling LC network to balance the voltage between the bottom and the top transistors, resulting in a general lower cell degradation. As the top transistor is the most degraded, we applied the V_T correction technique on the V_{casc} node, which mitigates only a marginal part of the degradation. This kind of PA cell might be more sensitive to RF drift mitigation by using the common-source transistor at the bottom (V_G correction) even if it is less degraded. The estimated performance-lifetime trade-off between both cells (SA and Interstack) under 64QAM modulation is presented in Fig. 14. Regarding HCI degradation, Stand-Alone can be competitive versus Interstack if V_T correction is applied during its lifetime, the cascode voltage correction being marginal for Interstack. This stacked cell's performance can be boosted with $V_{DD}=2V$ ($V_{casc}=1.5V$), at a small cost on RF HCI lifetime, which is partly mitigated with V_{casc} correction. The stacked cell was not included in this benchmark due to its larger RF degradation compared to Interstack.

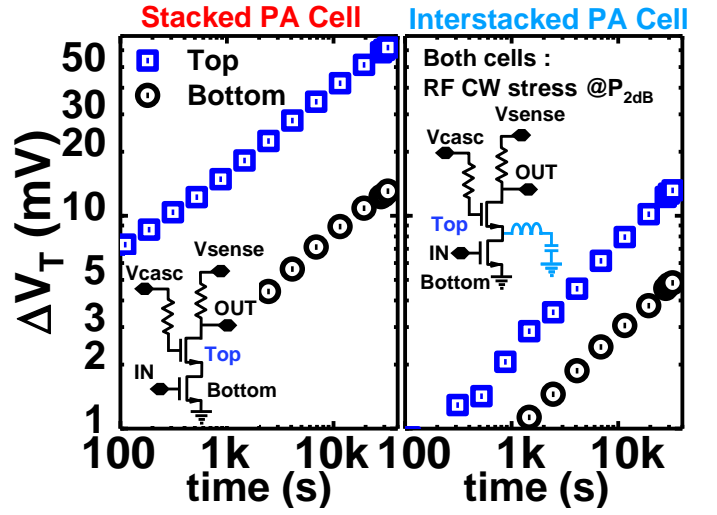


Fig. 13. V_{Tsat} drift versus time for both stacked PA cells, RF CW stress at $P_{2dB} = 17dBm$ (same for both DUT). Stack device is more degraded, whereas Interstack degradation is more balanced between top & bottom.

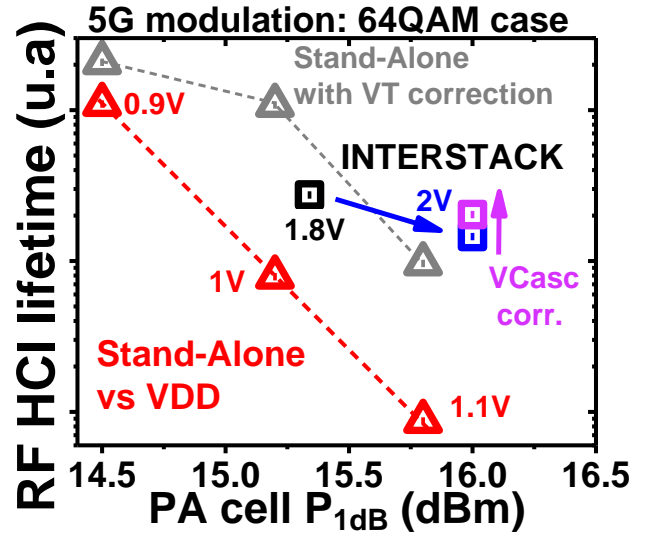


Fig. 14. Estimated performance/lifetime compromise between SA and Interstack power cells with different V_{DD} based on our methodology. V_T correction allows SA to be competitive versus Interstack.

IV. CONCLUSION

A methodology to address CMOS PA cells aging under complex mission profiles is presented and applied to the 5G-FR2 case. The DC and RF parameters degradations due to HCI under RF CW stress are modeled for different bias and modulations. Lifetime increases with modulation complexity due to linearity constraints and lower general power levels. V_T drift correction on SA transistors allows up to 10x HCI lifetime increase under 5G-FR2 modulation, but only has marginal gains for Stacked cells if the correction is applied on the common-gate transistor. Using this mitigation technique, SA PA cell RF HCI lifetime becomes competitive versus Interstack.

ACKNOWLEDGMENT

This work is part of the IPCEI Microelectronics and Connectivity and was supported by the French Public Authorities within the frame of France 2030.



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