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Data Retention Insights from Joint Analysis on BEOL-Integrated HZO-Based Scaled FeCAPs and 16kbit 1T-1C FeRAM Arrays

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Abstract—Extensive data retention measurements are performed on HZO-based BEOL-integrated scaled ferroelectric capacitors (FeCAPs) and 16kbit 1T-1C FeRAM arrays for the first time. At FeCAP level, Opposite State (OS) retention is strongly degraded by imprint phenomenon occurring during bake with a 0.20eV activation energy (E_A) and affecting equally ‘0’ and ‘1’ states. Imprint is found to be write-voltage independent, showing great promises for FeRAM voltage scaling with adequate write and read voltages distinction. At FeRAM-array level, post-bake distributions are reconstructed. Same-State (SS) and OS drifts of both logic states along bake time and temperature are consistent with FeCAP data ($E_A = 0.19\text{eV}$). These drifts are attributed to imprint and are demonstrated to be partly recoverable through bipolar cycling at operating voltage.

Index Terms—Data Retention, Etched FeCAP, FeRAM, Imprint, Voltage Scaling

I. INTRODUCTION

Ferroelectric HfO_2 is a promising material for non-volatile memory applications thanks to its predicted scalability, demonstrated high write and read speed, and inherent low power consumption [1] - [3]. Reliability studies focusing on data retention of HfO_2 -based devices have evidenced the role of imprint in retention degradation [4], [5]. The imprint phenomenon is defined as a shift of the hysteresis Polarization-Voltage (P-V) loop along the voltage axis and hence causes a shift of the coercive voltages. It occurs during thermal bake and is a major issue for Ferroelectric Random Access Memory (FeRAM) reliability as it reduces or even closes the Memory Window (MW) due to reading at a fixed voltage. Moreover, imprint can lead to higher-voltage operation requirements and hence to a reduced endurance. Data retention has been mostly investigated at Metal-Ferroelectric-Metal (MFM) capacitor level [4] - [7], but only in some occurrences and independently at integrated scaled FeCAP [8], [9] and FeRAM array levels [3], [10]. This work aims at clarifying the mechanisms behind data retention loss and offers for the first time a joint analysis on Back-End-Of-Line (BEOL) integrated FeCAP and FeRAM arrays based on an equivalent experimental strategy. Data retention is assessed at FeCAP level for different write and read electric fields, bake times and temperatures, then consolidated by statistical results at 16kbit 1T-1C FeRAM array level.

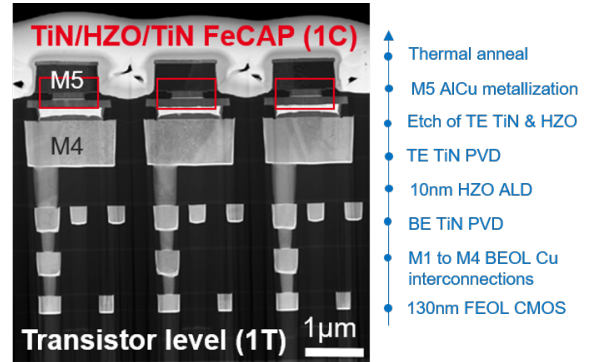


Fig. 1. (left) STEM cross-section of scaled HZO-based FeCAPs integrated between M4 and M5 in the BEOL of 130nm CMOS. (right) Simplified process flow for the fabrication of FeCAPs and 16kbit 1T-1C FeRAM arrays. Final thermal anneal was performed at BEOL-compatible temperature.

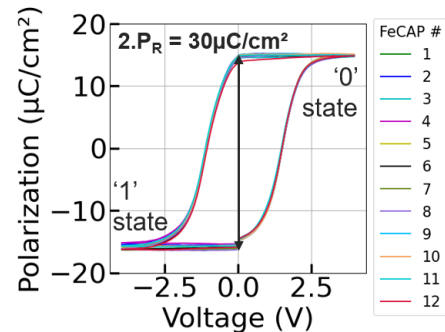


Fig. 2. Polarization-Voltage (P-V) hysteresis loops of 12 nominally identical FeCAPs with $0.24\mu\text{m}^2$ diameter, from $\pm 4\text{MV/cm}$ -10kHz PUND measurements performed after 10^4 triangular wake-up cycles at $\pm 4\text{MV/cm}$ -100kHz. FeCAPs show high device-to-device homogeneity and median $2.P_R$ is $30\mu\text{C/cm}^2$.

II. DEVICE FABRICATION AND FERROELECTRIC PROPERTIES

$\text{TiN} / \text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ (HZO) / TiN capacitors were integrated in the BEOL of 130nm CMOS [3]. After TiN Bottom Electrode (BE) PVD deposition, a 10nm-thick HZO layer was deposited by ALD. Following TiN Top Electrode (TE) PVD deposition, both TE and HZO layers were etched as in [11] (Fig. 1). Capacitor fields made of 1290 parallelly-routed

FeCAPs with individual area of $0.24\mu\text{m}^2$, as well as 16kbit 1T-1C FeRAM arrays with $0.38\mu\text{m}^2$ FeCAPs were integrated on the same wafer. P-V curves from PUND measurements at $\pm 4\text{MV/cm}$ - 10kHz on 12 nominally identical FeCAPs across wafer show very high device-to-device homogeneity and good ferroelectric (FE) performance, with a $30\mu\text{C/cm}^2$ median remanent polarization ($2.P_R$) after wake-up (Fig. 2).

III. DATA RETENTION AT BEOL-INTEGRATED SCALED FE CAP LEVEL

Data retention at the single device level is assessed by a specific pulse sequence as introduced in [4] and [12], which aims at analysing the impact of a thermal bake on each logic state programmed before bake, as well as each complementary state programmed and read post-bake. Fig. 3 shows the voltage pattern applied to two nominally identical FeCAPs to evaluate SS (Same State, state baked), NSS (New Same State, state baked restored after bake) and OS (Opposite State, state complementary to state baked) retention after a series of bakes at 85°C , 105°C and 125°C for 10^3s , 10^4s and 10^5s . Write and read fields have been set equal and were varied from 3MV/cm to 5MV/cm . Identical devices from different dies on the wafer were used for different write and read fields and bake temperature conditions. For each state, $2.P_R$ Margin is defined as the remanent polarization integrated from the ferroelectric switching current of Data1-Data0. On the contrary, P_{SW} is integrated directly from either Data0 or Data1 and is or includes a dielectric contribution, respectively. The retention response to this pattern with opposite polarities, *i.e.* with a negative read voltage applied to TE, was also measured to assess stack symmetry.

Fig. 4 gathers $2.P_R$ Margin results of SS, NSS and OS retention states in positive and negative polarities at 4MV/cm , along bake time and for bake temperatures of 85°C , 105°C and 125°C respectively. A semilog linear fit is used as a visual guide to assess 10 year-data retention. For all temperatures, no asymmetry between positive and negative polarities is visible, indicating that top and bottom electrode interfaces are not fundamentally different from a data retention viewpoint. This result is in line with the data presented by [4] and [8] and in the following, only positive polarities will be analyzed. Similarly, SS and NSS states are found to be stable over bake time for all temperatures. This indicates that the influence of thermal depolarization, expected to lower the remanent polarization after the bake [12], is very limited in our case. The most probable explanation is that the bake temperatures investigated, based on consumer or automotive applications requirements, are too low compared to the material's Curie temperature (estimated in the range of 600K to 1000K by [13]) to degrade SS retention. However, OS retention degrades much more quickly with bake time than SS and NSS because of imprint. This degradation is found to be highly dependent on bake temperature, as already shown on PZT [12] and HZO [9], thus making OS the limiting factor of data retention in ferroelectric memories, and imprint the main factor for data retention loss.

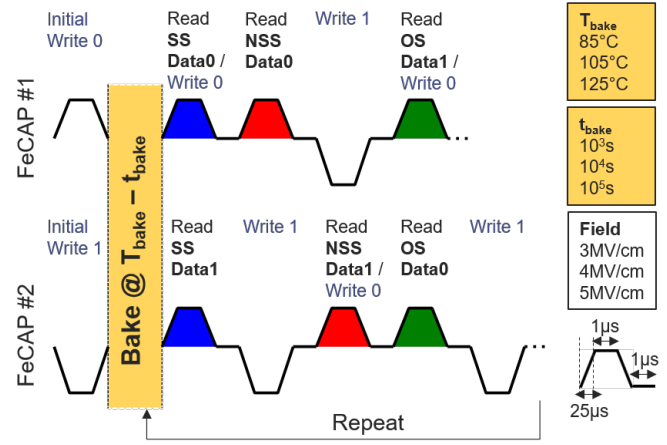


Fig. 3. Voltage-time pattern applied to the TE of 2 nominally identical FeCAPs to evaluate Same State (SS, blue), New Same State (NSS, red) and Opposite State (OS, green) retention. For all retention states, $2.P_R$ Margin is defined as the remanent polarization of Data1-Data0, while P_{SW} describes the polarization of either Data0 or Data1. Write and read voltages are equal, and in this case, the polarization state is read by positively pulsing the TE. The effect on retention of various bake times, temperatures and write and read fields is investigated.

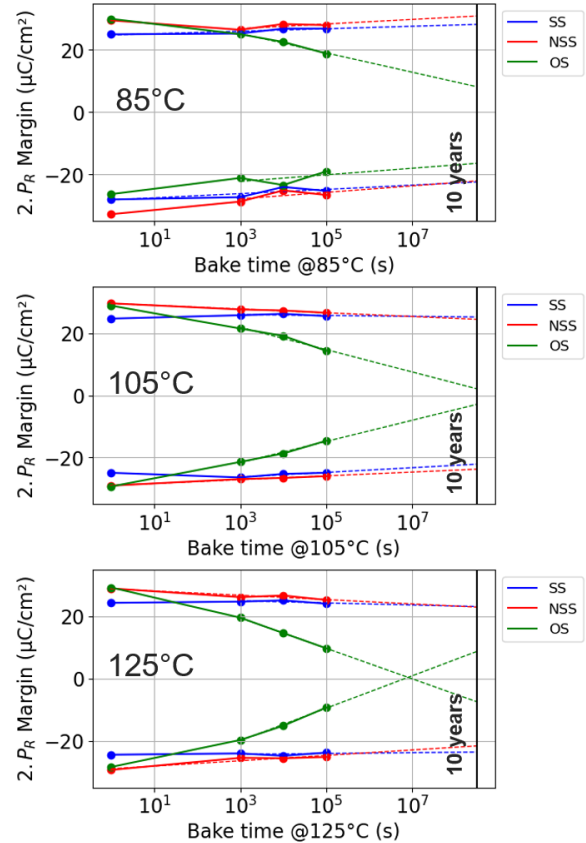


Fig. 4. $2.P_R$ Margin for SS, NSS and OS along bake time for temperatures of 85°C , 105°C and 125°C . Positive margin values correspond to pattern presented in Fig. 3 at 4MV/cm (read by positive pulse), while negative margin values account for opposite voltages (read by negative pulse). OS degrades strongly with bake time and temperature while SS and NSS are quite stable.

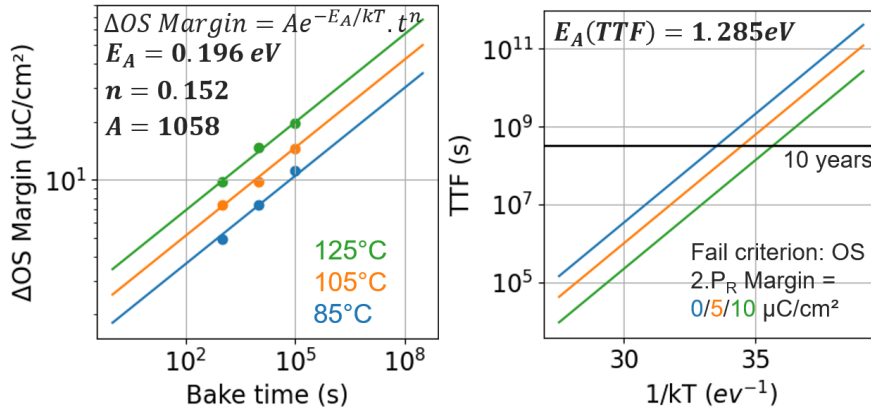


Fig. 5. (left) ΔOS represents OS 2.P_R Margin shift from the initial value (at t₀) due to thermal bake. The OS degradation is fitted by a power law along bake time and temperature with $E_A=0.196\text{eV}$ and $n=0.152$. (right) Time-To-Fail is modelled by an Arrhenius plot along $1/kT$ with $E_A(\text{TTF})=1.3\text{eV}$, no matter the fail criterion chosen. The two different activation energies are linked by n , where $E_A(\text{TTF})=E_A/n$.

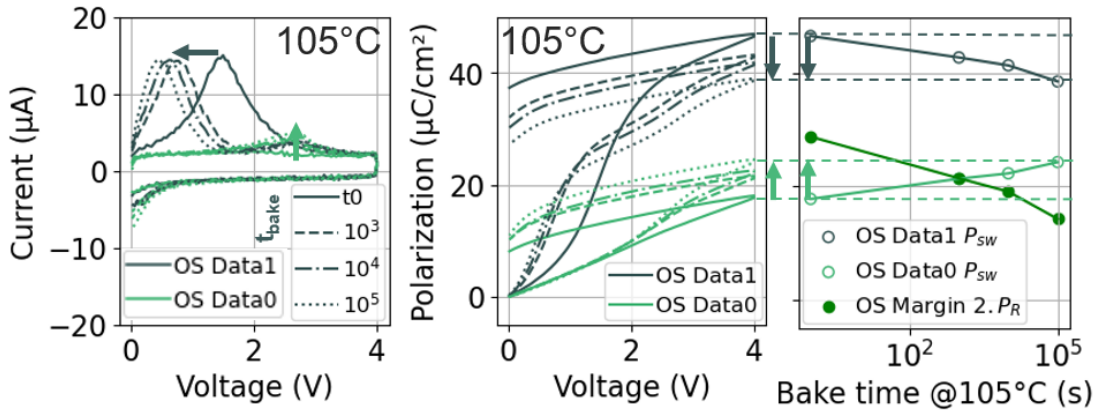


Fig. 6. (left) I-V, (middle) P-V and (right) P-t_{bake} from OS retention test at 4MV/cm, with bake temperature of 105°C. Imprinted ferroelectric switching current peaks cause increasing OS Data0 P_{SW} and decreasing OS Data1 P_{SW} along bake time that both equally contribute to a degraded OS 2.P_R Margin.

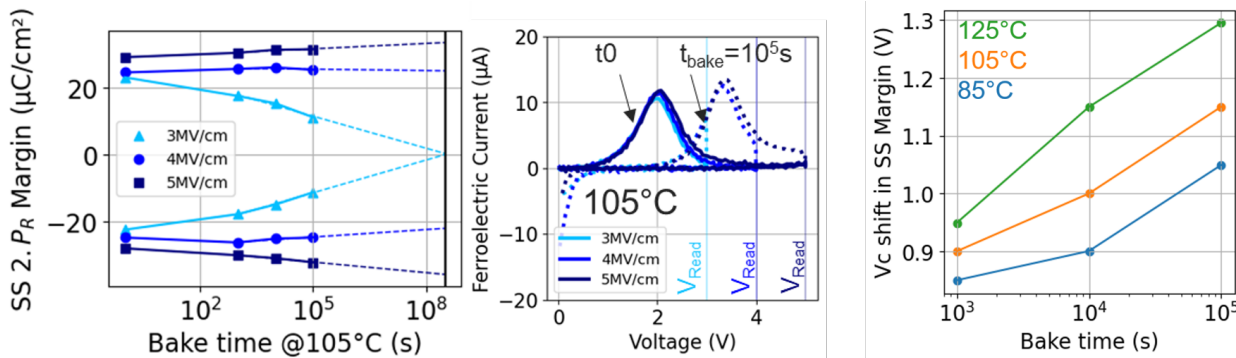


Fig. 7. (left) SS 2.P_R Margin-t_{bake} and (middle) I-V from SS retention test at different write and read fields, with bake temperature of 105°C. Coercive voltage shift occurring during bake does not depend on write field but reading field dramatically impacts SS 2.P_R Margin. (right) Coercive voltage shift in SS 2.P_R Margin as a function of bake time from SS retention test at 5MV/cm. Imprint leads to a V_c shift that increases with bake time and temperature.

For this reason, OS retention degradation is modelled in Fig. 5. The metric used represents the decrease of OS 2.P_R Margin compared to the initial value (at t₀, *i.e.* before bake) and is labelled Δ OS Margin. The experimental points of Δ OS Margin are found to be well-described by a unique thermally-activated power law

$$\Delta OS Margin = A e^{(-E_A/kT)} t^n \quad (1)$$

where fitting parameters are adjusted as follows: E_A , the activation energy for OS degradation, is 0.196eV, the pre-factor A is 1058 and the n-factor is 0.152. The power law thus fitted can then be used to model Time-To-Fail (TTF) as

$$TTF = B e^{(-E_A(TTF)/kT)} \quad (2)$$

in an Arrhenius plot. From (1), it follows that $B = \text{fail criterion}/A$ and $E_A(TTF) = E_A/n$. The fail criteria represented in Fig. 5 account for an OS 2.P_R Margin (see Fig. 4) reaching 0, 5 or 10 μ C/cm², respectively. Those low remanent polarization values are chosen to be indicative of weak retention at FeCAP level and forebode strongly degraded performances at FeRAM level. For all fail criteria, TTF curves generated by the power law are parallel and it is shown that $E_A(TTF)$ is 1.3eV and fail criterion independent. The relationship between E_A and $E_A(TTF)$ denotes a strong link between a physically-based activation energy (E_A) and an lifetime-related effective activation energy ($E_A(TTF)$). With an initial remanent polarization of 30 μ C/cm² and based on 0 μ C/cm² to 10 μ C/cm² fail criteria, extrapolated 10-year retentions at 74°C to 54°C are projected, respectively. Considering the microscopic imprint model provided by [7] and supported by DFT simulations, $E_A=0.196$ eV could be attributed to the position of oxygen vacancy related defects at the TiN/HZO interface. Change in the charge state of oxygen vacancies during retention bakes [12] is thought to activate shallow de-trapping sites that could affect the internal field [7]. A similar E_A of 0.2eV is reported in [14] and linked to oxygen vacancies in hafnium-based stacks.

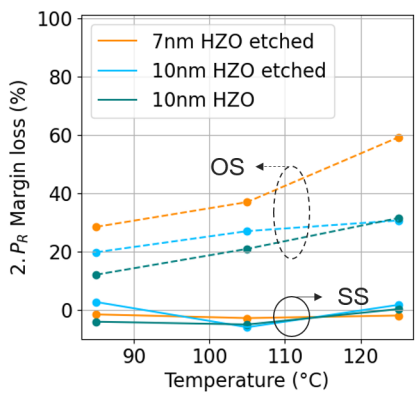


Fig. 8. SS and OS 2.P_R Margin loss percentage from retention tests at 4MV/cm as a function of bake temperature ($t_{\text{bake}}=10^3$ s) for three different splits: HZO 10nm with etched FE layer, HZO 10nm with non-etched FE layer and HZO 7nm with etched FE layer. While SS degradation is limited and similar for all splits, OS retention is worsened for thinner layers.

To better understand the electrical signature of OS retention degradation, Fig. 6 delves deeper into the OS retention of FeCAPs programmed at 4MV/cm and subjected to a series of thermal bakes at 105°C. Fig. 4 presented experimental points of OS 2.P_R Margin from Data1-Data0. In Fig. 6, the individual I-V (left) and P-V (middle) as well as P-t_{bake} (right) characteristics of OS Data0 and OS Data1 are looked into. From the I-V curves, it can be seen that the ferroelectric switching current peak of OS Data1 shifts towards lower voltages when the bake time is increased, consistently with results from [4], [5] and [7]. Because of this shift in the coercive voltage, or imprint, the current peak is increasingly truncated with bake time, leading to a reduced amount of switchable domains, and thus to a reduced polarization, as can be seen on the P-V curve. Hence, because imprint prevents polarization switching in an increasing number of domains with bake time, OS Data1 P_{SW} decreases, as can be seen in P-t_{bake}. This coercive voltage shift accompanied by remanent polarization loss due to imprint matches data presented in [7]. Simultaneously, the I-V of OS Data0 evidence a non-zero current peak which increases with bake time. This means that after baking a FeCAP in the '1' state, the attempt at programming a '0' (OS Data0) will not lead to a pure dielectric state but rather to a dielectric state with a ferroelectric contribution that increases with bake time. This phenomenon gives rise to an increasing polarization and thus to an increasing OS Data0 P_{SW} with bake time. Both trends contribute equally to OS 2.P_R Margin degradation.

Imprint occurring during bake also impacts SS retention to some extent. From Fig. 4, the results presented at 4MV/cm showed no degradation of SS retention. However, Fig. 7 (left) shows that SS 2.P_R Margin can degrade rapidly over bake time when data is written and read at low field. The trends at low and high field are consistent with results from [7]. Looking at the ferroelectric current (middle, from Data1-Data0), writing field is found to have no influence on the post-bake peak position, *i.e.* imprint is not field-dependent, consistently with [5]. Yet, reading field strongly impacts the as-measured polarization as only some domains have their coercive field lying below E_{read} . Thus, imprint is responsible for SS (and NSS) Margin poor performances at low field, but could be largely improved in an array by decorrelating write and read fields. Although shift in the coercive voltage, or imprint, does not depend on the field, it does depend on the bake time and temperature, as can be seen in Fig. 7 (right). The measured trend is in line with results provided in [9]. Not only does imprint degrade OS retention, but it also degrades SS retention at low field and high temperature.

Finally, Fig. 8 studies SS and OS 2.P_R Margin loss as a function of bake temperature for different Metal / Ferroelectric / Metal (MFM) stacks. Additionally to 10nm HZO etched stack presented in Section II, 10nm HZO (non-etched) and 7nm HZO etched stacks were studied. Write and read voltages were adapted so as to maintain a constant electric field across the different stacks. It can be seen that SS data retention Margin loss is similar for all stacks, and that OS data retention presents little to no difference in Margin loss between 10nm

HZO stacks, whether the FE layer is etched or not. However, Fig. 8 shows a degraded OS Margin loss for the 7nm HZO stack compared to the 10nm HZO stack, similarly to results from [6] and especially at higher bake temperature.

A change in the internal field due to electron de-trapping during bake is thought to be the cause for imprint, as exposed in [5] and [7]. A possible explanation for the degraded OS data retention in the 7nm stack compared to 10nm stacks could be a higher internal field for thinner films that worsens the imprint effect during bake.

IV. DATA RETENTION AT FERAM ARRAY LEVEL

The evaluation of data retention performance at array level is essential from an application perspective as it brings a statistical outlook on results obtained at the FeCAP level and can evidence additional array-related factors that impact FeRAM data retention compared to FeCAP. In a FeRAM array, the statistical dispersion of bitline voltage elevation following a destructive read is presented as a σ versus reference voltage (V_{ref}) distribution, where σ is the standard deviation and V_{ref} is the internal reference signal applied to sense amplifiers in the array for read operation, as described in previous work [3]. To evaluate the impact of thermal bakes on the distributions of both logic states, and because of destructive read, 16kbit arrays were divided in 16 subarrays made of randomly selected Word Lines (WL), as in [3]. Subarrays were then read at a specific V_{ref} to reconstruct distributions. Beside that, the experimental strategy used was very similar to Fig. 3, with the notable exceptions that NSS was not investigated, and only one field (pulses at 4MV/cm during 2 μ s) and one polarity (read operation by positive pulse on the TE, corresponding to the Plate Line, PL) were tested.

In a 16kbit 1T-1C FeRAM array with 0.38 μ m² capacitors, half of the subarrays were baked as '0' and the other half as '1'. Each subarray was then read at a distinct V_{ref} to reconstruct SS distributions, then the OS was written and read to reconstruct OS distributions. The reconstructed distributions presented in Fig. 9 evidence a moderate shift of SS Data0 towards lower reference voltages with bake time, and a stronger shift of SS Data1 in the same direction. OS Data0 shifts towards higher V_{ref} values, while OS Data1 shift is stronger and in the opposite direction. It is noticeable that '0' and '1' states slopes do not vary along bake time (and temperature, not shown here). Given that OS Data0 and OS Data1 shift towards a central V_{ref} with bake time, hence closing the Memory Window, OS is still the limiting factor for data retention. Similarly to Section III, Δ OS Margin in 16kbit array has been modelled and represents the loss of median MW for OS (Data1-Data0) compared to pre-bake median MW.

Fig. 10 (left) represents Δ OS Margin in a FeRAM array along bake time for different bake temperatures. Δ OS Margin can be fitted by a unique power law, as in (1), with $E_A' = 0.19$ eV, $A' = 23.9$ and $n' = 0.154$. The similarity in activation energy and n-factor between FeCAP and FeRAM models highlights equivalent data retention dynamics in single devices and arrays, and confirms that data retention studies

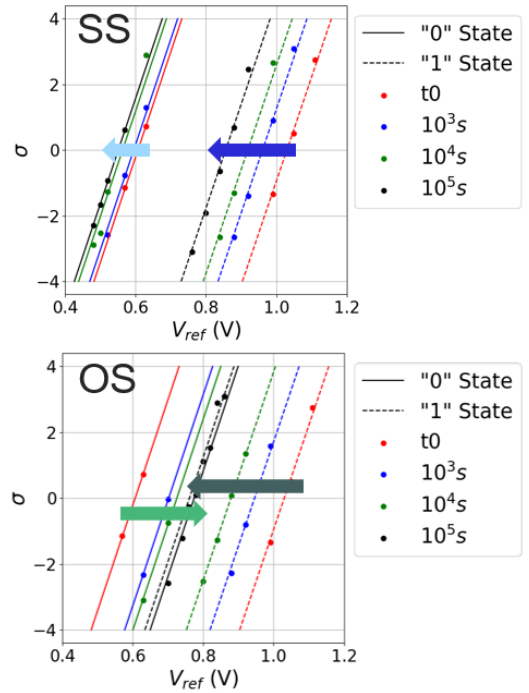


Fig. 9. SS and OS distributions reconstructed for both logic states post-bake at 105°C. Individual capacitors of the 16kbit 1T-1C FeRAM array were programmed and read at 4MV/cm-2 μ s, and the experimental points were measured on subarrays read at a specific V_{ref} each as in [3]. The arrows indicate the direction and strength of distributions shifts with bake time for all retention states: SS Data0, SS Data1, OS Data0, OS Data1.

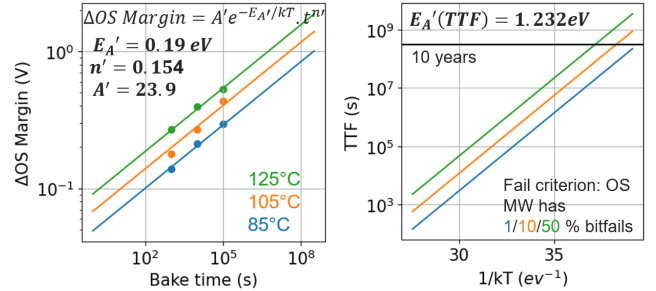


Fig. 10. (left) Δ OS represents OS median Memory Window shift from the initial value (t_0) due to thermal bake. The OS degradation is fitted by a power law along bake time and temperature with $E_A' = 0.19$ eV and $n = 0.154$. (right) Time-To-Fail is modelled by an Arrhenius plot along $1/kT$ with $E_A(TTF) = 1.2$ eV, no matter the intrinsic fail criterion chosen.

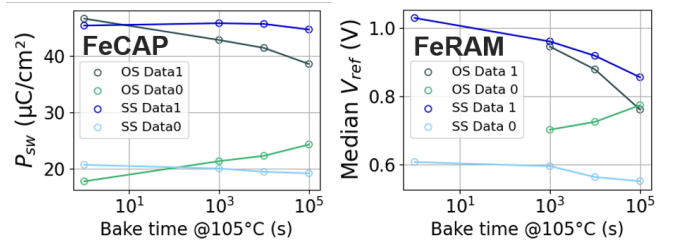


Fig. 11. P_{sw} and median V_{ref} as a function of bake time at 105°C for FeCAP and 16kbit 1T-1C FeRAM arrays respectively. Although the trend is similar for all retention states, FeRAM degradation is increased compared to FeCAP, pointing to an additional factor from the memory array.

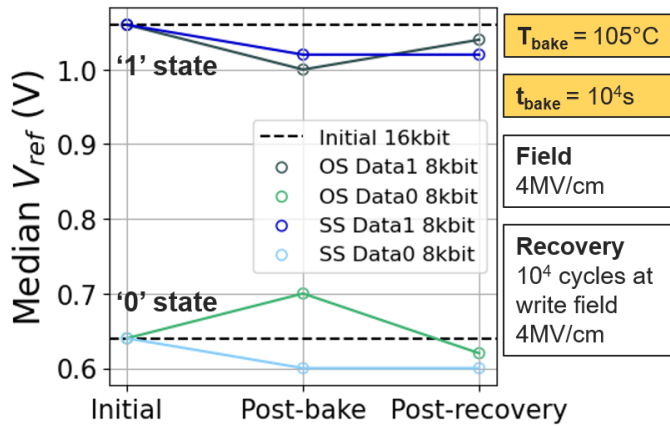


Fig. 12. Median V_{ref} for all retention states before bake, after bake at 105°C for 10^4s , and after 10^4 cycles at 4MV/cm . The recovery strategy consisting in cycling 16kbit 1T-1C FeRAM array at operating field enables to recover the distributions shifted by imprint during bake to initial distributions.

at FeCAP level are relevant to predict array behavior. A and A' are pre-factors of ΔOS Margin in FeCAP (see (1)) and FeRAM, respectively, and can be related with the MW formula

$$A'e^{(-E'_A/kT)} \cdot t^{n'} = Ae^{(-E_A/kT)} \cdot t^n \times \frac{S}{C_d + C_{BL}} \quad (3)$$

where S is the FeCAP area, C_d its dielectric capacitance and C_{BL} the circuit Bit Line capacitance [5]. Given that the activation energy and n -factor of FeCAP and FeRAM have been found to be very close, it follows that $A'/A = S/(C_d + C_{BL})$, confirmed by numerical application. At FeRAM level, TTF along $1/kT$ was also modelled by Arrhenius' law as in (2), with fail criteria of 1%, 10% and 50% intrinsic bitfails, taking advantage of the constant standard deviation, and thus distribution slopes, along bake time. Hence, TTF bitfails account for intrinsic variability in the array and bake-induced distributions shifts at array level. E'_A (TTF) was found to be 1.2eV , equal to E'_A/n' and close to that of FeCAPs (Fig. 10, right). This strongly indicates that the imprint phenomenon governing OS data retention loss at FeCAP level occurs in the same way at FeRAM level. Based on 1% to 50% bitfails criteria at memory array level, extrapolated 10-year retentions from 36°C to 51°C are projected at FeRAM level, respectively.

From data shown in Fig. 3 and Fig. 9 however, SS and OS retention degradation with bake time appears stronger at FeRAM level. This is confirmed by Fig. 11, which presents the evolution of FeCAP P_{SW} and FeRAM median V_{ref} along bake time at 105°C . All four retention states (OS Data1, OS Data0, SS Data1 and SS Data0) are investigated in the same conditions, and P_{SW} and V_{ref} can be related by analytical formulae presented in [3]. Global trends of shift direction and amplitude are found similar but FeRAM time-dependent retention appears degraded compared to that of its FeCAP counterpart. Indeed, while imprint has been demonstrated to affect ΔOS Margin in the same way in FeCAP and FeRAM, pre-bake OS Margin values may differ between FeCAP and FeRAM. In this case, it is thought that the lower OS Margin

value in FeRAM comes from a voltage drop in the array that leads to an overall reduced effective write and read voltage during operation at array level. To conclude, the results presented point toward an identical phenomenon governing data retention at FeCAP and FeRAM level, as well as additional design-related effects further degrading SS and OS retention in FeRAM arrays.

The main cause of data retention loss has been determined to be imprint. In MFM capacitors [5] [7] or scaled integrated FeCAPs [9], the application of a series of cycling pulses to the imprinted device has been demonstrated to induce recovery from imprint. At cycling field lower than operating field, partial recovery is possible [5]; at operating field, full recovery is possible without the need for a higher field as in the recovery of fatigue [15] [16]. To our knowledge, no such recovery effect from imprint has been investigated at the FeRAM array level. On a FeRAM array presenting shifted distributions of SS and OS for both logic states following a bake at 105°C for 10^4s , bipolar cycling at operating field is demonstrated to reverse the imprint effect and therefore recover most of the memory window (Fig. 12). This recovery, as first evidenced on FeCAPs, appears as a promising operating strategy for getting rid of OS-limited data retention in FeRAM arrays.

V. CONCLUSIONS

A thorough data retention assessment is reported to be consistent from HZO-based scaled FeCAPs to 16kbit 1T-1C FeRAM arrays integrated on the same wafers in the BEOL of 130nm CMOS. In the bake temperature range investigated (85°C - 125°C), OS retention is found to be the limiting factor for data retention loss with a 0.2eV activation energy. Imprint is responsible for OS retention degradation, as well as for SS degraded retention at low field and high bake temperature. OS retention is further degraded for MFM stacks with a thinner HZO layer, possibly due to a higher internal field that worsens the imprint phenomenon. Since imprint is not field-dependent, its effect on FeCAP SS data retention can be countered by reading SS data at higher field. In FeRAM arrays, a similar physically-based activation energy of 0.2eV was obtained, highlighting an identical phenomenon governing OS data retention loss at FeCAP and FeRAM level. Additional design-related factors have been shown to further degrade SS and OS retention compared to performance at FeCAP level. Finally, it has been shown that applying cycling pulses at operating field in FeRAM arrays enables to partially recover the imprinted distributions.

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