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Post-Deposition Annealing challenges for ALD $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x/\text{n-GaN}$ MOS devices

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Abstract—In this work, we investigate the impact of high-temperature Post-Deposition Annealing (PDA) on $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$ deposited by Atomic Layer Deposition (ALD). Reversed hysteresis is observed and explained by mobile charges originating from K^+ and Na^+ impurities. The high-temperature annealing does not cure the presence of these mobile charges. We also report the onset of film and interface degradation after annealing above 750°C under N_2 , with both inhomogeneous aluminium and silicon composition, signs of AlSiO crystallization and interfacial gallium oxide growth.

Keywords— AlSiO , GaN , MOS , PDA , *Mobile Charges*, *Interface*

1. Introduction

GaN has interesting physical properties for power electronics, such as a wide band gap and a high critical electric field. Coupled with AlGaN , the heterojunction AlGaN/GaN allows the fabrication of High Electron Mobility Transistors (HEMTs) with low ON-Resistance (R_{ON}) and high switching frequency [1]. These advantageous properties derive from the formation of a two-dimensional electron gas (2-DEG) with high mobility at the heterojunction. However, GaN HEMTs present a negative threshold voltage (V_{TH}), which can cause safety issues and complicates the driver design. GaN HEMTs with a positive V_{TH} are hence highly desirable. The Metal-Oxide-Semiconductor-channel HEMT (MOSc-HEMT) is a promising solution to obtain a HEMT with a positive V_{TH} , a wider voltage swing and a lower gate leakage [2]. Positive V_{TH} is obtained by fully recessing the AlGaN barrier at the gate region. Different gate dielectrics such as SiO_2 [3], [4], SiN_x [4] and Al_2O_3 [5], [6] have been studied. Among these oxides, Al_2O_3 is commonly used due to its high permittivity and high band gap [7], yet the $\text{Al}_2\text{O}_3/\text{GaN}$ gate stack can suffer from V_{TH} instability and low thermal stability [5], [8]. The latter hinders the use of high-temperature annealing to increase V_{TH} and reduce V_{TH} hysteresis. However, AlSiO is a promising dielectric with higher thermal stability [9], [10] and lower Flat-Band Voltage hysteresis (ΔV_{FB}) [9], [11]. Increasing the Si content in AlSiO was also reported to decrease hysteresis and increase the conduction band offset [11], [12]. If the beneficial impact of Post-Deposition Annealing (PDA) was studied for $\text{Al}_{0.78}\text{Si}_{0.22}\text{O}_x$ [10], the impact of PDA for higher Si content has not been investigated. Hence in this work, we investigate the impact of high-temperature PDA on $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$ with MOS capacitances (MOSCAPs) electrical measurements and physico-chemical analyses.

2. Experimental

19 nm $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$ (alternating Al_2O_3 and SiO_2) with a silicon content of 50% or 30 nm Al_2O_3 layers were deposited by Atomic Layer Deposition (ALD) on MOCVD as-grown n-GaN ($N_D=5 \times 10^{17} \text{ cm}^{-3}$)/Si 200mm wafer. For AlSiO, the ALD precursors for Al, Si and O sources were trimethylaluminium, tris(dimethylamino)silane and ozone, respectively. For Al_2O_3 , the precursors for Al and O were trimethylaluminium and water. Before ALD, a wet sequence without Na or K and ending with HF was performed on the GaN wafer surface. After ALD, the wafer was cut into $1.5 \times 1.5 \text{ cm}^2$ AlSiO samples and underwent PDA at 650°C , 750°C , 850°C and 950°C for 3min under N_2 . Then MOSCAPs test structures (**Fig.1**) were fabricated with Ni/Au deposited by e-beam evaporation.

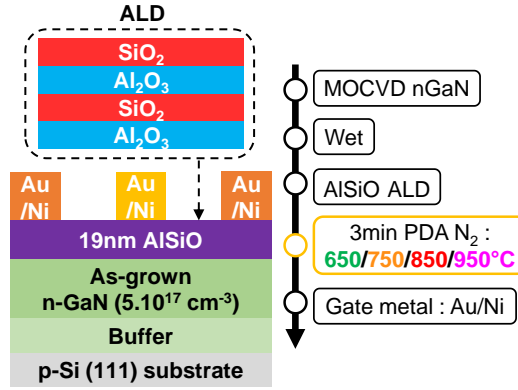


Fig.1: MOSCAPs process flow with different PDA temperatures.

Bidirectional C-V measurements were carried out at 1 kHz with a voltage sweep from -4V to 6V and back to -4V. C-V measurements were performed at three different measuring temperatures: 25°C , 150°C and 200°C . The Flat-Band Voltage (V_{FB}) was extracted by using the theoretical Flat-Band Capacitance (C_{FB}) calculated as:

$$C_{\text{FB}} = C_{\text{OX}} C_{\text{D}} / (C_{\text{OX}} + C_{\text{D}}) \quad (1)$$

$$\text{with } C_{\text{D}} = \sqrt{kT \epsilon_{\text{GaN}} \epsilon_0 / (q^2 N_{\text{D}})} \quad (2)$$

Where C_{OX} , k , T , ϵ_{GaN} , ϵ_0 and q are respectively the oxide capacitance, the Boltzmann constant, the temperature in Kelvin, the relative GaN permittivity, the vacuum permittivity and the electron elementary charge. Bias Temperature Stress (BTS) was carried out to calculate mobile charges density by stressing the gate at 1.8 V for 10 min at 200°C . After 10 min, the stress is maintained and the temperature is set to room temperature. Then at room temperature, a C-V measurement is performed and the procedure is repeated for the stress at -1.8 V. The mobile charges density is calculated as below:

$$Q_m = -C_{OX}(V_{FB}^{+1.8V} - V_{FB}^{-1.8V}) \quad (3)$$

These samples were also analysed by Transmission Electron Microscopy (TEM). Samples without metallization were analysed by Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and Angle-Resolved Hard X-ray Photoelectron Spectroscopy (AR-HAXPES). ToF-SIMS was performed on a ToF-SIMS 5 with a 500 eV Cs⁺ sputter gun, and both negative and positive ions were analysed with a 30 KeV Bi₃⁺ ion beam. The Al_{0.5}Si_{0.5}O_x/GaN interface was calibrated to where the reference bulk signal used for normalization drops by 50%. AR-HAXPES was performed at take-off angles of 42, 50 and 65° on a Phi Quantes equipped with a monochromatic Cr K α X-Ray source (h ν =5414.7 eV), allowing the analysis of buried interfaces. The Ga2p_{3/2} spectrum was used to analyse the Ga-O bond with respect to Ga-N by using the model in [13]. The GaO_x thickness was determined with the equation in **Fig.7.b**). The ratio $I_{GaN}^{\infty}/I_{GaO}^{\infty}$ was experimentally evaluated as 0.873 by using GaN and Ga₂O₃ reference samples, and λ , the inelastic mean free path of Ga2p_{3/2} photoelectrons in Ga₂O₃, was calculated to be 5.831 nm using the TPP-2M model. The 50% Si composition (or $100 \times Si/(Al + Si)$) for the different PDA temperatures was confirmed with HAXPES quantification at 75°, as represented in **Table 1**.

| PDA | w/o PDA | 650°C | 750°C | 850°C | 950°C |
|---------------------------|---------|-------|-------|-------|-------|
| $100 \times Si/(Al + Si)$ | 50% | 49% | 50% | 49% | 46% |

Table 1: Silicon composition extracted by HAXPES for the different PDA temperatures, the silicon content staying around 50%.

3. MOSCAPs electrical results

The C-V at different temperatures and the extracted Flat-Band Voltage hysteresis (ΔV_{FB}) are reported in **Fig.2** and **Fig.3.a**) respectively. No C-V characteristics were measured for the 950°C sample due to large leakage current in the oxide. For measurements at room temperature, AlSiO MOSCAPs exhibit slightly lower ΔV_{FB} compared to Al₂O₃, but increasing the PDA temperature up to 750°C leads to ΔV_{FB} decrease. With 850°C PDA ΔV_{FB} becomes unexpectedly negative (reversed hysteresis). Increasing the measuring temperature at 200°C reveals a reversed ΔV_{FB} for all AlSiO samples, which was already reported in literature but for higher Si content in AlSiO (73%) at room temperature, and on N-face GaN [11]. The presence of reversed hysteresis may originate from mobile charges [14]. BTS measurements reported in **Fig.3.b**) confirm the presence of $2.3 \sim 2.4 \times 10^{12}$ cm⁻² of mobile charges for the samples with and without 850°C PDA. Moreover, C-V at different frequencies (not shown here) reveal a density of interface states under 10^{10} eV⁻¹.cm⁻².

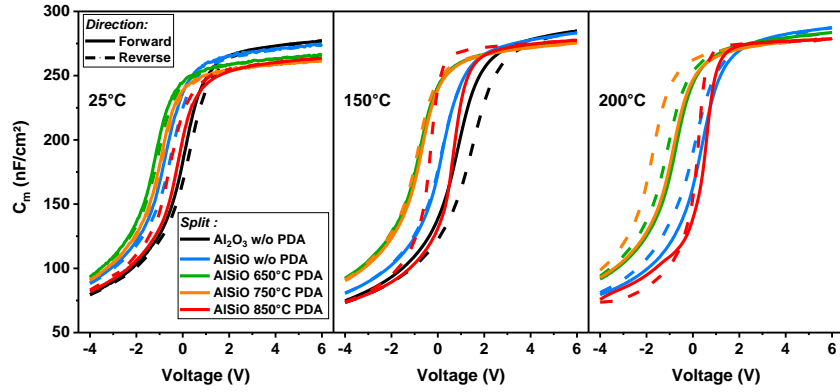


Fig.2: Bidirectional C-V measurements (median of five measurements). No C-V measurements are shown for 950°C PDA because of large leakage current, probably due to crystallization of AlSiO (c.f. Fig.6).

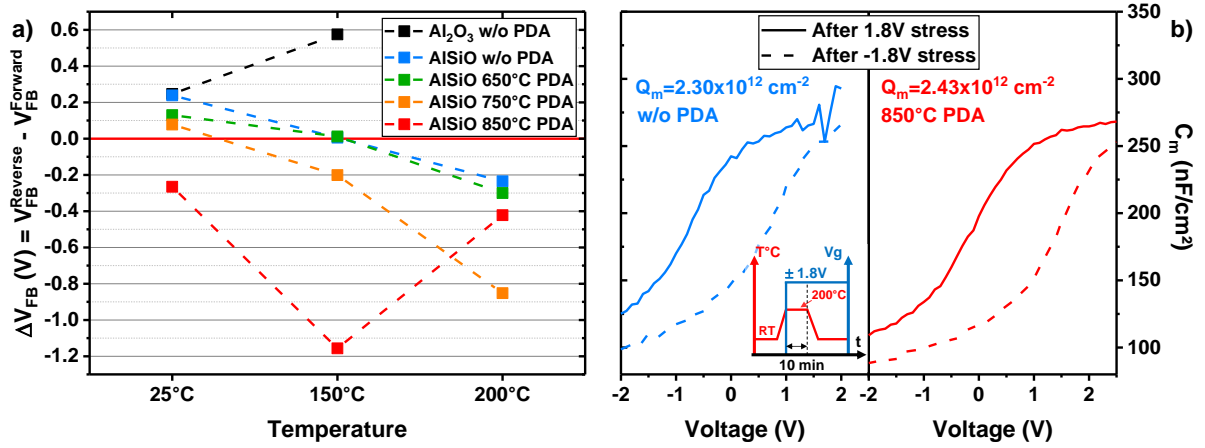


Fig.3: a) Extracted ΔV_{FB} from C-V measurements. Increasing the measuring temperature reveals reversed hysteresis for all AlSiO samples; b) BTS measurements on AlSiO samples without PDA and with 850°C PDA. Similar amount of mobile charges is calculated for the AlSiO samples without PDA and with 850°C PDA.

4. Discussion with physico-chemical analyses

The mobile charges observed in C-V and BTS measurements may come from the Na^+/K^+ contamination [14] detected by ToF-SIMS on AlSiO samples with and without 850°C PDA (Fig.4).

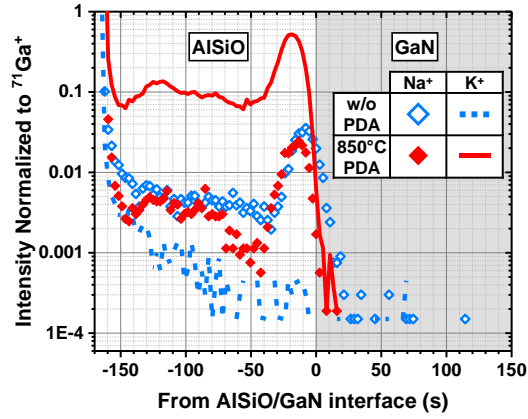


Fig.4: ToF-SIMS depth profiles of K^+ and Na^+ on AlSiO samples without and with 850°C PDA. Both samples have Na^+ and K^+ contamination.

The high PDA temperature does not cure their presence but further increases the presence of K^+ . Their origin is currently under investigation and it's most probably due to the process environment. Their origin might not be the wet cleaning because it does not contain Na or K and because the same cleaning was used for the Al_2O_3 sample which does not present reversed hysteresis. However, OH groups are reduced until 850°C PDA (**Fig.5.a**). Since they can trap electrons [15], their reduction could explain the decreased positive hysteresis measured at room temperature for PDA temperatures under 850°C. Other sources of electron trapping exist such as oxygen vacancies (V_O) but it was reported that Si reduces their presence in AlSiO [16]. Since similar amount of mobile charges are extracted for samples with or without 850°C PDA, the difference in reversed hysteresis for the different PDA temperatures can be partially explained by their respective different amounts of electron traps. The negative trapped electron charges would then compensate for the effect of positive mobile charges. Hence, increasing PDA temperature seems to reveal the mobile charges by reducing the electron traps.

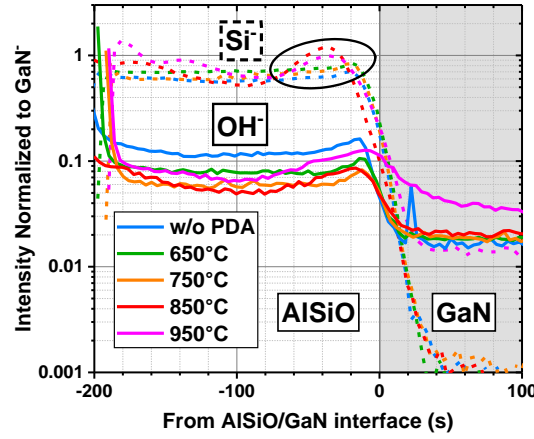


Fig.5: ToF-SIMS depth profiles of OH^- and of Si^- . Increasing PDA temperature reduces OH^- content to a minimum at 850°C, but from 850°C PDA the silicon accumulates at the AlSiO/GaN interface (same behaviour observed for Al- not shown here).

Moreover, high-temperature PDA further deteriorates the AlSiO layer. The absence of C-V characteristics for 950°C PDA is indeed due to crystallized regions observed by TEM (**Fig.6**) inducing large leakage current. Smaller regions are also observed for the 850°C PDA sample but they do not seem to affect the C-V measurements. However, they could accelerate the mobile charges movement since the 850°C sample has a reversed hysteresis for a C-V at room temperature [17]. This start of crystallization happens at a lower temperature than reported by Kikuta and co-workers for $\text{Al}_{0.78}\text{Si}_{0.22}\text{O}_x$ [10], a possible explanation being the different oxygen source. In fact, for HfO_2 , poorer oxygen content leads to lower crystallization temperature [18].

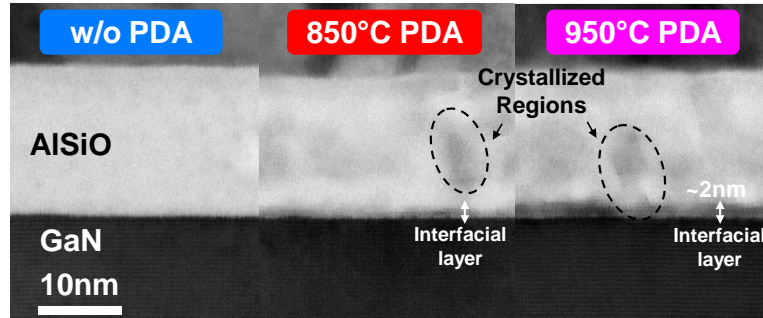


Fig.6: TEM images for AlSiO samples without and with PDA at 850°C and 950°C. Both PDA samples present crystallized regions and interfacial layers. But 950°C PDA sample has a thicker interfacial layer and more crystallized regions.

Likewise, inhomogeneous Si (and Al) distribution appears for PDA over 750°C, as shown by ToF-SIMS Si^- profiles (**Fig.5.b**), demonstrating that AlSiO is already degraded at this PDA temperature range. PDA above 750°C also leads to an interfacial layer, with a ~2 nm layer for 950°C PDA (**Fig.6**). This layer is identified as interfacial gallium oxide (GaO_x) as shown by ToF-SIMS $^{71}\text{GaO}^-$ profiles (**Fig.7.a**) and GaO_x thicknesses as extracted from AR-HAXPES (**Fig.7.b**). The thickness increasing after 750°C PDA correlates well with the $^{71}\text{GaO}^-$

profile extension inside AlSiO. The GaN thermal oxidation is known to increase for temperatures higher than 750°C. Similarly to SiO₂ or HfSiO_x, AlSiO with PDA over 750°C does not hinder the growth of interfacial GaO_x. However, its presence does not lead to a higher interface states density.

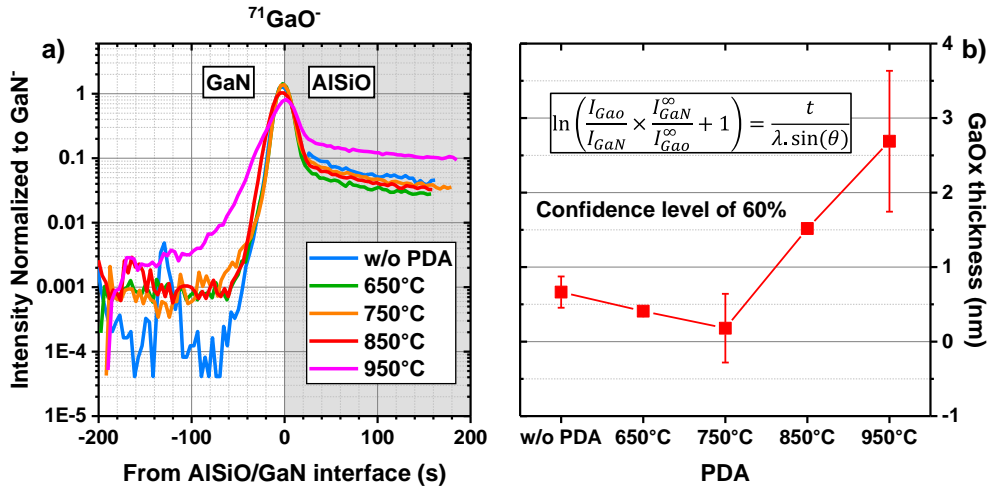


Fig.7: a) ToF-SIMS depth profiles of ⁷¹GaO⁻ and b) GaO_x thickness extracted from varying the HAXPES take-off angle between 42/50/65°. The ⁷¹GaO⁻ profile extend towards AlSiO for PDA temperature higher than 750°C, correlating to the increased GaO_x thickness after 750°C PDA.

5. Conclusion

We have investigated the impact of high PDA temperatures on Al_{0.5}Si_{0.5}O_x/n-GaN samples. Reversed hysteresis is observed for all AlSiO samples and seems to be related to mobile charges (Na⁺/K⁺). Higher PDA temperatures seem to reduce electron trapping by reducing hydroxyl groups, but PDA over 750°C leads to inhomogeneous atomic composition, GaO_x growth and to a beginning of crystallization. The optimal PDA temperature is 750°C, with more analyses with different Si% and oxygen source to be performed.

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References

- [1] J. He, W.-C. Cheng, Q. Wang, K. Cheng, H. Yu, and Y. Chai, “Recent Advances in GaN-Based Power HEMT Devices,” *Advanced electronic materials*, vol. 7, no. 4, p. 2001045, 2021, doi: 10.1002/aelm.202001045.

- [2] C. Le Royer *et al.*, “Normally-OFF 650V GaN-on-Si MOSc-HEMT Transistor: Benefits of the Fully Recessed Gate Architecture,” in *2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2022, pp. 49–52. doi: 10.1109/ISPSD49238.2022.9813672.
- [3] P. Fiorenza, G. Greco, F. Iucolano, A. Patti, and F. Roccaforte, “Channel Mobility in GaN Hybrid MOS-HEMT Using SiO₂ as Gate Insulator,” *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2893–2899, Jul. 2017, doi: 10.1109/TED.2017.2699786.
- [4] T.-L. Wu *et al.*, “Correlation of interface states/border traps and threshold voltage shift on AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistors,” *Appl. Phys. Lett.*, vol. 107, no. 9, p. 093507, Aug. 2015, doi: 10.1063/1.4930076.
- [5] Y. Hori, C. Mizue, and T. Hashizume, “Process Conditions for Improvement of Electrical Properties of Al₂O₃/n-GaN Structures Prepared by Atomic Layer Deposition,” *Jpn. J. Appl. Phys.*, vol. 49, no. 8, p. 080201, Aug. 2010, doi: 10.1143/JJAP.49.080201.
- [6] Q. Zhou *et al.*, “7.6 V Threshold Voltage High-Performance Normally-Off Al₂O₃/GaN MOSFET Achieved by Interface Charge Engineering,” *IEEE ELECTRON DEVICE LETTERS*, vol. 37, no. 2, p. 4, 2016, doi: 10.1109/LED.2015.2511026.
- [7] J. Robertson, “High dielectric constant oxides,” *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004, doi: 10.1051/epjap:2004206.
- [8] A. G. Viey *et al.*, “Influence of Carbon on pBTI Degradation in GaN-on-Si E-Mode MOSc-HEMT,” *IEEE Trans. Electron Devices*, pp. 1–8, 2021, doi: 10.1109/TED.2021.3050127.
- [9] S. H. Chan *et al.*, “Metalorganic chemical vapor deposition and characterization of (Al,Si)O dielectrics for GaN-based devices,” *Jpn. J. Appl. Phys.*, vol. 55, no. 2, p. 021501, Feb. 2016, doi: 10.7567/JJAP.55.021501.
- [10] D. Kikuta, K. Ito, T. Narita, and T. Kachi, “Highly reliable AlSiO gate oxides formed through post-deposition annealing for GaN-based MOS devices,” *Appl. Phys. Express*, vol. 13, no. 2, p. 026504, Feb. 2020, doi: 10.7567/1882-0786/ab658a.
- [11] I. Sayed, W. Liu, J. Georgieva, A. Krishna, S. Keller, and U. K. Mishra, “Characterization of AlSiO dielectrics with varying silicon composition for N-polar GaN-based devices,” *Semicond. Sci. Technol.*, vol. 35, no. 9, p. 095027, Sep. 2020, doi: 10.1088/1361-6641/ab9ecb.
- [12] D. Kikuta, K. Itoh, T. Narita, and T. Mori, “Al₂O₃/SiO₂ nanolaminate for a gate oxide in a GaN-based MOS device,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 35, no. 1, p. 01B122, Dec. 2016, doi: 10.1116/1.4971399.

- [13] P. Fernandes Paes Pinto Rocha *et al.*, “Impact of post-deposition anneal on ALD Al₂O₃/etched GaN interface for gate-first MOSc-HEMT,” *Power Electronic Devices and Components*, vol. 4, p. 100033, Jan. 2023, doi: 10.1016/j.pedc.2023.100033.
- [14] D. K. Schroder, “Oxide and Interface Trapped Charges, Oxide Thickness,” in *Semiconductor Material and Device Characterization*, John Wiley&Sons, Ltd.2005, pp. 319–387.
- [15] S. Ozaki *et al.*, “Effect of Oxidant Source on Threshold Voltage Shift of AlGaIn / GaN MIS-HEMTs Using ALD-Al₂O₃ Gate Insulator films,” presented at the CS MANTECH 2012 conference, Boston MA, 2011.
- [16] K. Chokawa *et al.*, “Absence of Oxygen-Vacancy-Related Deep Levels in the Amorphous Mixed Oxide (Al₂O₃)_{1-x}(SiO₂)_x: First-Principles Exploration of Gate Oxides in GaN -Based Power Devices,” *Phys. Rev. Applied*, vol. 14, no. 1, p. 014034, Jul. 2020, doi: 10.1103/PhysRevApplied.14.014034.
- [17] B. J. Tang, W. D. Zhang, J. F. Zhang, G. Van den bosch, B. Govoreanu, and J. Van Houdt, “Abnormal VTH/VFB shift caused by as-grown mobile charges in Al₂O₃ and its impacts on Flash memory cell operations,” in *2011 International Electron Devices Meeting*, Washington, DC, USA: IEEE, Dec. 2011, p. 9.6.1-9.6.4. doi: 10.1109/IEDM.2011.6131523.
- [18] D. Biswas, M. N. Singh, A. K. Sinha, S. Bhattacharyya, and S. Chakraborty, “Effect of excess hafnium on HfO₂ crystallization temperature and leakage current behavior of HfO₂/Si metal-oxide-semiconductor devices,” *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 34, no. 2, p. 022201, Mar. 2016, doi: 10.1116/1.4941247.
- [19] T. Yamada *et al.*, “Comprehensive study on initial thermal oxidation of GaN(0001) surface and subsequent oxide growth in dry oxygen ambient,” *Journal of Applied Physics*, vol. 121, no. 3, p. 035303, Jan. 2017, doi: 10.1063/1.4974458.
- [20] T. Yamada *et al.*, “Control of Ga-oxide interlayer growth and Ga diffusion in SiO₂/GaN stacks for high-quality GaN-based metal–oxide–semiconductor devices with improved gate dielectric reliability,” *Appl. Phys. Express*, vol. 11, no. 1, p. 015701, Jan. 2018, doi: 10.7567/APEX.11.015701.
- [21] E. Maeda *et al.*, “Change of characteristics of n-GaN MOS capacitors with Hf-rich HfSiO_x gate dielectrics by post-deposition annealing,” *Microelectronic Engineering*, vol. 216, p. 111036, Aug. 2019, doi: 10.1016/j.mee.2019.111036.