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## Post-Deposition Annealing challenges for ALD $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x/\text{n-GaN}$ MOS devices

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**Abstract**—In this work, we investigate the impact of high-temperature Post-Deposition Annealing (PDA) on  $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$  deposited by Atomic Layer Deposition (ALD). Reversed hysteresis is observed and explained by mobile charges originating from  $\text{K}^+$  and  $\text{Na}^+$  impurities. The high-temperature annealing does not cure the presence of these mobile charges. We also report the onset of film and interface degradation after annealing above  $750^\circ\text{C}$  under  $\text{N}_2$ , with both inhomogeneous aluminium and silicon composition, signs of  $\text{AlSiO}$  crystallization and interfacial gallium oxide growth.

**Keywords**— $\text{AlSiO}$ ,  $\text{GaN}$ ,  $\text{MOS}$ ,  $\text{PDA}$ , *Mobile Charges*, *Interface*

### 1. Introduction

$\text{GaN}$  has interesting physical properties for power electronics, such as a wide band gap and a high critical electric field. Coupled with  $\text{AlGaN}$ , the heterojunction  $\text{AlGaN}/\text{GaN}$  allows the fabrication of High Electron Mobility Transistors (HEMTs) with low ON-Resistance ( $R_{\text{ON}}$ ) and high switching frequency [1]. These advantageous properties derive from the formation of a two-dimensional electron gas (2-DEG) with high mobility at the heterojunction. However,  $\text{GaN}$  HEMTs present a negative threshold voltage ( $V_{\text{TH}}$ ), which can cause safety issues and complicates the driver design.  $\text{GaN}$  HEMTs with a positive  $V_{\text{TH}}$  are hence highly desirable. The Metal-Oxide-Semiconductor-channel HEMT (MOSc-HEMT) is a promising solution to obtain a HEMT with a positive  $V_{\text{TH}}$ , a wider voltage swing and a lower gate leakage [2]. Positive  $V_{\text{TH}}$  is obtained by fully recessing the  $\text{AlGaN}$  barrier at the gate region. Different gate dielectrics such as  $\text{SiO}_2$  [3], [4],  $\text{SiN}_x$  [4] and  $\text{Al}_2\text{O}_3$  [5], [6] have been studied. Among these oxides,  $\text{Al}_2\text{O}_3$  is commonly used due to its high permittivity and high band gap [7], yet the  $\text{Al}_2\text{O}_3/\text{GaN}$  gate stack can suffer from  $V_{\text{TH}}$  instability and low thermal stability [5], [8]. The latter hinders the use of high-temperature annealing to increase  $V_{\text{TH}}$  and reduce  $V_{\text{TH}}$  hysteresis. However,  $\text{AlSiO}$  is a promising dielectric with higher thermal stability [9], [10] and lower Flat-Band Voltage hysteresis ( $\Delta V_{\text{FB}}$ ) [9], [11]. Increasing the Si content in  $\text{AlSiO}$  was also reported to decrease hysteresis and increase the conduction band offset [11], [12]. If the beneficial impact of Post-Deposition Annealing (PDA) was studied for  $\text{Al}_{0.78}\text{Si}_{0.22}\text{O}_x$  [10], the impact of PDA for higher Si content has not been investigated. Hence in this work, we investigate the impact of high-temperature PDA on  $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$  with MOS capacitances (MOSCAPs) electrical measurements and physico-chemical analyses.

## 2. Experimental

19 nm  $\text{Al}_{0.5}\text{Si}_{0.5}\text{O}_x$  (alternating  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$ ) with a silicon content of 50% or 30 nm  $\text{Al}_2\text{O}_3$  layers were deposited by Atomic Layer Deposition (ALD) on MOCVD as-grown n-GaN ( $N_D=5 \times 10^{17} \text{ cm}^{-3}$ )/Si 200mm wafer. For AlSiO, the ALD precursors for Al, Si and O sources were trimethylaluminium, tris(dimethylamino)silane and ozone, respectively. For  $\text{Al}_2\text{O}_3$ , the precursors for Al and O were trimethylaluminium and water. Before ALD, a wet sequence without Na or K and ending with HF was performed on the GaN wafer surface. After ALD, the wafer was cut into  $1.5 \times 1.5 \text{ cm}^2$  AlSiO samples and underwent PDA at  $650^\circ\text{C}$ ,  $750^\circ\text{C}$ ,  $850^\circ\text{C}$  and  $950^\circ\text{C}$  for 3min under  $\text{N}_2$ . Then MOSCAPs test structures (**Fig.1**) were fabricated with Ni/Au deposited by e-beam evaporation.

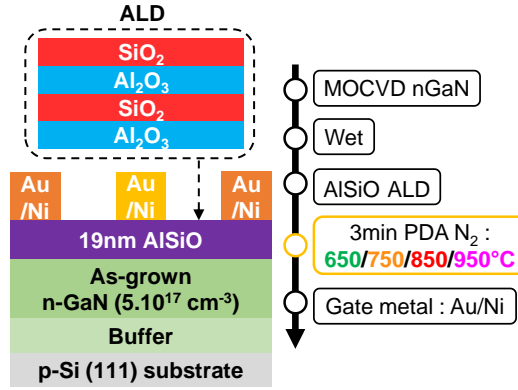


Fig.1: MOSCAPs process flow with different PDA temperatures.

Bidirectional C-V measurements were carried out at 1 kHz with a voltage sweep from -4V to 6V and back to -4V. C-V measurements were performed at three different measuring temperatures:  $25^\circ\text{C}$ ,  $150^\circ\text{C}$  and  $200^\circ\text{C}$ . The Flat-Band Voltage ( $V_{\text{FB}}$ ) was extracted by using the theoretical Flat-Band Capacitance ( $C_{\text{FB}}$ ) calculated as:

$$C_{\text{FB}} = C_{\text{OX}} C_{\text{D}} / (C_{\text{OX}} + C_{\text{D}}) \quad (1)$$

$$\text{with } C_{\text{D}} = \sqrt{kT \epsilon_{\text{GaN}} \epsilon_0 / (q^2 N_{\text{D}})} \quad (2)$$

Where  $C_{\text{OX}}$ ,  $k$ ,  $T$ ,  $\epsilon_{\text{GaN}}$ ,  $\epsilon_0$  and  $q$  are respectively the oxide capacitance, the Boltzmann constant, the temperature in Kelvin, the relative GaN permittivity, the vacuum permittivity and the electron elementary charge. Bias Temperature Stress (BTS) was carried out to calculate mobile charges density by stressing the gate at 1.8 V for 10 min at  $200^\circ\text{C}$ . After 10 min, the stress is maintained and the temperature is set to room temperature. Then at room temperature, a C-V measurement is performed and the procedure is repeated for the stress at -1.8 V. The mobile charges density is calculated as below:

$$Q_m = -C_{OX}(V_{FB}^{+1.8V} - V_{FB}^{-1.8V}) \quad (3)$$

These samples were also analysed by Transmission Electron Microscopy (TEM). Samples without metallization were analysed by Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) and Angle-Resolved Hard X-ray Photoelectron Spectroscopy (AR-HAXPES). ToF-SIMS was performed on a ToF-SIMS 5 with a 500 eV Cs<sup>+</sup> sputter gun, and both negative and positive ions were analysed with a 30 KeV Bi<sub>3</sub><sup>+</sup> ion beam. The Al<sub>0.5</sub>Si<sub>0.5</sub>O<sub>x</sub>/GaN interface was calibrated to where the reference bulk signal used for normalization drops by 50%. AR-HAXPES was performed at take-off angles of 42, 50 and 65° on a Phi Quantes equipped with a monochromatic Cr K $\alpha$  X-Ray source ( $h\nu=5414.7$  eV), allowing the analysis of buried interfaces. The Ga2p<sub>3/2</sub> spectrum was used to analyse the Ga-O bond with respect to Ga-N by using the model in [13]. The GaO<sub>x</sub> thickness was determined with the equation in **Fig.7.b**). The ratio  $I_{GaN}^{\infty}/I_{GaO}^{\infty}$  was experimentally evaluated as 0.873 by using GaN and Ga<sub>2</sub>O<sub>3</sub> reference samples, and  $\lambda$ , the inelastic mean free path of Ga2p<sub>3/2</sub> photoelectrons in Ga<sub>2</sub>O<sub>3</sub>, was calculated to be 5.831 nm using the TPP-2M model. The 50% Si composition (or  $100 \times Si/(Al + Si)$ ) for the different PDA temperatures was confirmed with HAXPES quantification at 75°, as represented in **Table 1**.

PDA	w/o PDA	650°C	750°C	850°C	950°C
$100 \times Si/(Al + Si)$	50%	49%	50%	49%	46%

Table 1: Silicon composition extracted by HAXPES for the different PDA temperatures, the silicon content staying around 50%.

### 3. MOSCAPs electrical results

The C-V at different temperatures and the extracted Flat-Band Voltage hysteresis ( $\Delta V_{FB}$ ) are reported in **Fig.2** and **Fig.3.a**) respectively. No C-V characteristics were measured for the 950°C sample due to large leakage current in the oxide. For measurements at room temperature, AlSiO MOSCAPs exhibit slightly lower  $\Delta V_{FB}$  compared to Al<sub>2</sub>O<sub>3</sub>, but increasing the PDA temperature up to 750°C leads to  $\Delta V_{FB}$  decrease. With 850°C PDA  $\Delta V_{FB}$  becomes unexpectedly negative (reversed hysteresis). Increasing the measuring temperature at 200°C reveals a reversed  $\Delta V_{FB}$  for all AlSiO samples, which was already reported in literature but for higher Si content in AlSiO (73%) at room temperature, and on N-face GaN [11]. The presence of reversed hysteresis may originate from mobile charges [14]. BTS measurements reported in **Fig.3.b**) confirm the presence of  $2.3\sim 2.4 \times 10^{12}$  cm<sup>-2</sup> of mobile charges for the samples with and without 850°C PDA. Moreover, C-V at different frequencies (not shown here) reveal a density of interface states under  $10^{10}$  eV<sup>-1</sup>.cm<sup>-2</sup>.

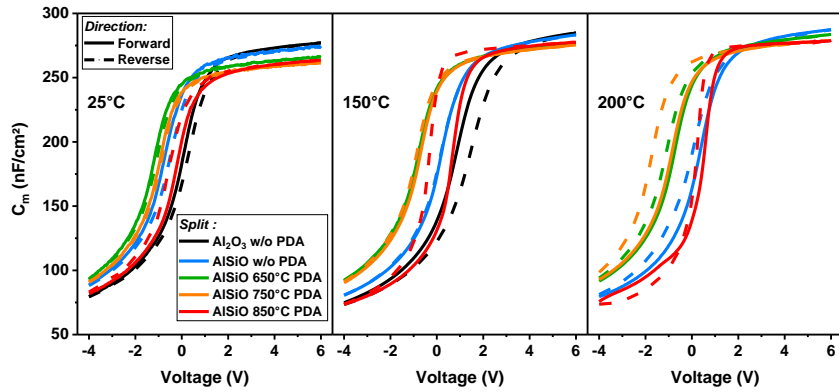


Fig.2: Bidirectional C-V measurements (median of five measurements). No C-V measurements are shown for 950°C PDA because of large leakage current, probably due to crystallization of AlSiO (c.f. Fig.6).

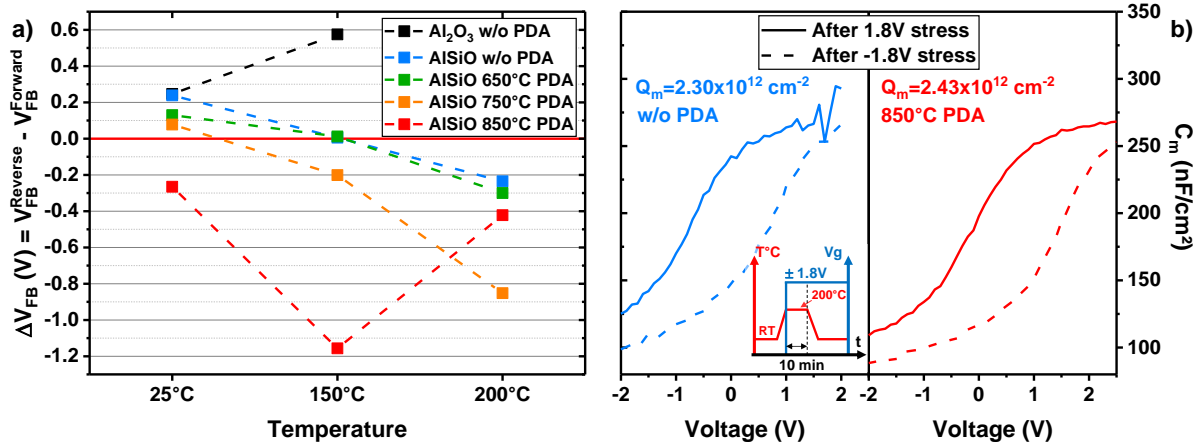


Fig.3: a) Extracted  $\Delta V_{FB}$  from C-V measurements. Increasing the measuring temperature reveals reversed hysteresis for all AlSiO samples; b) BTS measurements on AlSiO samples without PDA and with 850°C PDA. Similar amount of mobile charges is calculated for the AlSiO samples without PDA and with 850°C PDA.

#### 4. Discussion with physico-chemical analyses

The mobile charges observed in C-V and BTS measurements may come from the  $\text{Na}^+/\text{K}^+$  contamination [14] detected by ToF-SIMS on AlSiO samples with and without 850°C PDA (Fig.4).

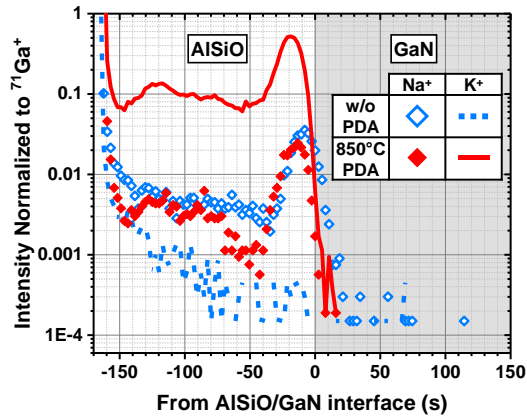


Fig.4: ToF-SIMS depth profiles of  $K^+$  and  $Na^+$  on AlSiO samples without and with 850°C PDA. Both samples have  $Na^+$  and  $K^+$  contamination.

The high PDA temperature does not cure their presence but further increases the presence of  $K^+$ . Their origin is currently under investigation and it's most probably due to the process environment. Their origin might not be the wet cleaning because it does not contain Na or K and because the same cleaning was used for the  $Al_2O_3$  sample which does not present reversed hysteresis. However, OH groups are reduced until 850°C PDA (**Fig.5.a**). Since they can trap electrons [15], their reduction could explain the decreased positive hysteresis measured at room temperature for PDA temperatures under 850°C. Other sources of electron trapping exist such as oxygen vacancies ( $V_o$ ) but it was reported that Si reduces their presence in AlSiO [16]. Since similar amount of mobile charges are extracted for samples with or without 850°C PDA, the difference in reversed hysteresis for the different PDA temperatures can be partially explained by their respective different amounts of electron traps. The negative trapped electron charges would then compensate for the effect of positive mobile charges. Hence, increasing PDA temperature seems to reveal the mobile charges by reducing the electron traps.

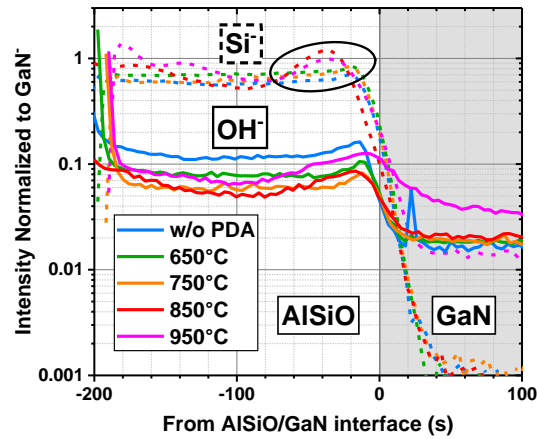


Fig.5: ToF-SIMS depth profiles of  $\text{OH}^-$  and of  $\text{Si}^-$ . Increasing PDA temperature reduces  $\text{OH}^-$  content to a minimum at  $850^\circ\text{C}$ , but from  $850^\circ\text{C}$  PDA the silicon accumulates at the AlSiO/GaN interface (same behaviour observed for Al- not shown here).

Moreover, high-temperature PDA further deteriorates the AlSiO layer. The absence of C-V characteristics for  $950^\circ\text{C}$  PDA is indeed due to crystallized regions observed by TEM (Fig.6) inducing large leakage current. Smaller regions are also observed for the  $850^\circ\text{C}$  PDA sample but they do not seem to affect the C-V measurements. However, they could accelerate the mobile charges movement since the  $850^\circ\text{C}$  sample has a reversed hysteresis for a C-V at room temperature [17]. This start of crystallization happens at a lower temperature than reported by Kikuta and co-workers for  $\text{Al}_{0.78}\text{Si}_{0.22}\text{O}_x$  [10], a possible explanation being the different oxygen source. In fact, for  $\text{HfO}_2$ , poorer oxygen content leads to lower crystallization temperature [18].

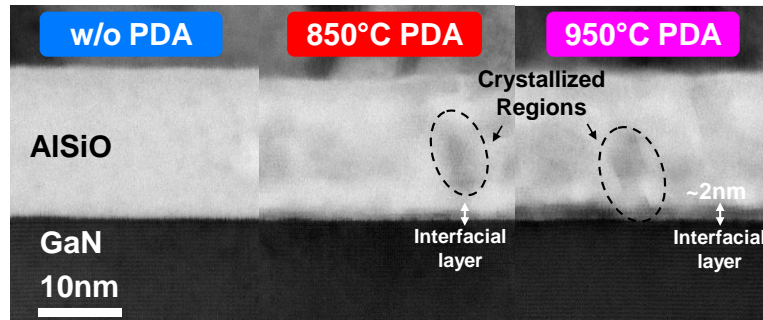


Fig.6: TEM images for AlSiO samples without and with PDA at  $850^\circ\text{C}$  and  $950^\circ\text{C}$ . Both PDA samples present crystallized regions and interfacial layers. But  $950^\circ\text{C}$  PDA sample has a thicker interfacial layer and more crystallized regions.

Likewise, inhomogeneous Si (and Al) distribution appears for PDA over  $750^\circ\text{C}$ , as shown by ToF-SIMS  $\text{Si}^-$  profiles (Fig.5.b)), demonstrating that AlSiO is already degraded at this PDA temperature range. PDA above  $750^\circ\text{C}$  also leads to an interfacial layer, with a  $\sim 2$  nm layer for  $950^\circ\text{C}$  PDA (Fig.6). This layer is identified as interfacial gallium oxide ( $\text{GaO}_x$ ) as shown by ToF-SIMS  $^{71}\text{GaO}^-$  profiles (Fig.7.a)) and  $\text{GaO}_x$  thicknesses as extracted from AR-HAXPES (Fig.7.b)). The thickness increasing after  $750^\circ\text{C}$  PDA correlates well with the  $^{71}\text{GaO}^-$

profile extension inside AlSiO. The GaN thermal oxidation is known to increase for temperatures higher than 750°C. Similarly to SiO<sub>2</sub> or HfSiO<sub>x</sub>, AlSiO with PDA over 750°C does not hinder the growth of interfacial GaO<sub>x</sub>. However, its presence does not lead to a higher interface states density.

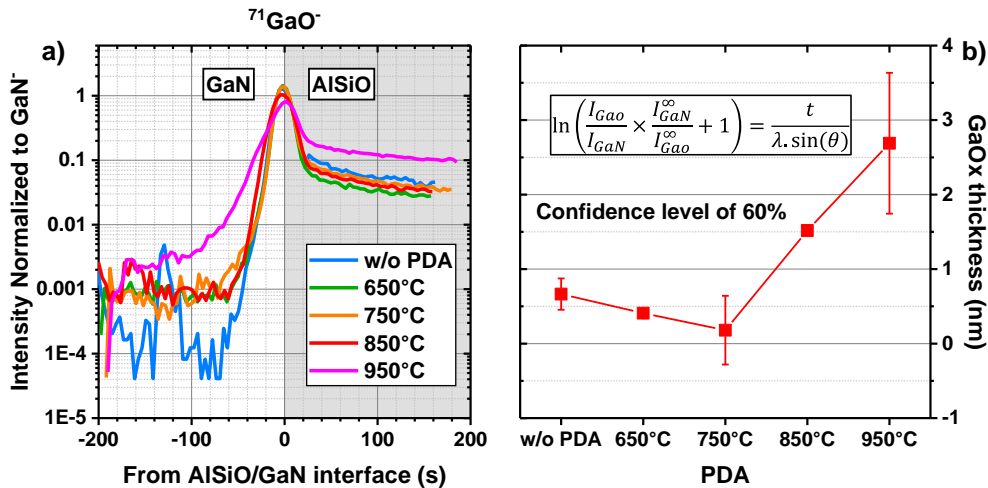


Fig.7: a) ToF-SIMS depth profiles of <sup>71</sup>GaO<sup>-</sup> and b) GaO<sub>x</sub> thickness extracted from varying the HAXPES take-off angle between 42/50/65°. The <sup>71</sup>GaO<sup>-</sup> profile extends towards AlSiO for PDA temperature higher than 750°C, correlating to the increased GaO<sub>x</sub> thickness after 750°C PDA.

## 5. Conclusion

We have investigated the impact of high PDA temperatures on Al<sub>0.5</sub>Si<sub>0.5</sub>O<sub>x</sub>/n-GaN samples. Reversed hysteresis is observed for all AlSiO samples and seems to be related to mobile charges (Na<sup>+</sup>/K<sup>+</sup>). Higher PDA temperatures seem to reduce electron trapping by reducing hydroxyl groups, but PDA over 750°C leads to inhomogeneous atomic composition, GaO<sub>x</sub> growth and to a beginning of crystallization. The optimal PDA temperature is 750°C, with more analyses with different Si% and oxygen source to be performed.

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