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# Processing and electrical characterization of SiC-on-Insulator structures

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Ion slicing technologies are becoming increasingly popular among silicon carbide (SiC) processing techniques, whether for manufacturing substrates for power electronics [1], [2] or integration platforms for optical devices [3]. For either of these applications, one has to ensure the excellent quality of the transferred layer. In this extent, silicon carbide-on-insulator (SICOI) structures can be of great interest in order to probe the properties of the transferred layer alone. The electrically insulating oxide layer between the receiver substrate and the transferred layer allows one to measure the electrical properties of the transferred layer, and to investigate the deep level defects created by the ion implantation step [4]. We thus report the fabrication process of such a SICOI structure, using a monocrystalline 4H-SiC wafer as the handle substrate. The choice of the later minimizes the difference of the thermal dilatation coefficients of the transferred layer and the substrate, as compared to the use of a Si handle [5], as well as allowing to benefit of a higher melting point. Doing so enables to access higher annealing temperatures, and to understand more acutely the effects of such manufacturing processes.

The substrates were processed as described on the Fig. 1. Layers of tetraethoxysilane (TEOS) were deposited on both the donor (550 nm) and the receiver (3500 nm) substrates (both of  $4 \cdot 10^{18} \text{ cm}^{-3}$  n-doped bulk 4H-SiC), before dehydrogenation at  $1100^\circ\text{C}$  (1 hr) under a  $\text{N}_2$  atmosphere. The donor wafer was then  $\text{H}^+$ -implanted at room temperature, 160 keV and at a dose of  $5,5 \cdot 10^{16} \text{ at.cm}^{-2}$ . The two substrates were directly bonded after cleaning and polishing steps. A subsequent thermal treatment of  $950^\circ\text{C}$  during 1 hr was then applied in order to split the implanted (donor) wafer at the maximum hydrogen concentration depth (i.e. around 700 nm). The SICOI substrates are eventually obtained after 1- a polishing, and 2- a final annealing step (which temperature ranges between  $1200^\circ\text{C}$  and  $1600^\circ\text{C}$ ) – benefitting both the bonding strength and the transferred layer crystal quality. The thicknesses of the oxide and transferred SiC layers of the resulting substrates were found to be of  $3.25 \mu\text{m}$  and  $525 \text{ nm}$ , respectively, with  $\pm 9.3 \%$  and  $\pm 14.2 \%$  variation over the entire wafer surface (see Fig. 2).

The Fig. 3 shows the doping level and the electron mobility inferred from Hall measurements. Both are found to be beneficially affected by a higher annealing temperatures, proof of a progressive healing of the electrical properties of the transferred material. After  $1600^\circ\text{C}$  anneal, one can even assess the recovery of a doping level and of an electron mobility close to those of the initial donor ( $3 \cdot 10^{18} \text{ cm}^{-3}$  and  $76 \text{ cm}^2/\text{V.s}$ , respectively). The TLM I-V measurements were carried out at several temperatures, ranging from RT to  $200^\circ\text{C}$ . The decrease of the electrical resistivity inferred from these measurements with increasing measuring temperature, shown on Fig. 4, indicates that electrical conduction mechanisms are subjected to ionization processes, which energies depend on the final annealing temperature. One can then calculate electrical compensation ratios for each one of these samples. Those we determine here range from 10 % (after  $1200^\circ\text{C}$  anneal) to 0 % ( $1400^\circ\text{C}$  and over).

SICOI substrates can thus be used as a tool for probing the electrical properties of a thin 4H-SiC layer transferred using an ion slicing technology. Hall and TLM measurement show an evolution of these properties with increasing annealing temperature: reduced resistivity, higher doping activation and higher electron mobility. Further measures of transistor effect and photoluminescence will now be carried out to highlight the presence of any depletion layer or any deep level defects inside the material.

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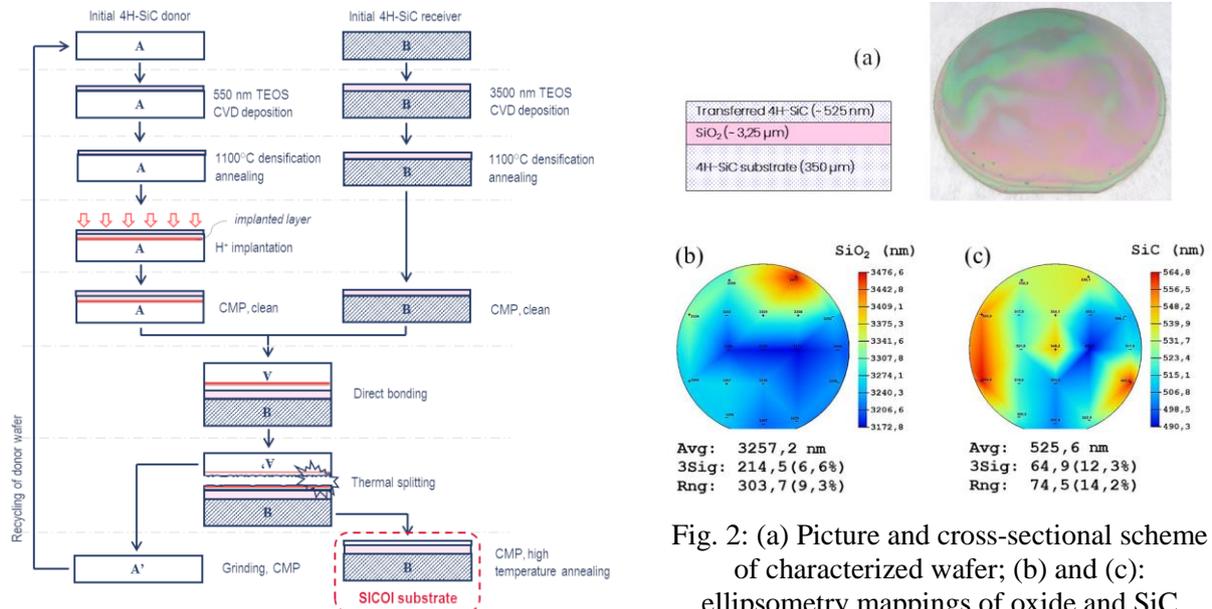


Fig. 1: Process flow of the SICOI substrates.

Fig. 2: (a) Picture and cross-sectional scheme of characterized wafer; (b) and (c): ellipsometry mappings of oxide and SiC thicknesses, respectively.

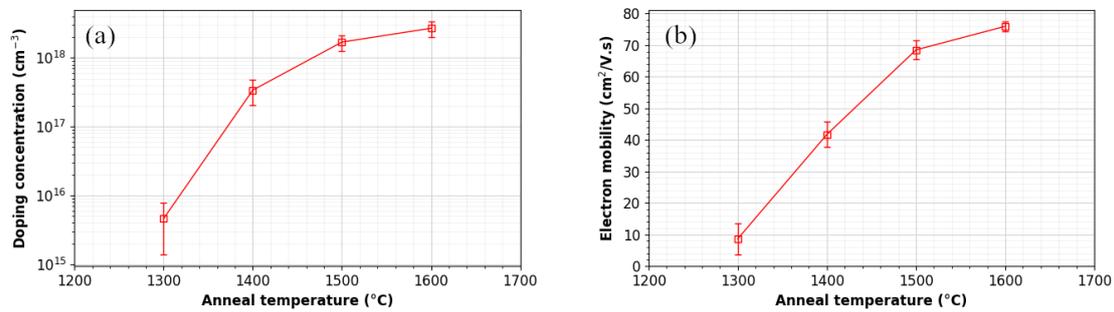


Fig. 3: Hall doping level (a) and electron mobility (b) measured at room temperature as a function of the annealing temperature.

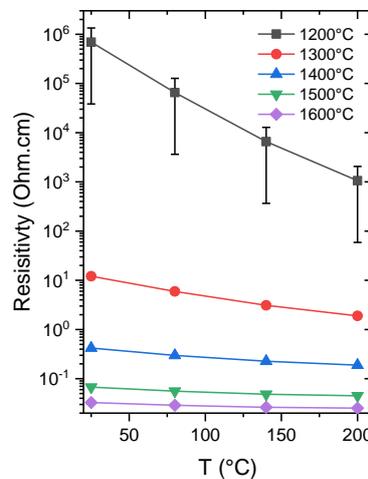


Fig. 4: Transferred layer resistivity values extracted from TLM measurements as a function of the measuring temperature for samples annealed between 1200°C and 1600°C.