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CMOS Pixel Circuit for GaN Micro-LED control in Very High Luminance Applications

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ABSTRACT

GaN micro-LED technology offers high luminance level, which is a strong requirement for microdisplays used in augmented reality, as well as large display applications. Their electro-optical characteristics differ from the commonly-used OLEDs. So new circuitry with higher driving capabilities for the pixel control needs to be developed. This paper discusses the architecture of such a CMOS pixel, suited for GaN micro-LED control.

1 INTRODUCTION

Display devices are already found in many applications, and tend to spread more and more. They can be as large as a wall, or as small as a coin, but in every case, we expect them to enable good watching quality. Classic demand asks for very high resolution, low pixel pitch, high contrast, and high bit depth. In outdoor applications, or for large displays, high luminance is also an important issue.

Indeed, luminance dilution on large panel displays imposes higher luminance at source level. For example, a smartphone screen of 1000cd/m^2 with a $50\mu\text{m}$ pixel pitch and a LED size of $5\mu\text{m}$ leads to a luminance of 100kcd/m^2 . Dilution is even bigger for a computer, or TV screen, thus demanding even higher luminance.

For microdisplay, luminance at source level is at least 100kcd/m^2 to several Mcd/m^2 . But very few light sources can deliver such a luminance level, although needed in these applications. Despite a low maturity level, GaN micro-LEDs could be a good candidate, with high contrast, high brightness, high efficiency as well as good lifetime [1].

Implementation of an array of GaN micro-LEDs was demonstrated many years ago [2]. High resolution array of GaN micro-LEDs have also been demonstrated [3], but don't provide the needed luminance for the whole array.

High resolution display devices require active matrix backplane to enable an accurate control of the array. This paper discusses pixel control solutions that could be implemented, regarding the specificity of GaN micro-LED technology, as well as their maturity level.

2 GAN MICROLEDS ELECTRO-OPTICAL CHARACTERISTICS

Considering the electro-optical Luminance-Voltage characteristic of a $7\mu\text{m}$ GaN micro-LED, shown Fig. 1, one

can deduce the important dispersion on the characteristic, whatever the voltage. So voltage control is less suitable for a GaN micro-LED than other devices like OLEDs.

A study on Luminance-Current curve, Fig. 2, measured for the same sample of GaN micro-LEDs, shows that Luminance is also very sensitive to current variation at low luminance level. But for high current densities, the curve shows less dispersions. It may be easier to bias LED with a current control circuit.

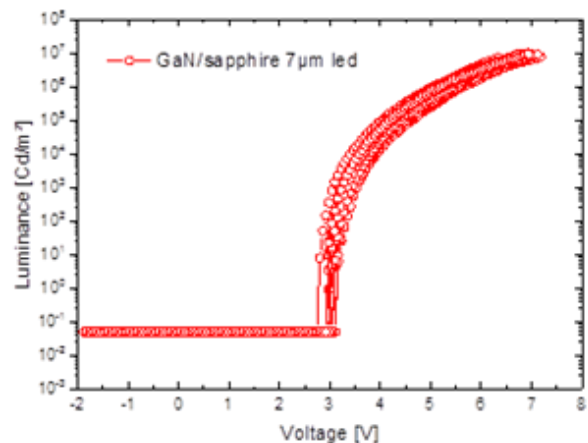


Fig. 1 Measured Luminance vs. Voltage

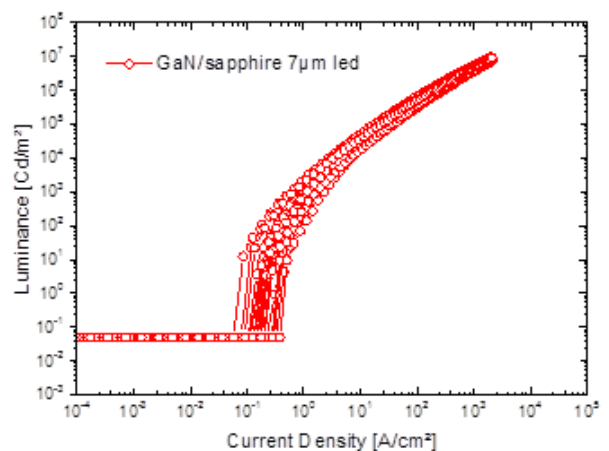


Fig. 2 Measured Luminance vs. Current

It seems also preferable to apply an individual correction to each LED to ensure a good luminance uniformity, and avoid visible imperfections that could degrade display performance.

3 DISCUSSION ON LED BIAS STRATEGY

In this paragraph, pixel bias is discussed. Commonly used architecture are compared with a proposed one.

3.1 LCD like pixel bias

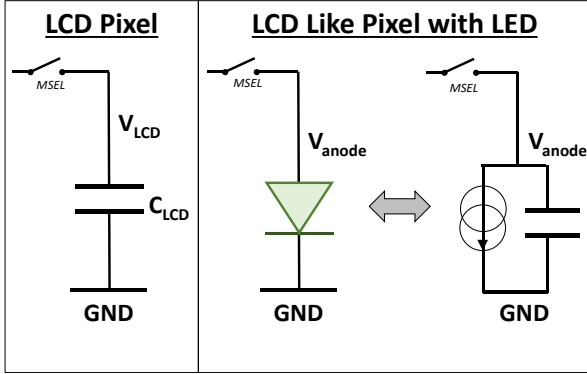


Fig. 3. LCD-like pixel bias for a LED

The bias of a LCD pixel consists in enabling a selection switch, and writing a voltage value on C_{LCD} floating electrode V_{LCD} . C_{LCD} acts as a storage capacitor and keeps the voltage V_{LCD} almost constant when the selection switch is disabled.

For an emissive pixel, with OLED or GaN micro-LED technology, this implementation is not possible. Indeed, when selection switch is enabled, bias value is set to V_{anode} and LED emission begins. But as soon as selection switch is disabled, LED parasitic capacitor, supposed to act as a storage capacitor, will start to discharge because of LED current consumption.

This is the reason why pixel with emissive source are implemented with other bias solutions.

3.2 AMOLED-like pixel bias

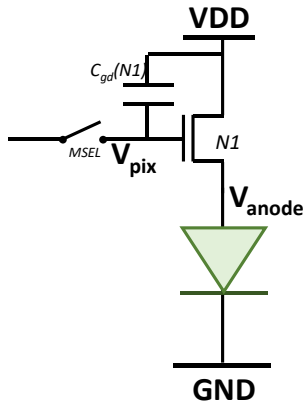


Fig. 4. Typical bias in AMOLED pixel

Most of AMOLED displays use a pixel bias control

similar to Fig. 4. In this solution, two transistors are integrated. As for every active matrix, a selection switch is necessary. A second transistor, a NMOS, if OLED cathode is routed to the common ground, acts as a "source follower". The control principle relies on the formula (1), derived from the classical source follower voltage gain expression.

$$\Delta V_{anode} = \frac{g_{m1} \times (r_{dsN1} // R_{LED})}{1 + g_{m1} (r_{dsN1} // R_{LED})} \Delta V_{pix} \quad (1)$$

Generally, $\frac{1}{g_{m1}} \ll r_{ds1} // R_{LED}$ so $\Delta V_{anode} \approx \Delta V_{pix}$,

meaning V_{anode} will follow the variations of V_{pix} . So when the selection switch is enabled, V_{pix} voltage is set and V_{anode} will follow voltage variation consequently, LED emission will begin with a luminance $L(V = V_{anode})$. When selection switch is disabled, V_{pix} value is stored on $N1$ parasitic capacitance $C_{gd}(N1)$ until a new V_{pix} value is written.

This topology is quite compact because it needs only two transistors.

The selection switch must be active long enough to reach the required accuracy, following equation (2). V_{pix} must be close enough to V_{DAC} , the analog value generated outside the pixel array, depending on the grey level to be displayed.

$$V_{pix} = V_{DAC} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (2)$$

So V_{pix} accuracy will depend on "t" (ON time of the selection switch), and τ (the time constant, depending on the column bus parasitic resistance and capacitance). τ is often tens of nanoseconds, whereas "t" is about tens of microseconds. So, if DAC output buffer enables enough current for the bus charge, settling time should not be a limitation with this topology.

But if V_{pix} value is stored thanks to $N1$ parasitic capacitance, a drop on V_{DD} supply will directly impact V_{pix} value, and consequently, V_{anode} , directly resulting in a luminance drop. This effect may be negligible in low luminance applications, but in the case of outdoor or large panel display applications, this effect may be visible to human eye.

In addition, previous paragraph explained that voltage control was not suitable to GaN LEDs due to their highly dispersed electro-optical characteristics.

Then, a third topology is discussed.

3.3 Proposed bias strategy

Another bias solution consists in controlling LED current I_{LED} instead of its voltage V_{anode} . In the case of a common cathode LED, the bias transistor is then a PMOS. Current control follows the formula (3)

$$I_{LED} = K \frac{W}{L} (V_{sg} - V_t)^2 \quad (3)$$

Where I_{LED} is the LED current, K is a technological parameter, W and L are P1 width and length chosen by design, V_{sg} is the gate source voltage, V_t is P1 threshold voltage.

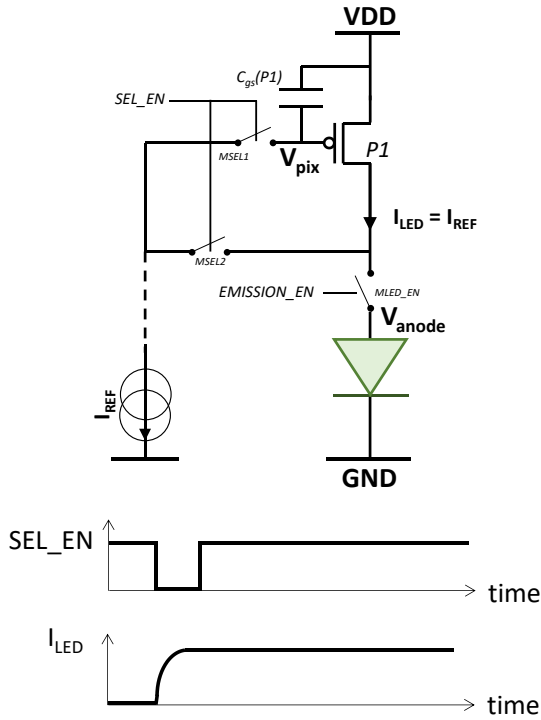


Fig. 5. Proposed pixel bias with timing of selection switches

For a current source built with a PMOS transistor, V_s is tied to VDD, and the current follows a quadratic variation with the gate voltage V_{pix} (see formula (3))

For some architecture, LED current biasing consists in the initialization of V_{pix} thanks to a voltage DAC. But if a voltage drop occurs on VDD, or if P1 threshold voltage suffers from dispersions, LED current could differ very much from the expected value. Then, the proposed solution relies on a current initialization. The impact on the pixel architecture is the addition two switches. During current initialization, both switches MSEL1 and MSEL2 are enabled, and P1 is in a diode connected configuration. While current initialization is running, LED emission is inhibited by turning OFF switch MLED_EN, preventing current source P1 from flowing through the LED and distort current initialization.

Special attention must be paid to ensure that the retention of the current information is good enough during a frame time. Moreover, charge injection caused by selection switches turning OFF, as well as flicker effects should be studied. To minimize those effects, storage capacitance must be larger than in the source follower configuration, resulting in larger transistor P1, or implementation of an additional capacitance. Thus the pixel area of the proposed architecture might be more important than that of the source follower architecture.

For the current initialization, the settling time depends on the ratio of current value on bus parasitic capacitance. For low luminance applications, this could be a limitation, but for high luminance, high current densities are

necessary and initialization is in the order of the ON duration of selection switches.

The expression (3) shows that the I_{LED} initialization depends on V_s voltage, corresponding to the local VDD supply. Consequently, if a voltage drop occurs before or during the current initialization, V_{pix} will adjust to deliver appropriate I_{LED} . If the supply voltage drop occurs after initialization, V_{pix} will fall almost like VDD and conserve its V_{sg} value, thus keeping good current value. This architecture doesn't suffer from limitation due to voltage drop, which is very important for high power densities applications.

Finally, LED Luminance-Current characteristic shown Fig. 2 illustrates that current drive is more appropriate than voltage bias, as explained in section 2.

To ensure good luminance uniformity for high luminance application, current drive approach is preferable.

4 Proposed CMOS pixel

An example of implementation is illustrated Fig. 6.

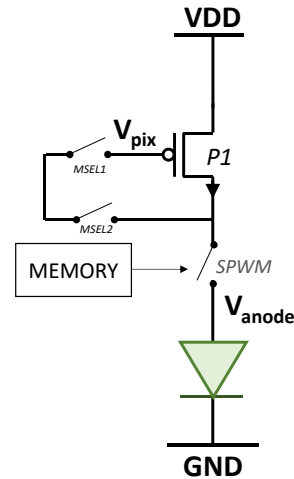


Fig. 6. Our CMOS pixel that includes the proposed bias solution for correcting LED dispersions and a pulse width modulation for controlling the luminance

The control circuit uses the bias solution proposed previously, coupled with a modulation of the ON state duration of the LED. Several current values will be possible to correct LED mismatch, while digital memory will implement the grey level by turning ON or OFF SPWM switch, and allow or avoid LED emission.

The pixel consists in a 3D stack of a GaN layer providing the emissive element, with a CMOS layer, providing control of the light source. The final pixel pitch is close to $10\mu m$, which is bigger than OLED pixels. Some improvement are considered to lower pixel area, by using a more aggressive CMOS node, with 3.3V transistors instead of 5V transistors, for example.

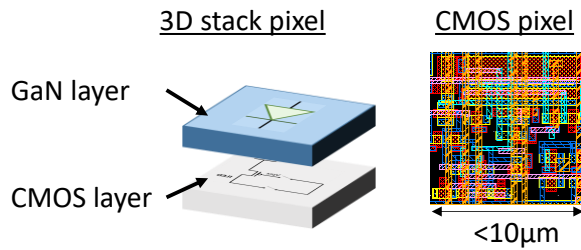


Fig. 7. Example of a GaN pixel controlled with a CMOS circuit. Left: 3D stack principle and right: CMOS layout

The luminance is expected to reach at least 1Mcd/m^2 at source level, much higher than the luminance of OLED microdisplays, about 10kcd/m^2 [4].

5 CONCLUSION

This paper discussed on classical pixel architecture, new aspects brought by GaN LED technology and the demand for high power densities. A new pixel topology was proposed to overcome limitations of the classical pixel control approach.

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