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# Disruptive approaches towards Energy Efficient VLSI Technologies

Olivier Faynot<sup>1</sup>, Sylvain Barraud<sup>1</sup>, Theophile Dubreuil<sup>1</sup>, Elisa Vianello<sup>1</sup>, Emmanuel Ollier<sup>1</sup>, Denis Dutoit<sup>2</sup>, François Andrieu<sup>1</sup>, Fabien Clermidy<sup>2</sup>, Julien Arcamone<sup>1</sup>

<sup>1</sup> CEA-Leti, <sup>2</sup> CEA-List, University Grenoble Alps, 17 rue des Martyrs, 38054 Grenoble Cedex, France

E-mail: [olivier.faynot@cea.fr](mailto:olivier.faynot@cea.fr)

**Abstract**—Nowadays, the data deluge related to data generation, transfer, compute and storage, induces a huge increase of power consumption related to the usage of integrated circuits. New technologies and concepts are necessary to overcome the issue. This paper will give an overview all the main ongoing developments that will significantly improve the Power efficiency of Integrated Circuits. Disruptive computing, such as Quantum or In Memory Computing are well known to provide significant improvement. Novel Non Volatile Memories, coupled with Neuromorphic architectures can also be an enabler of power efficient electronic. As data transfer is the main source of Power consumption, 3D integrations can enable chiplet approaches that reduce the length of interconnects.

## I. INTRODUCTION

World's digitalization induces a tremendous increase of data generation, close to 500 Zetabyte by 2030. This data deluge leads to a dramatic increase of energy consumption, not sustainable on a medium term. Technological breakthrough must be developed in order to improve by a factor of at least 1000, the Power efficiency of electronic devices. Since many years, CMOS scaling was able to reduce the power consumption when switching from the previous node to the next one. This was well known as the Moore's law. Today, with the huge increase of IC's usage, disruptive approaches are mandatory in order to reduce the energy consumption of semi-conductors.

## II. CMOS OPTIONS

Technology scaling, following Moore's law has always been the most efficient way to reduce the Power consumption from one node to another. An alternative approach appeared below 28nm, with the so-called FD-SOI technology. Besides key advantages related to its lower parasitics and outstanding RF performance for a Silicon based platform, this technology offers a key feature to circuit designers: the Back Bias effect. This effect was disappearing in planar Bulk technologies and does not exist in FinFET technology. On the contrary, this effect exists and is very efficient on FD-SOI technology. Such effect allows to significantly modulate the power consumption of integrated circuits, as illustrated in Fig. 1.

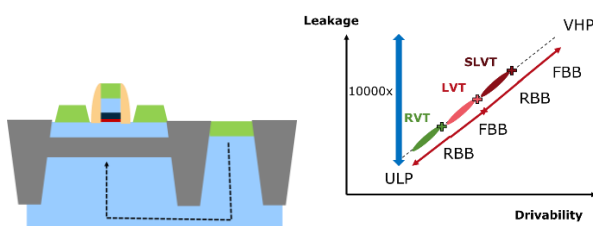


Fig. 1 : Back Biasing effect on planar FD-SOI technology

Such effect allows a significant improvement of the tradeoff between operation frequency and Power consumption, with up to 450% frequency improvement demonstrated on Cortex M4F [1].

## III. DISRUPTIVE COMPUTING

### A. Bio inspired resource-limited Edge AI hardware

As AI becomes increasingly integrated into our daily lives, there is a crucial need to address its energy consumption and storage requirements. Edge computing offers a potential solution by processing data in real-time at the source where sensors are located. However, this requires compact and low-power computer systems with low latency to be effective.

To meet these requirements, hybrid resistive memories-Complementary Metal-Oxide Semiconductor (CMOS) neuromorphic architectures with their in-memory event-driven computing capabilities provide an ideal hardware substrate. To showcase the full potential of these systems, we recently designed and fabricated an event-driven object-localization system based on the neuroanatomy of barn owls. Our system uses state-of-the-art piezoelectric ultrasound transducer sensors and a neuromorphic computational map based on resistive memories [2]. We have focused on the task of acoustic-based object localization. In particular, the owl's localization system encodes the time-of-flight of sound waves coming from prey to calculate its position. Our system implements a similar approach, using a single emitting piezoelectric microelectromechanical systems (pMUT) membrane operating at 111.9 kHz and two reception pMUT membranes to emulate the owl's ears. The system also includes a neuromorphic computational map that was fabricated by co-integrating a 130-nm CMOS processor with hafnium-dioxide resistive memory devices. The results of our experiments have revealed the potential of our approach, with orders of magnitude greater energy efficiency than a microcontroller performing the same task. This work highlights the promise of edge computing and neuromorphic architectures in meeting the energy consumption and storage requirements of AI systems.

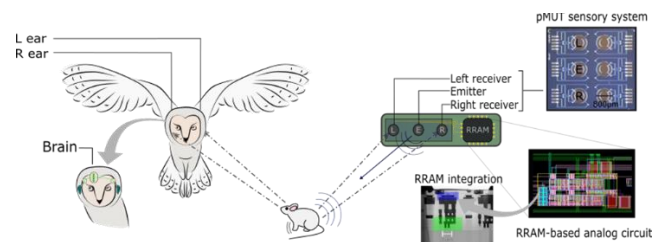


Fig. 2 : Object localization system in barn owls and the proposed bio-inspired technology

### B. Memory-centric High-Dimensional computing

Among alternative brain-inspired computing paradigm, High-Dimensional Computing (HDC), based on random distributed representation, offers a promising way for learning and classification tasks. Unlike conventional computing, HDC computes with (pseudo)-random hypervectors (HVs) of D-dimension. This implies significant advantages (Fig. 3): a simple algorithm with a well-defined set of arithmetic operations (Multiplication /Addition /Permutation), with fast and single-pass learning that can benefit from a memory-centric architecture (highly energy-efficient and fast thanks to a high degree of parallelism).

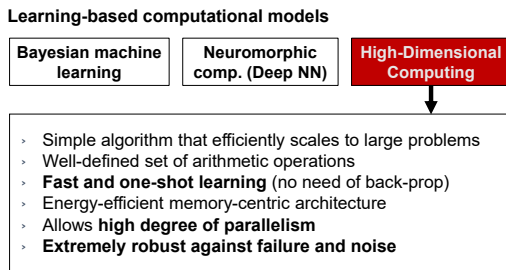


Fig. 3: Main characteristics of HDC algorithm vs other learning-based computational models.

The first hardware implementations of HDC based on emerging non-volatile memory provided a good accuracy of recognition with a promising energy efficiency, even if computing was partially produced within peripheral circuitry [3]. More recently, other 3D RRAM architectures have been proposed to implement the Multiply-Add-Permute (MAP) operations within the memory itself. Novel 3D RRAM architecture, which benefits from the high density of vertically stacked-channel transistors integrates the RRAM cell directly inside the drain contact of selector [4]. These highly compact 1T1R memory cells can be exploited to perform stateful in-memory MAP operations with a high level of parallelism (Fig. 4).

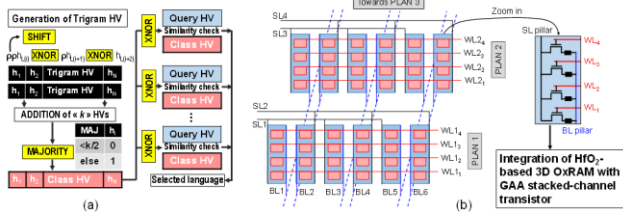


Fig. 4: (a) Overview of HDC algorithm for language recognition with the XNOR/MAJ/SHIFT operations, (b) Electrical schematic of a 3D 1T1R architecture based on the co-integration of HfO<sub>2</sub> OxRAM and GAA stacked-channel transistor.

### IV. 3D AND CHIPLET APPROACH

It is now well established that the combination of different kinds of integrated circuits by 2.5 and 3D technologies is a way to combine the best of different technologies and the

miniaturization to provide higher performance, flexibility and modularity with drastic energy efficiency benefits. Our current developments are focussed on developing i) the chiplet approach (Fig. 5) for high performance computing and Edge Artificial Intelligence, ii) multi-level architectures for image sensors and displays. Those developments are enabled by advanced 3D technological bricks (high density through silicon vias, wafer-to-wafer and die-to-wafer direct hybrid bonding, 3D sequential integration...) as illustrated on Fig.6.



Fig. 5: INTACT integrated circuit [5] with 6 chiplets stacked on an active interposer.

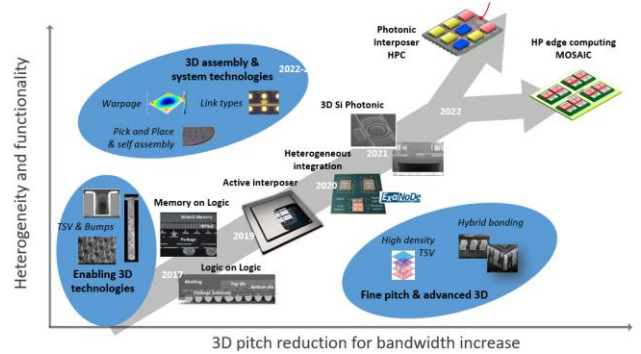


Fig. 6: Technological roadmap around 3D integration.

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