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Doped Channel SOI pMOS TCAD Description Including Floating Body Effects

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Abstract— In this work, we propose to investigate Silicon-on-Insulator (SOI) pMOS behavior modulation due to channel doping and its TCAD description. We first demonstrate channel doping variation due to the diffusion through the BOX and consumption during gate oxide formation. As the channel thickness is not so thin ($T_{Si}=22\text{nm}$), channel doping variation leads to different device operation from Fully Depleted (FD) to Partially Depleted (PD), going through an “in between” regime where Floating Body (FB) effects occurs. We finally propose TCAD methodology to account for channel doping variation in SOI pMOS.

Keywords— SOI; TCAD; Floating Body Effects

I. INTRODUCTION

SOI devices are studied since decades for many applications: Partially-Depleted SOI devices with thick silicon film ($>60\text{nm}$) are used for RF-SOI applications [1] while Fully-Depleted-SOI devices with thin SOI film ($<10\text{nm}$) are used for RF, digital and more Moore applications [2-4]. Floating Body (FB) effects are known to occur in PD-SOI devices [5-6] and can be canceled by body contact [7-8] while FD-SOI device are immune to FB effects thanks to the thin SOI film. Recently, SOI device on thin BOX with relatively thin film (22nm) have been proposed to fulfill imager application requirements with 3D sequential integration [9], where SOI film doping can be used for V_t centering. The objective of this paper is to determine the operation of such a SOI device and to propose the corresponding TCAD description, accounting for the SOI film doping.

II. DEVICE & TCAD DESCRIPTION

SOI pMOS is defined to fulfill imager applications requirements ($V_{DD}=2.5\text{V}$) [9]: SiO₂-polysilicon gate, 22 nm

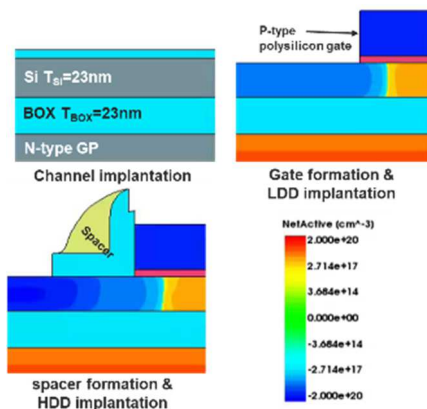


Fig. 2 : pMOS structure snapshots taken during TCAD process simulation

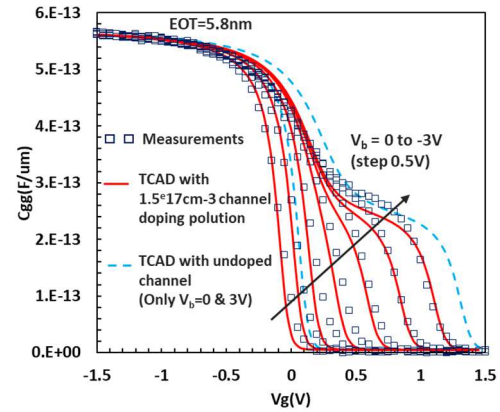


Fig. 1 : ($C_{GG}-V_G$) for $V_b=0$ to -3V from measurement and TCAD before and after tuning.

silicon film thickness (T_{Si}), 25 nm buried oxide thickness (T_{BOX}), 5 nm SiO₂ gate oxide grown by Rapid Thermal Oxidation (RTO) and a highly in-situ doped N-type Ground Plane (GP, Phosphorus, 2.10^{20}cm^{-3}). To build high V_T devices, channel doping is performed with BF₂ implantation for large dose variation (0 to 6.10^{13}cm^{-2}) and gate length L varies from 0.15 to $1\mu\text{m}$. TCAD is performed through process and device simulations. The complete process is simulated (Fig.1): channel implantation, gate formation (RTO and P-type polysilicon), LDD implantation, spacer formation and HDD implantation. Device simulations are then performed with Poisson equation, drift-diffusion, SRH recombination and ThinLayer(IAlmob) model including HighFieldSaturation.

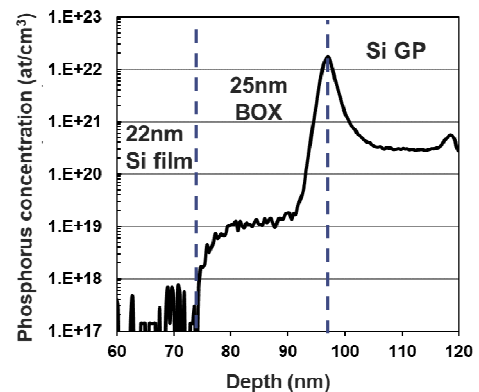


Fig. 3 : SIMS characteristic in the SOI substrate highlighting the phosphorus diffusion from the GP to the Si film.

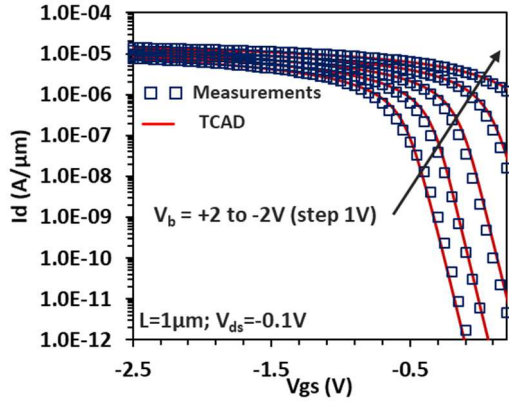


Fig. 4 : $L=1\mu\text{m}$ pMOS I_d - V_g for V_b variation at $V_d=-0.1\text{V}$ from TCAD and measurement.

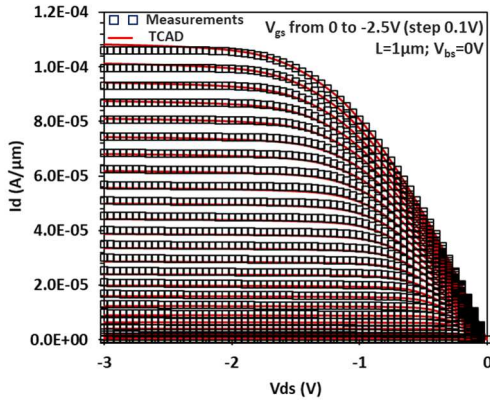


Fig. 5 : $L=1\mu\text{m}$ pMOS I_d - V_d for V_g variation from 0 to -2.5V at $V_b=0\text{V}$ from TCAD and measurement

III. UNDOPED CHANNEL SOI PMOS TCAD VALIDATION

We first focus on long channel ($L=1\mu\text{m}$) undoped channel SOI pMOS. Gate capacitance with gate voltage characteristic (C_{gg} - V_g , Fig.2) highlight that strong inversion regime is well described but there is lower TCAD threshold voltage V_T at $V_b=0$ & 3V than measurement (dashed blue line). To increase TCAD V_T , higher N-type channel doping is necessary and cannot come from the implantation steps, which are all P-type. From Secondary Ion Mass Spectrometry (SIMS) measurement performed on SOI substrate (Fig.3), we

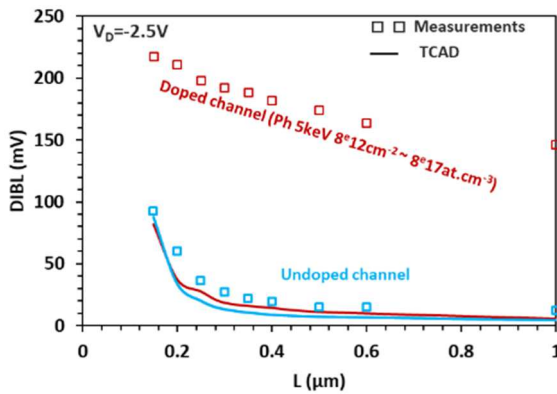


Fig. 7 : DIBL variation with gate length L for doped and undoped channel from TCAD and measurement

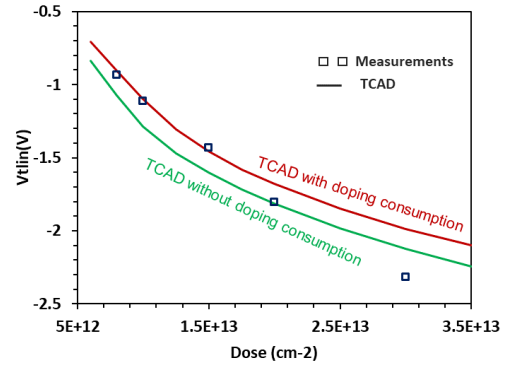


Fig. 8 : $L=1\mu\text{m}$ V_{tlin} variation with Phosphorus implantation dose from measurement and TCAD

demonstrate that $1\sim 4e17\text{cm}^{-3}$ Phosphorus diffused from the GP to the channel through the 25nm thick BOX. It is included in TCAD and C_{gg} - V_g for V_b variation is reproduced (red line on Fig.2), as well as long channel I_d - V_g at $V_d=-0.1\text{V}$ for V_b variation & I_d - V_d at $V_b=0\text{V}$ (Fig 4,5). The short channel TCAD description is then validated with DIBL variation versus gate length (Fig.6). An important DIBL degradation appears for doped channel, even for long gate and is not observed in TCAD.

IV. DOPED CHANNEL SOI PMOS TCAD DESCRIPTION

Linear regime threshold voltage V_{tlin} variation with channel implantation dose is overestimated by TCAD (green curve on Fig.7). SIMS (Fig.8) characterization reveals that as-implanted phosphorus profile in the 22nm silicon film is well predicted by TCAD (blue curves). However, it also highlights that the mean doping in the silicon film is significantly reduced after the gate oxide formation (Fig.8 dashed lines: $\sim 3.10^{18}\text{cm}^{-3}$ doping loss during the gate oxide formation). We attribute it to doping consumption in the surface during the oxidation and include it as a 3nm silicon etching in the process simulation. The phosphorus profile agreement between TCAD and SIMS is improved (Fig.8, red curves) as well as the V_{tlin} variation (red curve on Fig.7) up to phosphorus dose $1.5.10^{13}\text{cm}^{-2}$ and $V_{tlin}=-1.5\text{V}$. As the channel doping increases, the silicon depletion layer decreases and can be lower than the silicon film: the device

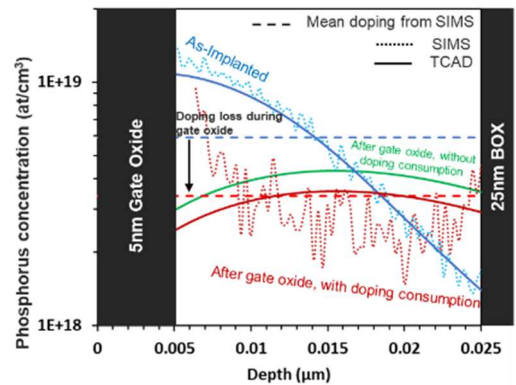


Fig. 6 : as-implanted and after gate oxide phosphorus profile in the Si film comparison between SIMS and TCAD

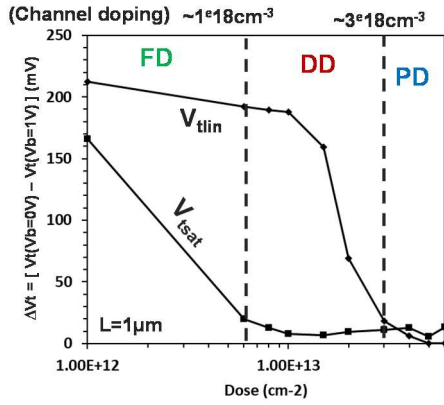


Fig. 9 : $L=1\mu\text{m}$ pMOS V_{tlin} and V_{tsat} variation from $V_{\text{B}}=0$ to $1V_{\text{b}}$ as a function of the channel implantation dose. Channel doping from TCAD are provided.

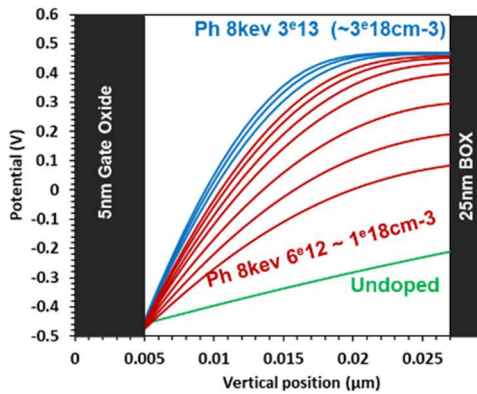


Fig. 10 : Potential variation in the Si film from the gate oxide to the BOX at $V_{\text{G}}=V_{\text{tlin}}$ and $V_{\text{D}}=-0.1V$ for several channel implantation dose.

operation can move from Fully Depleted (FD) to Partially Depleted (PD) operation. Because of the undepleted portion of the silicon film in PD operation, the ground plane bias (V_{B}) has no impact on V_{T} contrary to FD [2]. Fig.9 shows the measurement of the V_{tlin} dependency to V_{B} as a function of channel doping and demonstrates that PD operation starts around 3.10^{18}cm^{-3} channel doping. Same plot is performed with V_{tsat} (saturated regime V_{T} at $V_{\text{D}}=-2.5V$) shows that V_{B} impact is canceled for doping $>1.10^{18}\text{cm}^{-3}$. The channel doping range where V_{tlin} depends on the V_{B} and V_{tsat} doesn't depends on V_{B} defines the Dynamic Depleted (DD) operation where the device is FD in linear regime, and PD in saturated regime [10,11]. The potential variation at $V_{\text{G}}=V_{\text{T}}$ and $V_{\text{D}}=-0.1V$ in the Si film is shown on Fig.10 and highlights the difference between the 3 operating regimes: linear for FD, curved for DD and curved with a constant portion close to the BOX for PD. With channel doping increase, the depleted layer controlled by the gate decreases, so the floating area is thicker. We then focused on TCAD description of device with V_{T} lower than $-1.5V$ (FD and DD regimes).

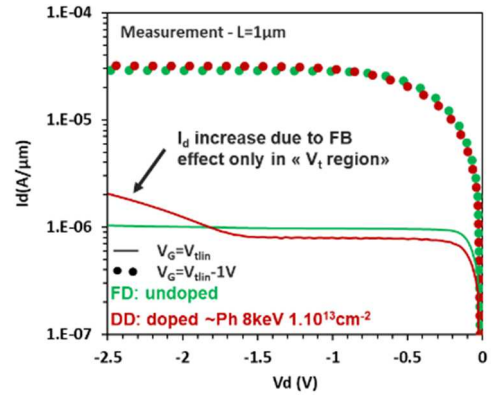


Fig. 11 : Measured $I_{\text{d}}-V_{\text{d}}$ for $L=1\mu\text{m}$ doped and undoped pMOS at $V_{\text{G}}=V_{\text{tlin}}$ & $V_{\text{G}}=V_{\text{tlin}}-1V$

V. FLOATING BODY EFFECTS TCAD DESCRIPTION

In DD operation, Floating Body effects (FB) occur. As shown by $I_{\text{d}}-V_{\text{d}}$ measurements (Fig.11), they produce a drain current increase at $|V_{\text{D}}|>1.5V$ only for V_{G} around V_{T} . This is due to the silicon floating area charged by Impact Ionization (II) at the drain [5]. For pMOS, it is charged with electrons: this negative charge reduces V_{tsat} and cancels the V_{B} impact on V_{tsat} : the long channel DIBL increases with channel doping because FB effects are worsened (Fig.12). To account for it in TCAD, II needs to be activated. DriftDiffusion simulations with default parameters leads to too high DIBL (blue on Fig.12). II is usually lower with hydrodynamic simulation [12] but DIBL is still too high. To reduce DIBL for long and doped channel, FB effect needs to be reduced. Two options are possible: reducing the II rate by a factor ($\text{II}_{\text{FACTOR}}$) or increase the recombination rate in the floating area with carrier lifetime reduction by a factor (τ_{FACTOR}). Note that it was demonstrated that carrier lifetime are shorter in thin film SOI than in bulk device ($\sim 10\text{ns}$ is 7nm Si film, [13]). Fig.13 shows the TCAD long channel DIBL variation for $\text{II}_{\text{FACTOR}}$ and τ_{FACTOR} variations: in the following, we use ($\text{II}_{\text{FACTOR}}=0.01$ and $\tau_{\text{FACTOR}}=0.2$ (same value as [14])). With this TCAD improvement, DIBL variation with channel doping is reproduced (Fig.12). To

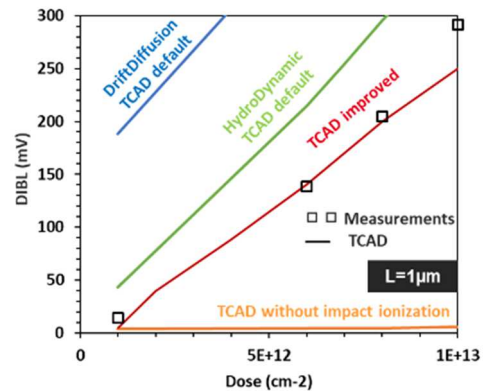


Fig. 12 : DIBL variation with the channel implantation dose from measurement and different TCAD settings.

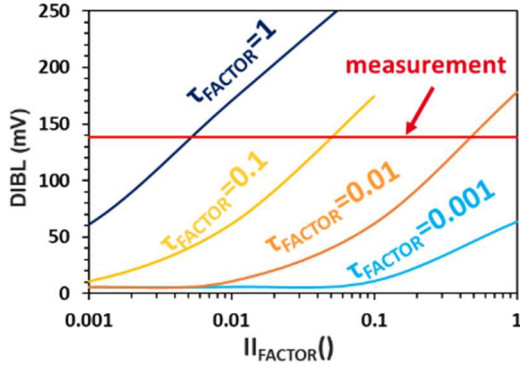


Fig. 13 : $L=1\mu\text{m}$ DIBL variation with II_{FACTOR} for several τ_{FACTOR} at constant channel doping (Phosphorus dose 6.10^{12}cm^{-2}) compare to measurement (red line)

observe FB effects, we need $|V_D| > 1.5\text{V}$ and channel doping needs to be $> 1.10^{18}\text{cm}^{-3}$ (Fig.14). It also shows floating area thickness increases with channel doping: the electrons stored increases, so the charge increases and the DIBL increases. Finally, Fig.15 shows the FB effects TCAD description improvement for various channel doping on I_d-V_d at $V_g=V_{\text{th}}$.

To highlight FB effects impact on the characteristic, drain current is normalized by its value at $V_d=-1\text{V}$, where there is

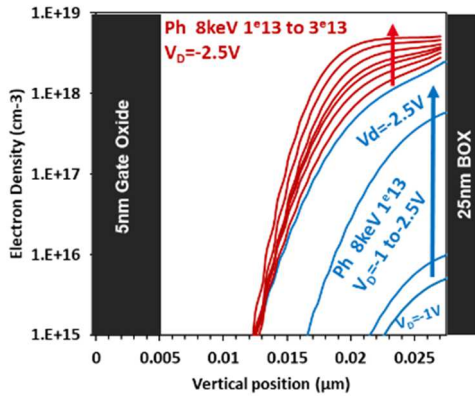


Fig. 14 : Electron density in the Si film at $V_g=V_{\text{th}}$ from tuned TCAD for V_D and channel doping variation.

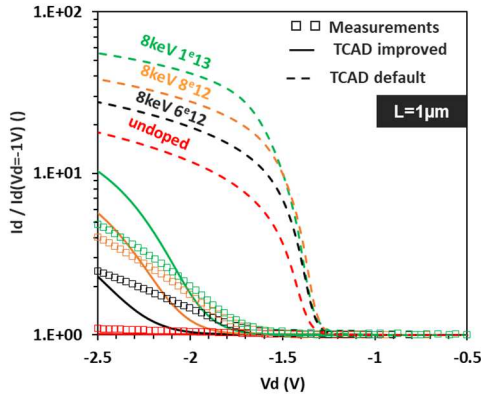


Fig. 15 : I_D-V_D normalized by $I_D(V_D=-1\text{V})$ at $V_G=V_T$ at $V_G=V_{\text{th}}$, from measurement, default hydrodynamic TCAD and tuned TCAD for channel doping variation.

no FB effect. Our description can still be improved, but the channel doping impact is well captured.

VI. CONCLUSION

In this paper, we propose a TCAD description of 22nm thick SOI device including the floating body effect variation with channel doping. We highlight that large parameter variation is required to match the experimental long channel DIBL, but the modeling still needs to be improved to reproduce experimental $I_D V_D$ characteristics.

REFERENCES

- [1] P. Chevalier et al., "PD-SOI CMOS and SiGe BiCMOS Technologies for 5G and 6G communications," 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2020, pp. 34.4.1-34.4.4, doi: 10.1109/IEDM13553.2020.9371954.
- [2] N. Planes et al., "28nm FDSOI technology platform for high-speed low-voltage digital applications," 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 2012, pp. 133-134, doi: 10.1109/VLSIT.2012.6242497.
- [3] O. Weber et al., "18nm FDSOI Enhanced Device Platform for ULP/ULL MCUs," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 27.2.1-27.2.4, doi: 10.1109/IEDM45625.2022.10019397.
- [4] R. Carter et al., "22nm FDSOI technology for emerging mobile, Internet-of-Things, and RF applications," 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2016, pp. 2.2.1-2.2.4, doi: 10.1109/IEDM.2016.7838029.
- [5] T. Ouisse et al. "Investigation of floating body effects in silicon-on-insulator metal-oxide-semiconductor field-effect transistors Journal of Applied Physics 70, 3912-3919 (1991) <https://doi.org/10.1063/1.349200>
- [6] S. K. H. Fung et al., "Controlling floating-body effects for 0.13 /spl mu/m and 0.10 /spl mu/m SOI CMOS," International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138), San Francisco, CA, USA, 2000, pp. 231-234, doi: 10.1109/IEDM.2000.904299.
- [7] S. Pemmaraju and S. A. Parke, "Elimination of body effects in SOI CMOS devices," 2004 IEEE Workshop on Microelectronics and Electron Devices, Boise, ID, USA, 2004, pp. 126-128, doi: 10.1109/WMED.2004.1297373.
- [8] J. Sleight and K. Mistry, "A compact Schottky body contact technology for SOI transistors," International Electron Devices Meeting. IEDM Technical Digest, Washington, DC, USA, 1997, pp. 419-422, doi: 10.1109/IEDM.1997.650414.
- [9] F. Guyader et al., "3-Tier BSI CIS with 3D Sequential & Hybrid Bonding Enabling a 1.4um pitch, 106dB HDR Flicker Free Pixel," 2022 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2022, pp. 37.4.1-37.4.4, doi: 10.1109/IEDM45625.2022.10019432.H.-K. Lim et al. TED 83
- [10] J. J. W. Sleight and K. R. Mistry, "DC and transient characterization of a compact Schottky body contact technology for SOI transistors," in IEEE Transactions on Electron Devices, vol. 46, no. 7, pp. 1451-1456, July 1999, doi: 10.1109/16.772490.
- [11] W. Wu et al. "Surface-potential-based compact modeling of dynamically depleted SOI MOSFETs," Solid-State Electronics, Volume 54, Issue 5, 2010 <https://doi.org/10.1016/j.sse.2009.12.040>.
- [12] D. Munteanu and G. Le Carval "Assessment of Anomalous Behavior in Hydrodynamic Simulation of CMOS Bulk and Partially Depleted SOI Devices" Journal of The Electrochemical Society, Volume 149, Number 10 <https://doi.org/10.1149/1.1506168>
- [13] K. H. Lee, M. Bawedin, H. -J. Park, M. Parihar and S. Cristoloveanu, "Carrier lifetime evaluation in FD-SOI layers," 2017 47th European Solid-State Device Research Conference (ESSDERC), Leuven, Belgium, 2017, pp. 140-143, doi: 10.1109/ESSDERC.2017.8066611.
- [14] D. Bosch et al. "SOI pMOS drain leakage understanding based on TCAD and measurements" to be published to SISPAD 2023