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Electrical characterization of SOI pMOS device leakage

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ABSTRACT

This work investigates Silicon-on-Insulator (SOI) pMOS leakage current. Temperature measurements indicates the superposition of two leakage mechanisms: band-to-band tunneling (BTBT) and Shockley-Read-Hall Field-Enhanced (SRHFE) generation recombination. Thanks to a dedicated low current measurement setup, the impact of device width (W), thickness (t_{si}) and polarization (back bias, drain and source) on leakage level is evaluated for both mechanisms.

1. Introduction

SOI technologies target ultra-low leakage applications such as analog and SRAM [1] or CMOS image sensor [2]. Usually, the gate induced drain leakage (GIDL) is attributed to band-to band tunneling (BTBT) in the gate-to-drain overlap region due to strong electric field [3,4]. However, under low electric field, leakage is rather described by Shockley-Read-Hall Field-Enhanced (SRHFE) generation and recombination model [5]. Depending on which mechanism is involved, leakage optimization techniques can be different (for instance lightly doped drain suppression in [1] for BTBT reduction). The aim of the presented study is firstly, to discriminate between these two leakage mechanisms thanks to temperature measurements, and secondly to evaluate the impact of transistor width, back gate bias voltage and silicon thickness on leakage.

2. Leakage current characterization

Fig. 1 shows a TEM cross section of the measured pMOS SOI devices targeting $V_{DD} = 2.5$ V applications. They feature a nominal silicon film thickness (t_{si}) of 23 nm, 25 nm buried oxide thickness (t_{BOX}), a 5.6 nm Equivalent Oxide Thickness (EOT) and a SiO_2 polysilicon gate. To reach several threshold voltages (V_T) value, channel doping is varied. A heavily doped poly N-type back plane enables static back biasing. As the film thickness is not so thin (23 nm), device operation is fully depleted for undoped devices and could be dynamic depleted (fully depleted in

linear regime and partially depleted in saturated regime), depending on channel doping level (see [6]). In this study, the silicon film doping is low enough to be fully depleted for both linear and saturated regime.

Electrical measurements have been performed with a dedicated setup using B1517A Agilent high-resolution source measurement unit and proper measurement integration time. Such a configuration allows low current measurements down to 10^{-15} A (Fig. 2(a), optimized setup), to be compared with the by default $1-2 \cdot 10^{-13}$ A resolution.

Nevertheless, leakage currents especially for low drain voltage (V_{DS}) or narrow devices can be even lower. To overcome this limitation, matrices of 100 devices in parallel are available to increase the current by two decades at the detriment of variability (Fig. 2(b)). However, this averaging effect is seen as an asset since a lower number of dies (lower measurement time) is required to ensure meaningful statistical data. In the presented case (low $V_{DS} = -0.05$ V), the optimized setup combined with matrix structure is required for full V_{GS} range measurement. If one of the condition is lacking, leakage below $V_{GS} = 2$ V cannot be captured.

3. Results and discussion

Thanks to the measurement accuracy improvement, we are able to sense all the leakage variation especially for low polarization. Next part will focus on how to discriminate between BTBT and SRHFE leakage mechanisms before analyzing leakage sensitivity to device parameters (channel doping, silicon film thickness, back bias and width).

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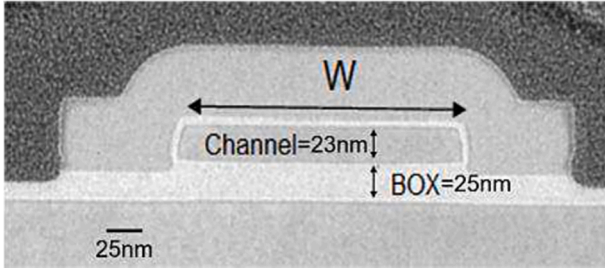


Fig. 1. TEM cross-section of a measured SOI device, cut along the W direction.

3.1. Discrimination between BTBT and SRHFE leakage mechanism predominance

3.1.1. Drain, source, gate polarization

Typical I_D - V_{GS} curves are depicted in Fig. 3(a) for various drain to source polarization V_{DS} . Fig. 3(b) presents I_D - V_{DS} curves but unlike conventional one, for $V_G > 0$ V (*i.e.* below V_T in leakage region). The idea here is to find a way to discriminate between BTBT and SRHFE leakage mechanism predominance. The drain current in GIDL region due to a tunneling mechanism, can be written as $I_D = A.F.exp^{\frac{B}{F}}$ with $F = \frac{V_{DG}-1.2}{3.T_{ox}}$ [3]. Instead of fitting the curve and being sensitive to fitting parameters, we prefer to search for a dedicated quantity that highlights this BTBT behavior. Starting from this equation, we can write:

$$\frac{dI_D}{dF} = \left(\frac{1}{F} + \frac{B}{F^2} \right) I_D$$

$$U = \frac{d}{dF} \left(\frac{dI_D}{dF} \cdot \frac{1}{I_D} \cdot F^2 \right) = \text{CONSTANT}$$

Note that A and B depends on $E_G(T)$.

Thus, if the starting behavior is of the form of GIDL current one, the mathematical transformation U leads to a constant value. When this transformation is applied to experimental I_D - V_{DS} curves (Fig. 3(c)), this constant behavior is found back for V_{DS} higher than a threshold V_{DS} value, suggesting a BTBT behavior-like. Note that this threshold value is higher for lower V_{GS} that is coherent with a field dependency effect. However, this method only states that the behavior is of the form of BTBT but does not exclude another mechanism.

3.1.2. Temperature measurements

To go further, temperature measurements have been performed. As highlighted in Fig. 4(a), I_D - V_{DS} curves are highly sensitive to temperature, especially for low V_{DS} values. For instance at $V_{DS} = -0.5$ V the drain current varies by 0.03 dec/ $^{\circ}$ C whereas for $V_{DS} = -3$ V the variation is much smaller and equals to 0.009 dec/ $^{\circ}$ C. Activation energy (E_A) [7] has been extracted for various V_{DS} and V_{GS} values (Fig. 4(b)). The lateral translation between undoped and doped devices (dash versus plain

lines) for a fixed V_G is attributed to the V_T difference. Low E_A ($E_A < 0.1$ eV = $E_{A-crit-ref}$) indicates a temperature insensitive leakage mechanism such as BTBT [8]. On the contrary, higher E_A (> 0.1 eV) indicates a junction thermal leakage current (SRHFE). In fact for low field value (low V_{DS} and/or low V_{GS}), SRHFE is predominant whereas for larger field values BTBT override leakage as expected. Note that the $E_{A-crit-ref} = 0.1$ eV to discriminate between SRHFE and BTBT is higher than the one extracted on I_D - V_{DS} curve: $E_{A-crit-U} = 0.07$ eV.

3.2. Leakage sensitivity to device variation (channel doping, silicon film thickness, back bias and width)

This part will explore the leakage behavior in BTBT or SRHFE predominance regime for various device variations.

3.2.1. Doped versus undoped channel

No major difference is seen on leakage current between undoped and doped device at same gate overdrive (see Fig. 5(a)) in SRHFE predominance region. However, for large (V_{GS} , V_{DS}) couple, doped devices are less leaky which is in contradiction with the BTBT behavior seen for overlapped drain junction for FinFETs devices [9]. TCAD simulation are required to understand further. If we assume that it corresponds to a SRHFE to BTBT transition, the extracted $E_{A-crit-dop}$ is 0.06 eV.

3.2.2. Silicon film thickness

Fig. 5(b) presents I_D - V_{GS} for $V_{DS} = -1$ V (*i.e.* SRHFE predominance region) and $V_{DS} = -2.5$ V (*i.e.* SRHFE or BTBT region depending on V_{GS} value) for silicon thickness ranging from 23 nm down to 16 nm. The inset shows that the leakage slightly increases for lower silicon thickness when the predominant leakage mechanism is SRHFE. However for $V_{DS} = -2.5$ V, this silicon thickness dependency vanishes for $V_{GS} > 1.8$ V which could be coherent with a BTBT process. This hypothesis must be validated though TCAD simulation. Here, $E_{A-tsi} = 0.06$ eV.

3.2.3. Back-bias sensitivity

As presented in Fig. 6(a), back polarization V_B has no impact for $V_{GS} > 2.5$ V (BTBT predominance regime) and a slight influence on leakage current otherwise (SRHFE predominance regime). In fact (see Fig. 6(b)) minimum leakage current is much more sensitive to drain and source polarization than back bias one for $V_{BS} \in [-1V; +3V]$. The sudden leakage increase seen for large negative V_{BS} is attributed to the formation of a back channel near BOX interface.

3.2.4. Device width

Mesa isolated transistors can be seen as a top transistor in parallel with an edge transistor [10]. It results in unusual characteristics especially for doped channel devices. In fact, the subthreshold regime is driven only by transistor edges for all device width. To evaluate the

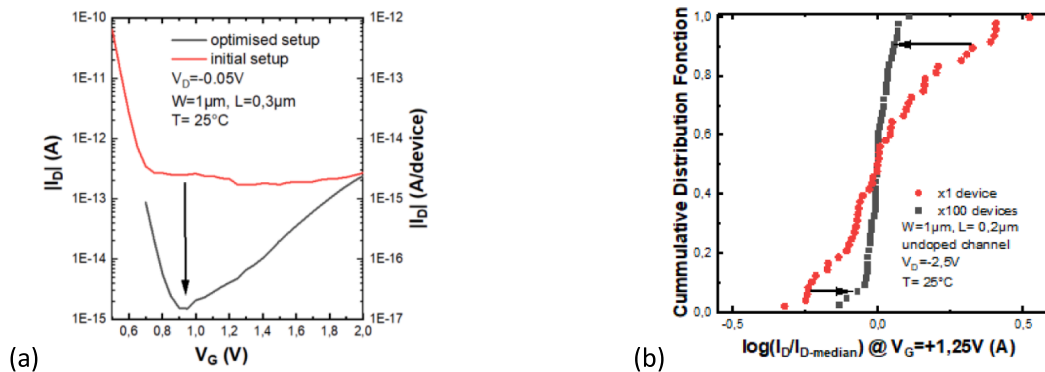


Fig. 2. (a) I_D - V_G at $V_{DS} = -0.05$ V for both optimised and initial setup. (b) Cumulative Distribution of drain current for $V_{GS} = +1.25$ V. x100 devices structures tighten the distribution.

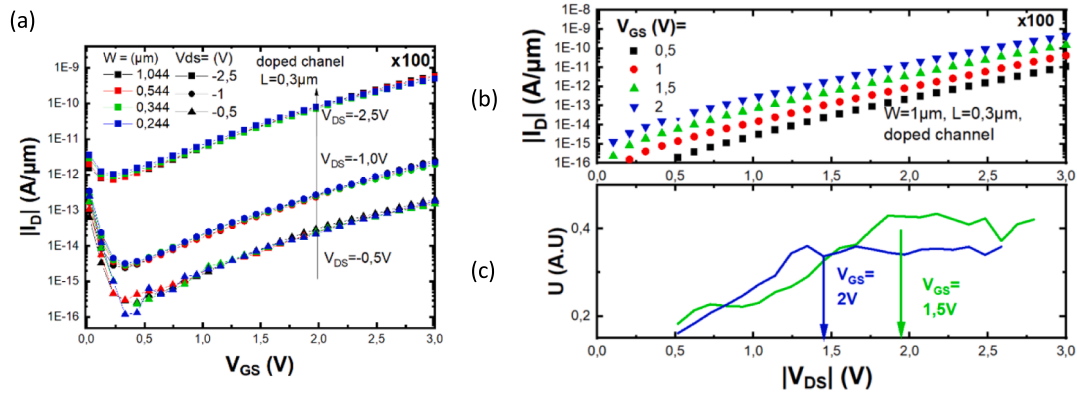


Fig. 3. (a): I_D - V_{GS} for various V_{DS} and width device. $L = 0.3 \mu\text{m}$, doped channel. (b): I_D - V_{DS} for various V_G . (c): U as a function of V_{DS} .

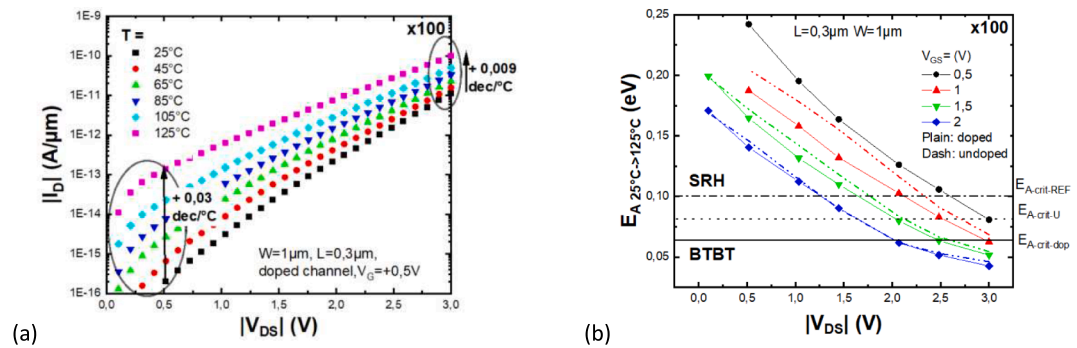


Fig. 4. (a): I_D - V_{DS} at $V_G = +0.5 \text{ V}$ for $W = 1 \mu\text{m}$ and $L = 0.3 \mu\text{m}$ and die temperature from 25°C to 125°C . (b): Activation energy (E_A) between 25°C and 125°C as a function of V_{DS} for various V_G and both doped and undoped devices.

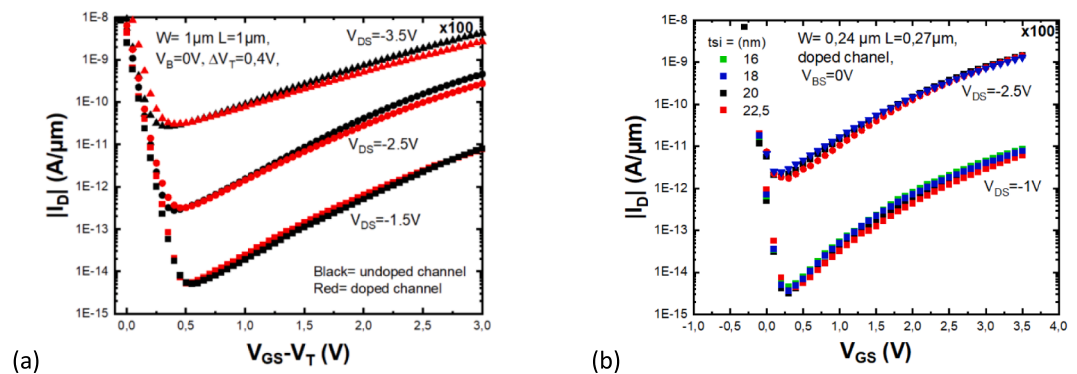


Fig. 5. (a): I_D - $(V_{GS}-V_T)$ for $V_{DS} = -0.5 \text{ V}$ for undoped vs. doped device. (b): I_D - V_{GS} for silicon film thickness from 18.5 nm up to 20.5 nm . Drain leakage depends on silicon film thickness for low (V_{DS} , V_{GS}) value.

impact of width on leakage, I_D - V_{GS} curves for various V_{DS} values and device width from $0.244 \mu\text{m}$ to $1.044 \mu\text{m}$ are plotted in Fig. 3(a). No major difference in normalized leakage is seen between all the width dimensions. It indicates that mesa isolation does not lead to an additional leakage component.

3.3. Activation energy (E_A) criterion discussion

As a summary, Fig. 7 presents the different zones where SRHFE or BTBT are predominant as a function of V_D and V_G . Various criteria are indicated. In literature, usually $E_{A-crit} = 0.1 \text{ eV}$ is used to determine whether SRHFE or BTBT leakage mechanism predominates for bulk devices. However, we experimentally find a predominance of BTBT

leakage mechanism for $E_A < 0.07 \text{ eV}$ (U transformation of I_D - V_D curves). In addition to, we observe that for $E_A < 0.06 \text{ eV}$ the leakage is no longer dependent on film thickness and stats depending on channel doping. This specific behavior could be linked to a SRHFE to BTBT transition but additional TCAD is required to validate this statement. In overall, it suggests that this $E_{A-crit} = 0.1 \text{ eV}$ criterion must be lower down for SOI devices.

4. Conclusion

Leakage currents down to a few fA have been measured. Temperature measurements indicate the (V_{DS} ; V_{GS}) regions where either BTBT or SRHFE leakage mechanism predominate, using an activation energy

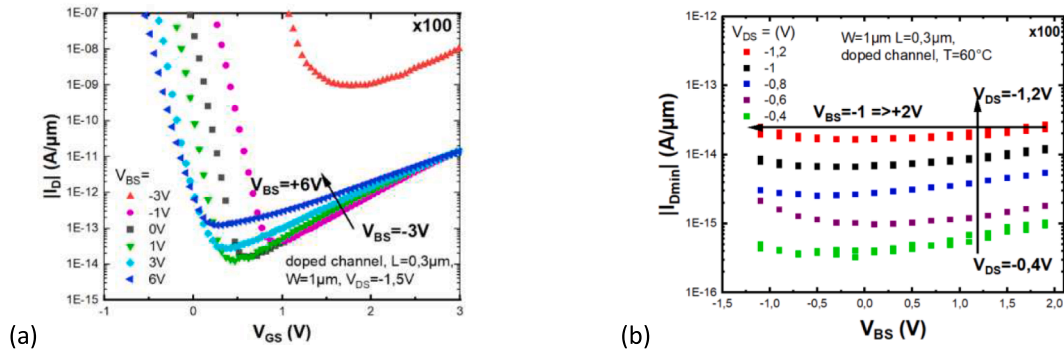


Fig. 6. (a): I_D - V_{GS} for V_{BS} ranging from $-3V$ to $+6V$ at $V_{DS} = -1.5V$, $W = 1\mu m$, $L = 0.3\mu m$ doped channel. (b): Minimum I_D current as a function of V_{BS} for various V_{DS} . Note that a same curve color is obtained for several (V_D ; V_S) couples.

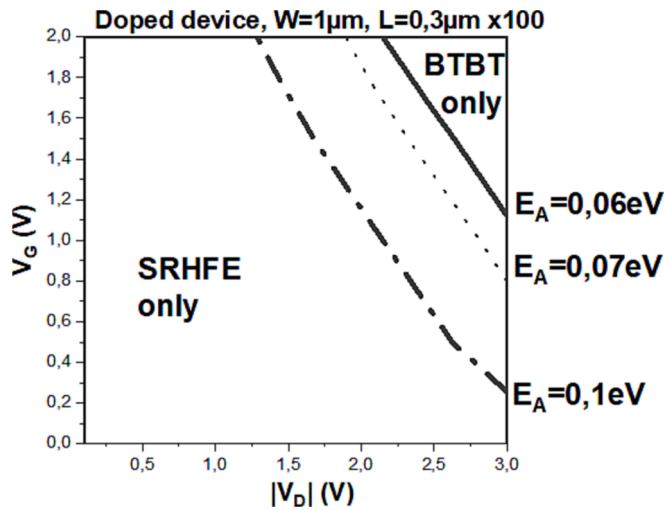


Fig. 7. Activation energy from 25 to 125 °C as a function of V_G and V_D with the various E_A criteria.

criteria. The activation energy criteria have been lowered down compared to literature to match experimental observations. We thus noticed that SRHFE leakage is slightly dependent on silicon thickness and V_{BS} whereas BTBT leakage is dependent on channel doping. It is worth noticing that the aforementioned degradation is negligible compare with $V_{DS}/V_{GS}/T$ operating point.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence

the work reported in this paper.

Data availability

The authors do not have permission to share data.

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