6.6W/mm 200mm CMOS compatible AlN/GaN/Si MIS-HEMT with in-situ SiN gate dielectric and low temperature ohmic contacts

Erwan Morvan, Yveline Gobil, Fanny Morisot, Jérôme Biscarrat, Matthew Charles, Jose Lugo, Alexis Divay, Mohammed Medbouhi, Ismael Charlet, Julien Delprato, et al.

6.6W/mm 200mm CMOS compatible AlN/GaN/Si MIS-HEMT with in-situ SiN gate dielectric and low temperature ohmic contacts

E.Morvan,Y.Gobil, F.Morisot, J.Biscarat, M.Charles, J. Lugo, A.Divay, M.Medbouhi, I.Charlet, J.Delprato, P.Scheiblin, B.Rrustemi, A.Giry, A.Serhan, S.Ruel, P.Pimenta-Barros, F.Laulagnet, S.Minoret, A.Anotta, T.Billon, B.Duriez
CEA Leti, Université Grenoble Alpes, 38000 Grenoble, France , email: erwan.morvan@cea.fr

***Abstract*—**We report on the development of CMOS compatible SiN/AlN/GaN MIS-HEMT process on 200mm Si substrates for Ka-band power amplification. The combination of soft gate process, gate design with reduced electric field, in-situ SiN gate dielectric, low temperature ohmic contacts, low substrate RF losses and GaN:C back-barrier leads to Ft/F_{MAX} of 81/173GHz for 2x50µm devices with L_G=150nm. At 28 GHz, the device shows performance similar to other GaN/Si technologies at V_{DD}=10V and competitive performance with GaN/SiC at V_{DD}=20V with PAE=41% and P_{SAT}= 6.6W/mm.

I. INTRODUCTION

GaN-based high electron mobility transistors (HEMT) have shown superior performance for RF applications such as mobile communication, radar, satcom, earth observation or industrial heating, due to its high breakdown field and high carrier density (Ns) and electron saturation velocity of its two dimensional electron gas (2DEG) [1]. One of the emerging mm-wave III-N HEMT technology is using ultra-thin, ultra-wide bandgap (UWBG) barrier layer, like AlN or ScAlN, to simultaneously support operation at high current, high voltage and high frequency [2],[6],[12],[14]. In order to avoid excessive gate leakage associated with ultra-thin barriers, MIS-HEMT structures have been proposed. Recently, very high performance MIS-HEMT has been demonstrated, using CMOS compatible, deeply scaled ex-situ high-k gate insulator [4],[9]. An alternative approach is to use in-situ MOCVD SiN for the gate dielectric. In-situ SiN/AlN/GaN HEMT stack has the combined advantage of high Ns with a very thin barrier layer due to the high spontaneous and piezoelectric polarization of AlN on GaN with high quality in-situ SiN layer. This structure shows very good performance up to mm-wave. However the majority of published studies are based on GaN/SiC and/or non CMOS compatible processing [5],[6],[7],[14].

In this work, we demonstrate state of the art 200mm CMOS compatible SiN/AlN/GaN/Si MIS-HEMT with in-situ SiN gate dielectric, a low damage gate process and low temperature ohmic contacts to preserve heterojunction performance. These devices are designed with a reference gate length, L_G=150nm for power amplification in Ka-band.

II. DEVICE TECHNOLOGY

A. *Epitaxy structure and Device Processing*

The starting material is 200mm MOCVD GaN epitaxy on Si-HR <111> substrate with resistivity > 3 kΩ.cm from ENKRIS Semiconductor. It consists of nucleation and stress management layers, a carbon doped GaN buffer (GaN:C), a 150nm un-intentionally doped GaN channel (appropriate for L_G =150nm), a 5nm AlN barrier and an in-situ 2.5 nm SiN capping layer (Fig.1). The fully CMOS compatible, gold free process flow is summarized in Fig.2. Ar was implanted for device isolation. Fully recessed Ti/Al ohmic contacts annealed at 590°C show a contact resistance, Rc of 0.4 Ω.mm, extracted from TLM measurement and a metal sheet resistance of 0.24Ω/sq. This low temperature contact avoids 2DEG properties degradation observed for high temperature contact (>800°C) even with in-situ SiN capping layer [5]. At metal 1 level, the 2DEG sheet resistance, R_S is 220 Ω/sq (Van der Pauw) close to the post-epitaxy value of 200 Ω/sq (Eddy current). The gate finger has a static resistance of 0.106 Ω per micron gate width for L_G=150nm. The sheet resistance of the 1.4 µm Ti/TiN/AlCu/Ti/TiN metal 1 interconnects is 21 mΩ/sq. RF losses of 0.13 +/- 0.01 dB/mm are extracted at 30 GHz from Coplanar Waveguide (CPW) S-parameters measurements at the end of the HEMT process (Fig.3). The final coplanar two finger device is shown in Fig.4. The uniformity of typical device parameters is shown in Fig.5.

Device TEM cross-section is shown in Fig.6. The dielectric stack used for the gate foot fabrication allows very soft gate processing with minimal impact on the in-situ SiN gate dielectric and heterojunction underneath. Before ALCVD TiN deposition, the bottom oxide layer is wet etched, which additionally produces rounded gate edge to minimize electric field peak at the gate corner. TCAD simulations, carried out with Sentaurus Device from Synopsys (Fig.7 and Fig.8), show the reduction of the electric field peak at gate edge due to the wet etch undercut (UC). Low field channel transport properties were measured with a gated Hall bar test structure (Fig.9). High channel sheet carrier density, N_S, and mobility, µ, associated with a low channel sheet resistance, R_S are obtained, indicating low gate process impact on the 2DEG.

B. *Transistor measurement*

The reference HEMT has a 150nm gate length, 2x50µm width, L_{GS} = 0.4µm and L_{GD} = 1.1µm. Its DC characteristics are

shown in Fig.10. At Vds=10V, a typical HEMT shows a high maximum drain current, I_{DMAX} of 1.8 A/mm at Vgs=+2V, a pinch-off voltage, Vp of -2.6V (at Vds=10V, Id=100µA/mm), and a Gm_{MAX} of 610 mS/mm. In off-state at Vgs=-7.1V Id reached 3mA/mm at V_{DS}=24V. This is not a gate-drain breakdown but a D-S leakage (Fig.10.d). The onset of this leakage is strongly dependent on L_G (Fig.11) due to a short channel effect (SCE) [8] as shown in Fig.12 and Fig.13. The on-state resistance, R_{ON} = 1.3 Ohm.mm for L_G=150nm (Fig.11) is mainly driven by Rc (~60%) which leaves room for improvement of this device. We have reached Rc = 0.22 +/- 0.014 Ω.mm with recess optimization, which would translate to R_{ON} = 0.94 Ω.mm. [3] even reached 0.15 Ω.mm with a similar contact technology. The device behaves well at 150°C with I_{DMAX} =1.5A/mm (Fig.14). The temperature impact on the knee voltage is low due to the weak temperature sensitivity of Rc.

Pulsed I-V measurements were carried out on the reference HEMT with a PIV AM3200 from AMCAD Engineering. A pulse width and delay of 1µs and a duty cycle of 0.1% were used. The reference bias was Vgsq/Vdsq=0/0V and the stress biases were Vgs_{OFF}/0V, /10V, /15V, /20V with Vgs_{OFF}= -5.1 V. A typical pulsed-IV characteristic is shown in Fig.15. Gate lag (GL) and Drain lag (DL) are extracted from maximum power load-lines (including both knee voltage and drain current degradations due to trapping). Four dies have been measured across the wafer radius. As can be observed in Table 1, the GL is very small and the mean DL is below 10% at Vdsq/Vgsq=20V/-5.1V (with similar values on 4 dies), indicating a low trapping effect and good uniformity.

S-parameters were measured using 100µm pitch GSG probes and a N5227B PNA from Keysight on a semi-automatic prober from MPI. The frequency range is 100MHz to 67GHz with an IF of 100Hz. Voltage biasing was done through the intern bias-T from the VNA and DC polarizations was applied using B1500 SMU. After de-embedding, the reference HEMT yields Ft = 81GHz and F_{MAX}=173GHz (Fig.16). L_G and W_G impact on Ft and F_{MAX} are described in Fig.17 and Fig.18, respectively. Ft does not increase for L_G=80nm because the channel is too thick (150nm) and because of a parasitic capacitance due to unwanted proximity between the gate head and the source contact after oxide polishing (see Fig.6). F_{MAX} higher than 200 GHz is reached for 2x35µm devices thanks to smaller R_G.

The continuous wave (CW) large signal performance of the transistors was measured using an on-wafer vectorial multi-harmonic Load-Pull (LP) setup. The fundamental frequency was set to 28GHz, with second harmonic tuning on both source and load. The source and load impedances were set for optimum PAE (Power Added Efficiency). The tuners were connected directly to the probes for improved impedance coverage (DELTA tuners from Focus Microwaves). The reference HEMT was measured at different bias points, with PAE_{MAX}= 47.2% and P_{SAT}=2.93W/mm at V_{DD}=10V (Fig.19). At V_{DD}=20V, the device shows a PAE_{MAX}=41.1% and P_{SAT}=6.58W/mm. A HEMT with W_G=2x35µm is more efficient with PAE_{MAX}=51.5% at V_{DD}=8V and 49.5% at V_{DD}=10V (Fig.20). Table 2 summarizes LP results on various device geometries. An estimation of the reference device temperature rise is obtained from measured DC power as a function of P_{IN} and a transistor thermal resistance, R_{TH} of 116 K/W, extracted by IR thermal imaging on the same transistor fabricated on a very similar epi stack [10]. The high thermal conductivity of the GaN:C back-barrier (compared to AlGaN based), close to the heat source, allows the device temperature to remain below 135°C (30°C chuck) at a P_{OUT} of 6.6 W/mm (Fig.21).

High power density has been reached in this work thanks to 1) high drain current available with AlN barrier 2) low substrate RF losses 3) low lag 4) delayed forward gate injection due to SiN gate insulator allowing large gate swing (Fig.10a) and 5) reasonable R_{TH} with GaN:C back-barrier. A benchmark of PAE versus $P_{OUT\ MAX}$ is shown in Fig.22. This power performance is close to the best GaN/Si results at V_{DS}=10V and shows that this technology can approach GaN/SiC power density performance around 30 GHz for PA applications at higher voltages. Fig.23 compares the F_{MAX} versus Ft of the reference device in this work with other GaN transistors with same or lower L_G. This work shows state of the art Ft and F_{MAX} for L_G=150nm when compared to GaN/SiC devices with comparable L_G and competitive performance when compared to other GaN/Si devices with lower L_G.

III. Conclusion

CMOS compatible 200mm SiN/AlN/GaN MIS-HEMT on Silicon demonstration is reported. Low damage gate process and low temperature ohmic contacts integrated on high Ns/µ AlN based heterostructure with in-situ SiN gate dielectric leads to high current (1.8A/mm), high Gm_{MAX} (>600mS/mm) and high CW P_{OUT} (>6.5W/mm) at 28 GHz. This work brings GaN/Si HEMT closer to GaN/SiC performance at 28 GHz in terms of power density and highlights SiN/AlN/GaN on silicon MIS-HEMT as a potential candidate for high power Ka-band PAs. It is foreseen from those results that device performance can be further improved by reduction of R_C and optimization of channel thickness to reduce SCE for short gate lengths.

Acknowledgment

The authors would like to thank ST Microelectronics-Crolles and III-V Lab teams for fruitful discussions and financial support, Focus Microwave for LP measurements and IEMN for their contribution to IR thermography measurements. This work was supported by IPCEI European Project.

References

[1] K. Shinohara et al, IEEE TED, vol.60, no.10, p.2982, 2013; [2] T.E. Kazior et al, IMS, Tu4E-1, 2022; [3] B. Parvais et al IEDM p.155, 2020; [4] H.W. Then et al, IEEE microwave and wireless technology letters, p.1, may 2023; [5] H. Du et al., IEEE EDL, p. 1, 2023; [6] E. Kacou, EDICON 2019; [7] K. Arrouche, IMS 2020, Tu3H-2,p.285; [8] R. Elkashlan et al, IMS, Th2E-2, 2022; [9] H.W. Then et al, IEDM 2021 p.231; [10] A. Chanuel PhD thesis p.131; [11] R. Elkashlan et al, IMS, Tu1B-5, 2023 ; [12] E.M. Chumbes et al, IMS, Tu4E-3, 2022 ; [13] M. Mi et al., TED vol.64,n.12,p.4875, 2017 ; [14] K. Arrouche et al, Journal of the EDS, vol.7,p.1145,2019; [15] S. Piotrowicz et al, Eumic 2016,p.69; [16] Y. Cui et al, IMS,We1G-3, 2020; [17] D.F. Brown et al, IMS, Tu2B-4, 2023; [18] R.S. Howell et al, IMS 2023; [19] H.Xie et al, IEEE microwave and wireless components letters, vol. 31,no.2,feb 2021.

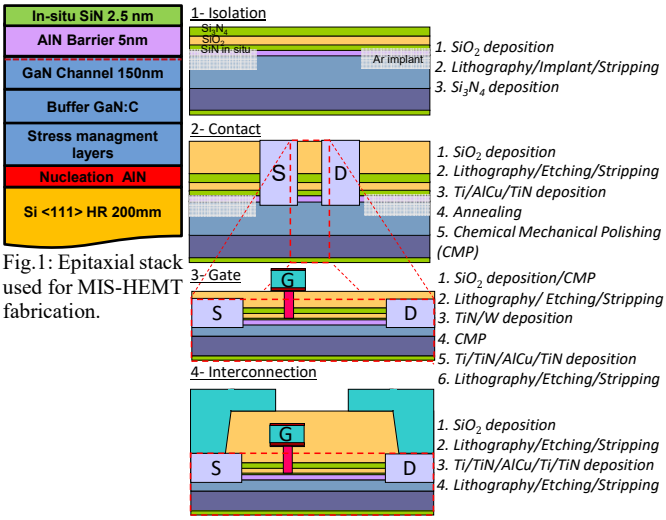

Fig.1: Epitaxial stack used for MIS-HEMT fabrication.

Fig.2: Process flow of the coplanar 2 finger devices.

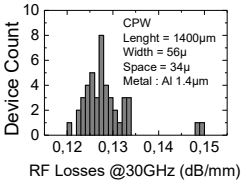

Fig.3: normalized RF losses distribution at 30 GHz.

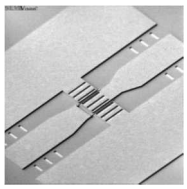

Fig.4: SEM top view of the coplanar 2x50µm transistor at Metal 1 level with GSG in/out.

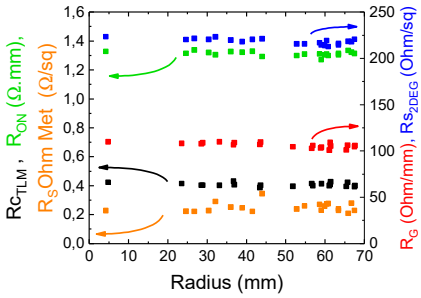

Fig.5: Uniformity of Rc, R_{ON}, Rs_{2DEG} and R_G as a function of radial position on the wafer.

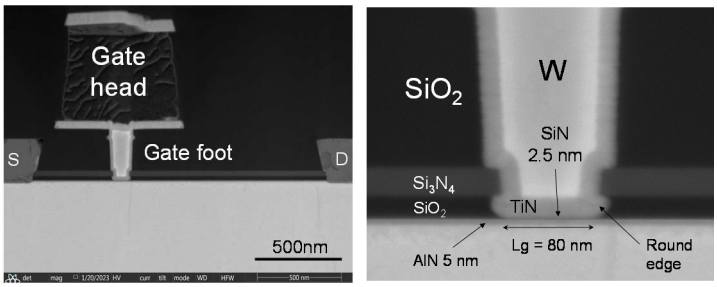

Fig.6: **Left**: STEM cross-section of the transistor showing asymmetry of L_{GS} and L_{GD} and large gate head section to achieve low R_G. Very good S/D edge definition is obtained with contact recessing, low temperature annealing and planarization. **Right**: STEM cross-section of a 80nm gate foot showing the conformal gate metal (TiN), the 2.5nm in-situ SiN gate dielectric, the 5nm AlN barrier and the rounded gate edge.

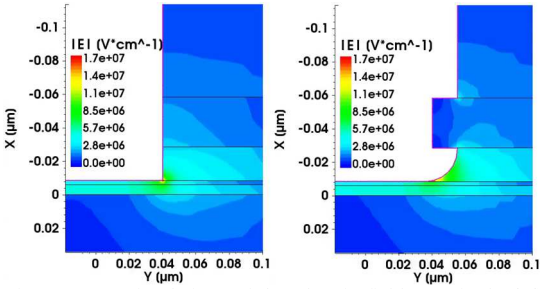

Fig.7: TCAD simulations of the Electric field magnitude (|E|) at the drain side of the gate foot on the reference transistor at V_{GS}/V_{DS} = -5V/10V, w/o UC (left) and with UC (right) in the oxide layer.

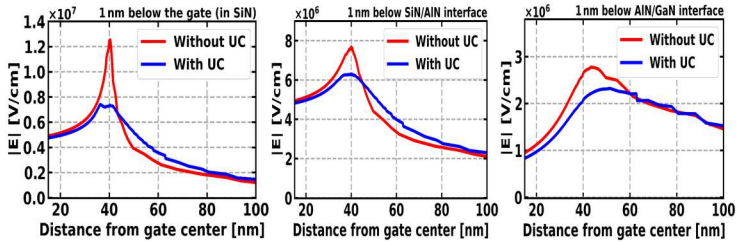

Fig.8: Simulated 1D Electric field magnitude (|E|) profiles for V_{DS}=10V/V_{GS}=-5V at constant depth below the gate showing 42%/18%/18% reduction of |E| in in-situ SiN, AlN barrier and GaN channel layers respectively, due to undercut.

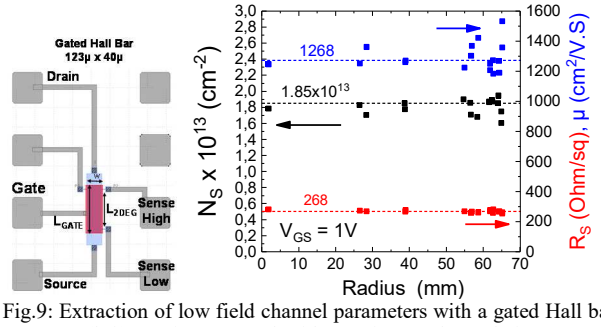

Fig.9: Extraction of low field channel parameters with a gated Hall bar structure (left). R_S is measured with 4 points probe technique. N_S, is obtained by integration of C(V_{GS}) and µ = 1/(N_S.q.R_S) where q is the electronic charge. Uniformity across the wafer is shown on the right graph for V_{GS}= +1V with median values of R_S, N_S and µ.

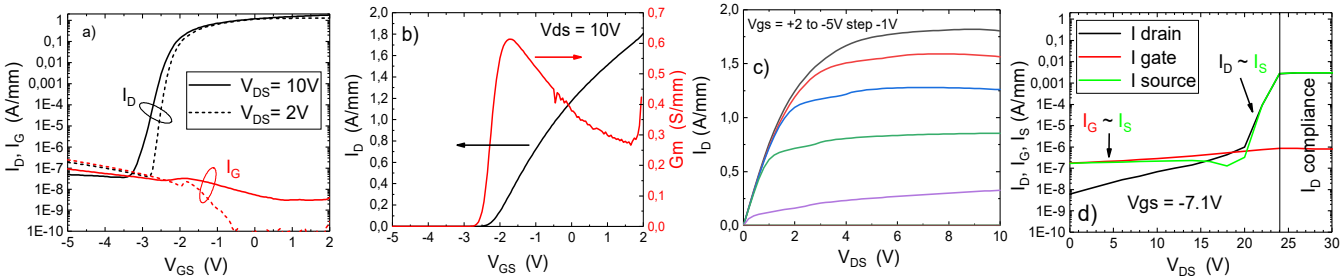

Fig.10: typical DC characteristics of 2x50µm HEMT (L_G = 150nm). **a)**: I_D and I_G (V_{GS}) at V_{DS}=10V and 2V showing good pinch-off behavior, no forward gate injection at V_{GS}=+2V and low gate leakage current thanks to in-situ SiN gate dielectric (3 orders of magnitudes lower than the corresponding Schottky gate leakage, not shown). **b)** I_D and G_m(V_{GS}) at V_{DS}=10V showing a maximum drain current of 1.8 A/mm at V_{GS}=+2V and a peak g_m of 610 mS/mm. **c)** I_D(V_{DS},V_{GS}) **d)** I_D, I_G and I_S(V_{DS}) in off-state showing a low V_{DS} regime with low drain current and a source current driven by G-S leakage (I_S~I_G) and a high V_{DS} regime above 20V where the drain current is driven by a D-S leakage with negligible gate current. The non-destructive drain current compliance (3mA/mm) is reached at V_{DS}=24V. The two terminal G-D diode breakdown voltage with L_G=150nm is 35 +/-2.5V (not shown).

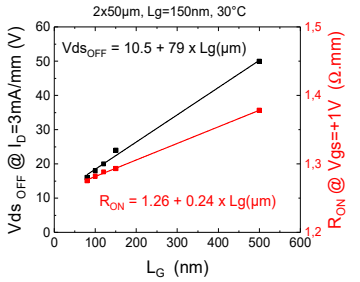

Fig.11: $V_{DS\ OFF}(L_G)$ at V_{GS}=-7.1V and I_D=3mA/mm (black) . Degradation of $V_{DS\ OFF}$ with Lg is due to a short channel effect. $R_{ON}(L_G)$ (red) is dominated by access resistance, mainly R_C (~60%).

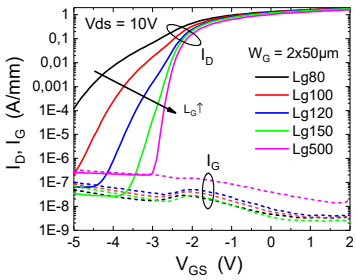

Fig.12: Impact of L_G on $I_D(V_{GS})$ (bold) and $I_G(V_{GS})$ (dot). Short L_G suffer from insufficient 2DEG confinement due to non-optimum channel thickness (150nm), which leads to V_P shift.

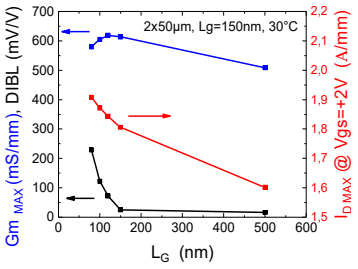

Fig.13: Impact of L_G on Gm_{MAX}, $I_{D\ MAX}$ and DIBL. Although $I_{D\ MAX}$ increases for shorter L_G, V_P shift degrades G_M. DIBL is 25mV/V for L_G=150nm but degrades strongly for smaller L_G.

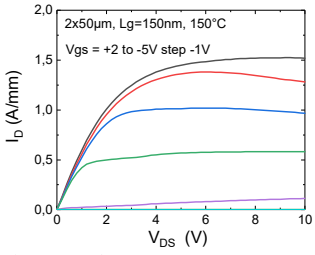

Fig.14: Reference HEMT $I_D(V_{DS})$ at 150°C. I_{DMAX} reduction is mainly due to a decrease of the saturation velocity with temperature.

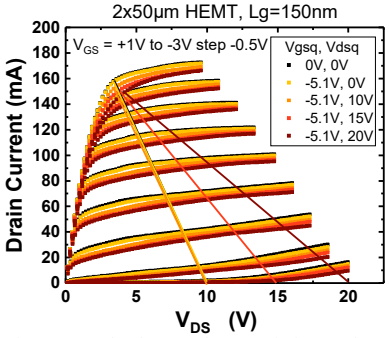

Fig.15: Pulsed-IV characteristics of a 2x50µm HEMT with Lg=150nm. Each point of the $I_D(V_{DS},V_{GS})$ curves is pulsed from a given stress bias point (Vgsq,Vdsq). GL is negligible (light orange vs black curves) and DL is low up to 20V (dark red vs black curves). Straight lines are optimum load-lines for output power.

Die	GL (%)	DL10 (%)	DL15 (%)	DL20 (%)	$I_D$max (A/mm)
0	0.4	4.0	7.9	10.2	1.69
1	0.4	3.6	6.9	9.6	1.73
2	0.5	3.3	6.6	10.5	1.84
3	1.4	1.8	4.8	8.0	1.81
Mean	0.67	3.17	6.55	9.57	1.76

Table 1: Pulsed-IV results on 4 dies across a wafer radius. Gate Lag (GL) is extracted form V_{GS}/V_{DS}= $V_{GS\text{-}OFF}$/0V and Drain Lags (DL10,15 and 20) are extracted from V_{GS}/V_{DS}=$V_{GS\text{-}OFF}$/10, 15 and 20V, respectively.

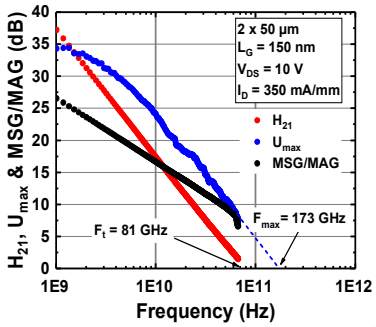

Fig.16: 2x50µm HEMT H21, Umax and MSG/MAG versus frequency. Extrapolation gives Ft/ F_{MAX} = 81/173 GHz.

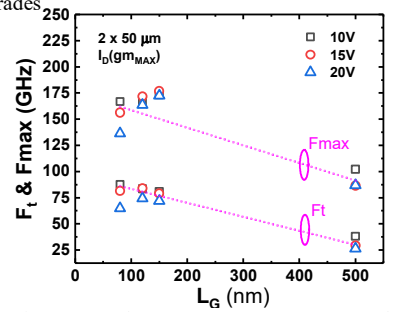

Fig.17: Ft and F_{MAX} vs L_G at V_{DS}= 10, 15 and 20V and I_D at Gm_{MAX}.

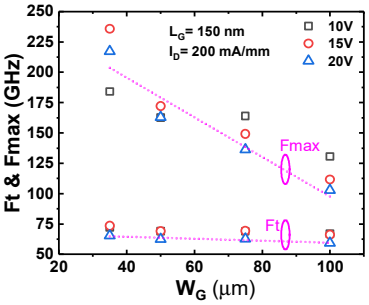

Fig.18: Ft and F_{MAX} vs gate Width (W_G) at V_{DS} = 10, 15 and 20V and I_D=200mA/mm. The reduction of R_G for smaller W_G leads to an increase of F_{MAX} above 200 GHz.

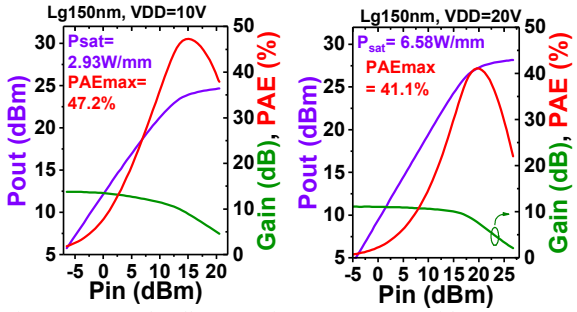

Fig.19: CW Load-pull sweep of 2x50µm HEMT with L_G=150nm at 28 GHz. We obtain state of the art $P_{OUT,MAX}$ of 2.9 W/mm at V_{DD}=10V and record 6.6W/mm at V_{DD}=20V for a CMOS compatible 200mm SiN/AlN/GaN/Si MIS-HEMT.

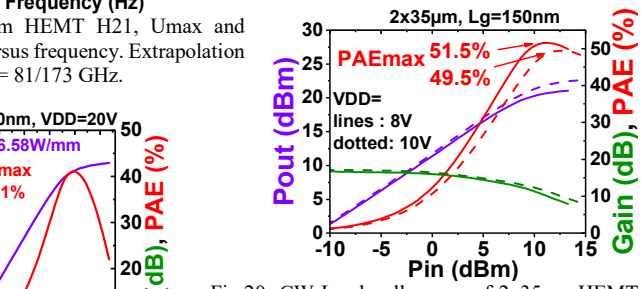

Fig.20: CW Load-pull sweep of 2x35µm HEMT with Lg=150nm at 28 GHz. The device reached 51% PAE at V_{DD}=8V and 17dB linear power gain.

L_G (nm)	Wg (µ)	V_{DS} (V)	PAE_{MAX} (%)	P_{OUT} @PAE_{MAX} (W/mm)	P_{SAT} (W/mm)
150	2x50	10	47.2	2.17	2.93
		15	45.33	3.25	3.61
		20	41.1	4.94	**6.58**
150	2x35	8	**51.5**	1.68	1.83
		10	49.5	2.39	2.62
80	2x50	8	46.6	1.98	-
		10	41	2.52	3

Table 2: PAE, P_{OUT} at max PAE and P_{SAT} for different device geometries and bias voltages.

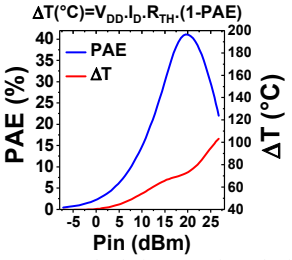

Fig.21: Calculation of device temperature rise as a function of P_{IN} and PAE with R_{TH}=116 K/W.

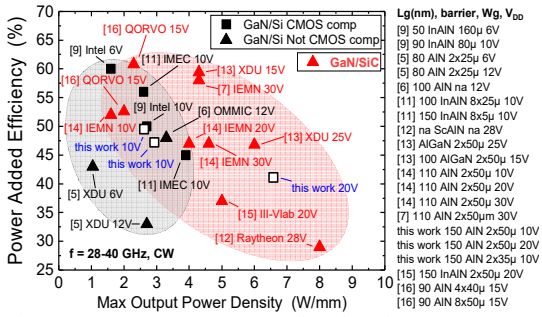

Fig.22: CW PAE vs max P_{OUT} benchmark at 28-40 GHz. GaN/Si (black) and GaN/SiC (red). CMOS compatible (square) and non-compatible (triangles). This work (blue) shows state of the art at 10V and high power density at 20V, similar to GaN/SiC.

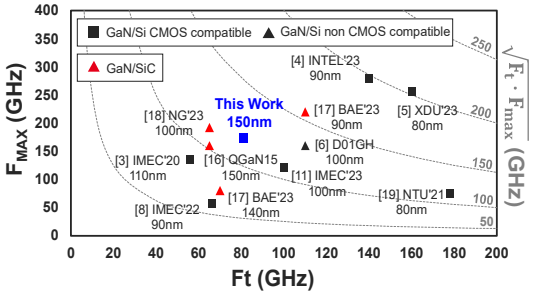

Fig.23: Comparison of F_{MAX} vs Ft for GaN/Si (black) and GaN/SiC (red) devices for L_G between 80nm and 150nm. This work (blue) shows state of the art Ft and F_{MAX} for L_G=150nm.