Specificities of linear Si QD arrays integration and characterization

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Abstract

The low temperature operation of quantum computing devices implies developing characterization protocols, from extensive statistical tests to targeted device screening at cryogenic temperature. This paper reviews major integration constraints arising in linear Si quantum dots arrays and their implication on both the device operation and electrical characterization.

Keywords: quantum dots, qubits, FDSOI, variability

Introduction

Si spin qubits are a solution investigated by multiple teams across the world to serve as core quantum chip [1][2][3][4]. One major advantage of Si quantum dots (QD) is their natural ability to scale to large arrays, with fabrication processes very similar to CMOS technology. An example of such linear QD array is presented in Fig. 1. Compared to transistors, characterizing QD arrays requires dedicated test procedures. This is mainly due to the low temperature of operation of quantum devices. To this end, a three steps characterization protocol is ideal (Fig. 2) to monitor relevant figures of merit at the considered temperature and characterization speed. QD arrays also differs from transistors at the design level, as they require single charge detection. Multiple detection schemes exist [5], yielding various device designs (Fig. 3) for which additional modules are required. In the development phase, to fairly benchmark this set of layouts with significant impact on the device operation, a neat optimization of the process is required. This paper reviews the associated characterization and electrical validation protocols.

Linear gate arrays

The linear arrangement of gates constitutes a first major difference. While unitary transistors are surrounded by source-drain regions, the inter-gate regions of linear quantum dot arrays need to remain intrinsic to allow direct tunnel coupling between neighbor QD. Coupling to charges reservoirs also requires optimized junction engineering or additional access gates to help device initialization and readout. Operating a QD array as a standard transistor may consist in biasing it as one single gate device (Fig. 4) where all front gates (or plunger gates) are swept at the same time. In that case, significant variability in threshold voltage (V_{th}) and subthreshold slope (SS) is observed. Performing finer analysis of each gate reveals the source of such variability. Fig. 5 shows the behavior of each of the four front gates (FG) swept individually. While inner gates (G2 & G3) have state-of-the art figures of merit, their outer counterparts (G1 & G4) exhibit clearly larger V_{th} and SS spread, (Fig. 6). This is attributed to their proximity with junctions, leading electron density below outer gates to depend on dopant concentration as confirmed by TCAD simulation (Fig. 7). As a result, a larger variability is expected on outer gates due to random dopant fluctuations. Thus, operating outer gates as access gates –rather than to confine QDs enables to alleviate variability originating from edge effects. It is also an interesting lever to tune electrically dot coupling to the reservoirs.

Overlay in split gates designs

The split-gate design (Fig. 3) on FDSOI substrate offers versatile operability of QD arrays, enabling to work both in the exchange and readout regimes [4]. This face-to-face arrangement of the front gates is obtained by a dedicated "cut" lithography. Fig.8 shows the I_dV_g characteristics of two front gates facing each other. Shifted transfer curves are a clear indication of a physical asymmetry at the morphological level. In this case, a smaller (larger) coverage of the qubit layer by the right (left) front gate is expected, due to misalignment of the cut lithography step. In comparison to a symmetric configuration, this misalignment increases (reduces) the right (left) front gate V_{th}, as expected from TCAD simulations. Even when some V_{th} mismatch is considered acceptable at 300K, one can expect exacerbated asymmetry at 2K and below due to the ΔV_{th} temperature dependence, as illustrated in Fig. 9. Strict overlay control is therefore a key parameter in order to ensure ideal operability of split gates devices.

Defect-free inter-gate regions

One major source of yield loss in Si QD arrays is spurious dots within the qubit layer. Although they can be spotted in the form of parasitic lines on stability diagrams (Fig. 10), revealing spurious dots earlier in the characterization chain –during 300K tests for example is preferred for the sake of learning cycle time. However, standard transistor parametric tests are unsuitable to reveal such defectivity. Fig. 11 illustrates a method specifically designed to highlight the presence of inter-gate defectivity using 300K characterization. This technique consists in monitoring the screening effect inter-gate defectivity has on the exchange gate polarization. For negative values of V_J, the front gates V_{th} is poorly shifted when inter-gate defectivity is present.

On the process side, a possible solution to suppress spurious dots is to avoid using any implantation steps, as those can introduce defects or parasitic dopants in the qubit layer. However, well doping, which is required for back-biasing, is uneasy to achieve when deprived from any implantation step. A possible option effective at cryogenic temperature consists in implementing a metallic backgate electrode, so the backgate is no longer subject to dopants freeze out [6]. In the example shown in Fig. 12, a TSV-like backgate was etched by DRIE through the substrate landing on the lower BOX interface, followed by CVD metallization. Functionality of this approach is verified at 200mK, yielding a similar body factor to the one at 300K (Fig.13).

Conclusion

Given their specific designs and integration constraints, new measurement protocols are required to characterize FDSOI QD arrays. Adapting 300K parametric test procedures offers the possibility to gather statistical data on the expected device behavior at cryogenic temperature. New methodologies and metrics, such as the ones presented in this paper, are developed to speed up learning cycle time in the development of large scale quantum computing.

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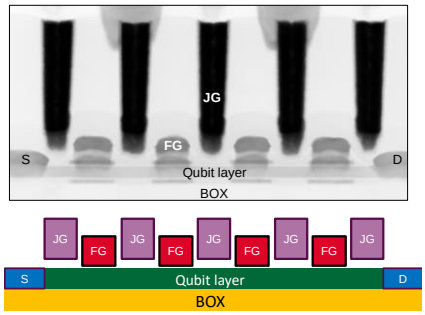

Fig. 1: TEM image of a 4-Front Gates (FG) QD array with exchange gates (JG), and corresponding schematic cross section.

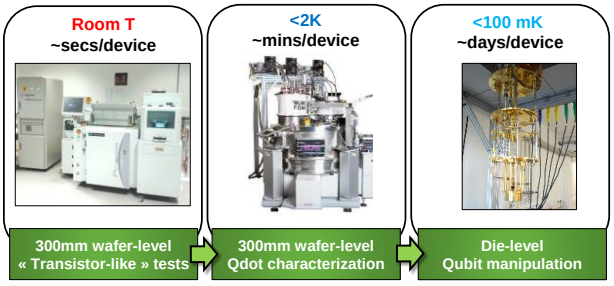

Fig. 2: Diagram of the 3-steps characterization chain of QD arrays performed at CEA-Leti, with various temperature and throughput constraints.

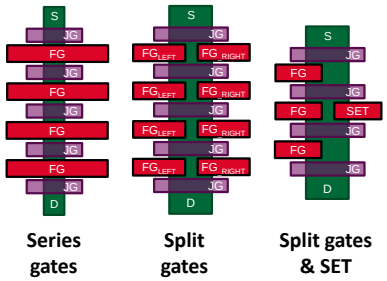

Fig. 3: Examples of linear QD arrays designs. FG: front gate, JG: exchange gate, SET: single electron transistor.

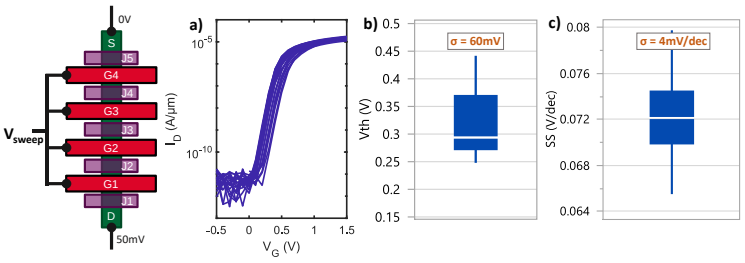

Fig. 4: I_dV_g characteristics at 300K of a 4-FGs array with simultaneous sweep of all FGs (a); Extracted threshold voltage (b) and subthreshold slope (c).

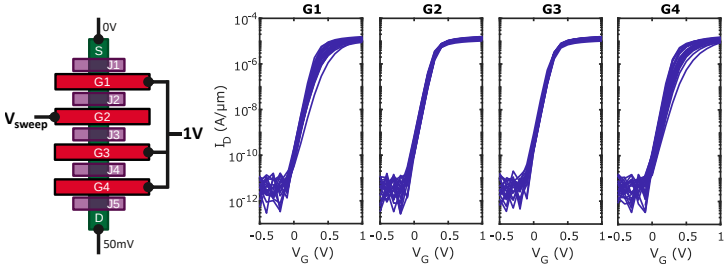

Fig. 5: I_dV_g characteristics at 300K of each individual FG when the three other gates are set to 1V. Larger spread is observed on outer gates (G1, G4).

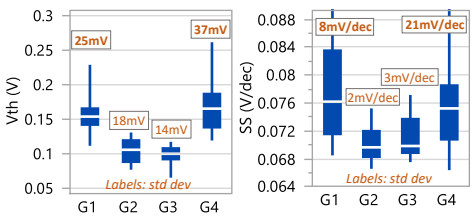

Fig. 6: Extracted threshold voltage (a) and subthreshold slope (b) for each front gate at 300K. Standard deviation is labelled for each gate boxplot.

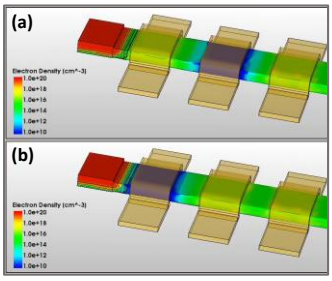

Fig. 7: Electron density in the qubit layer when sweeping inner (a) & outer (b) gates. Black lines: dopants distribution.

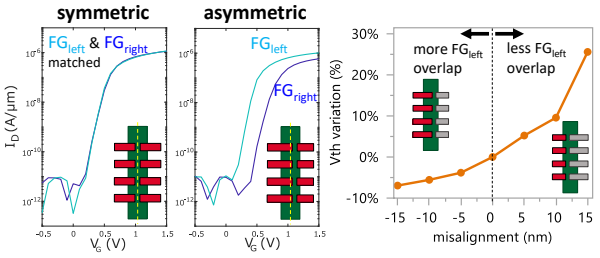

Fig. 8: I_dV_g characteristics at 300K of two FGs facing each other with symmetric (a) and asymmetric (b) coverage of the qubit layer. Expected V_{th} variation vs CUT misalignment from TCAD (c).

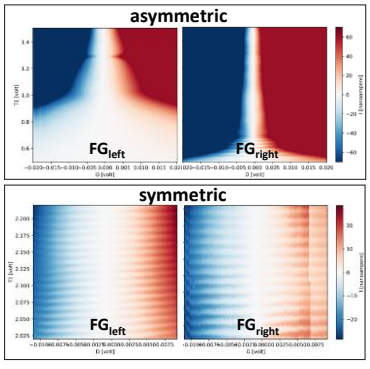

Fig. 9: Coulomb diamonds diagrams of a split gate device with asymmetric vs symmetric gates at 2K.

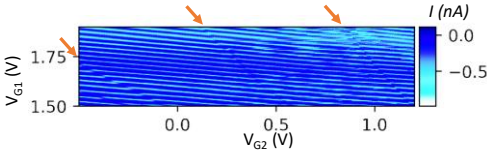

Fig. 10: Stability diagram of a split-gates device obtained at 2K. Spurious dot signature appears though diagonal dark lines.

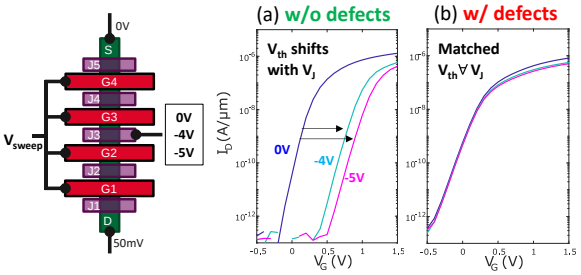

Fig. 11: I_dV_g FGs sweeps at 300K for various exchange gate voltages (V_J), in the presence (a) or absence (b) of inter-gate defects. Such defects inhibit the V_{th} shift expected at negative V_J.

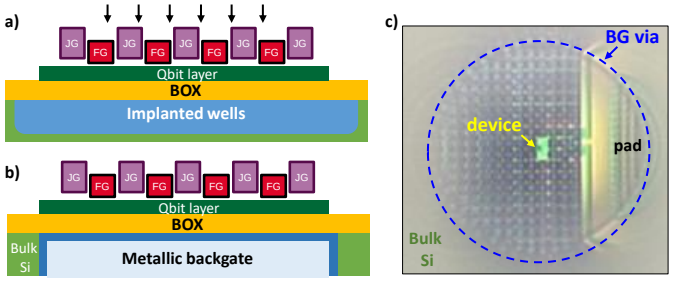

Fig. 12 : Schematic cross section of implanted wells (a) vs metallic backgate (b) integration. Corresponding optical microscope image of the backgate through-silicon-via observed post cavity etch (c).

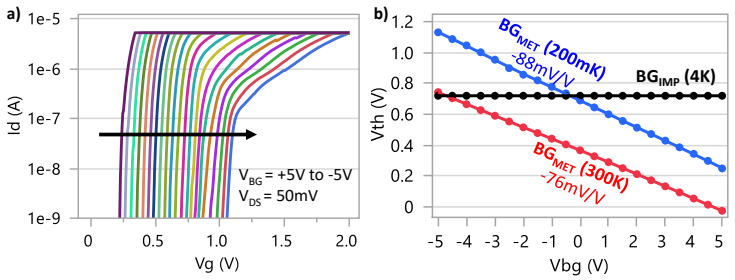

Fig. 13: I_dV_g sweeps at 200mK of a single gate device featuring a metallic backgate for various backgate polarization V_{BG} (a). Extracted V_{th} vs V_{BG} lines show similar slopes at 200mK and 300K (b), suggesting functional back-biasing at cryogenic temperature.