Buried PN junctions impact on the performances of an inductor at RF frequencies in the presence of parasitic surface conduction

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Buried PN Junctions Impact on the Performances of an Inductor at RF Frequencies

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***Abstract*—This paper shows the effect of buried PN junctions on the performances of inductors, and investigates the limitation of the subsequent substrate losses. We provide a simple and robust model that enables a precise evaluation of the substrate losses for devices fabricated on various substrates, and using various PN junctions implantation conditions. We point out that buried PN junctions are very efficient to counter the parasitic surface conduction, increasing the quality factor of inductors by more than 30% in the best experimental conditions. However, this integration does not reach the same performance level as trap rich substrates measured in the same conditions.**

***Index Terms*—parasitic surface conduction, inductors, substrate resistivity, RF, mmW**

I. Introduction

The integration of passive devices at high frequency induces a demand for higher resistivity substrates in order to decrease the losses in the silicon. However, the actual resistivity is limited by the appearance of a conductive layer at the interface between the high resistivity silicon wafer and the dielectric layer lying upon it. Said layer is called parasitic surface conduction (PSC) [1]. New integration techniques were implemented in order to obliterate this parasitic feature, such as buried PN junctions [2]–[4], which is the alternative explored in this article. This integration is compatible with SOI substrate, in zones where the SiO_2 Box is removed locally. Similarly to what has been developed in the case of coplanar waveguides, in this paper, we propose to evaluate the substrate losses for inductors by extracting the substrate resistance it experiences (R_{Sub}) on the model section III. Furthermore, we compare the improvement that buried PN junctions can provide to inductors, using various substrates resistivities, from standard (10 - 15 Ω.cm) to high resistivity (HR), and with various PN implantation conditions.

II. Fabrication of the devices

The inductors fabricated were integrated on silicon substrates of various nominal resistivities. In order to have a reference, standard substrates (15 Ω.cm) were used, as well as high resistivity ones (HR), with nominal resistivities ranging from 0.5 to 5.7 kΩ.cm. In order to address the well-known issue of PSC, we have also used wafers with a thick trap-rich polysilicon layer on top (TR), with 4.7 kΩ.cm nominal bulk resistivity, and the RF behaviour of which is known to be excellent [5]. On all wafers, the process carried out was identical for the dielectric layers of the back end of the line (BEOL), and the metallisation process. The metallisation layers used correspond to a metal level and a thick copper layer, equivalent to usual top Aluminium metal in terms of resistivity. In order to reduce the PSC, underneath some devices, we implanted alternatively P and N, so that the PN patterns follow the metallisation loop, as proposed in [2]–[4]. The implants are designed to reach approximately the same depth and concentration of dopants. The energy values chosen are 15 keV for the boron, and 35 keV for the phosphorus, and a dose variation is defined as follows:

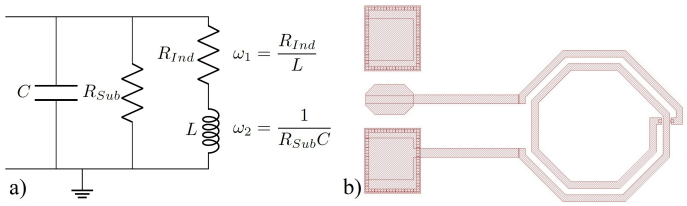

Fig. 1. a) Electric model representing the inductor, and characteristic pulsations ω_1 and ω_2; b) Schematic of the inductors studied.

TABLE I
Doses implanted per quadrant

Quadrant	Q1	Q2	Q3	Q4
Dose (cm^{-2})	5×10^{12}	1×10^{13}	2×10^{13}	4×10^{13}

The optimal conditions can be achieved finding the most adequate tradeoff between the implantation pitch and the implantation energy to passivate in depth and have abrupt junctions at the same time. With a 320 nm pitch, the devices studied are in a favorable configuration, even though fine tuning is still possible for minor performance improvement.

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III. Modelling and Extraction of Physical Parameters

We can consider that an integrated inductor can be described by a simple electrical model composed of a RL circuit that is actually the metallic loop of interest which is shorted by an RC circuit [6], [7]. This approach takes into account the substrate equivalent capacitance, the resistance of the PSC, and the conductance through the substrate. This simplified approach is valid under the assumption $C \ll C_{Pads} \approx 1$ pF, where C_{Pads} is the capacitance between the pads of the inductor and the substrate. This equivalent circuit is depicted in Fig. 1. We can evaluate the parameters of this model using S parameter measurements that were carried out using a Vector Network Analyser (VNA) between 100 MHz and 40 GHz. Assuming the substrate resistance to be much higher than the metallic loop resistance, we obtain R_{Ind} as the real part of the impedance at low frequency. Furthermore, considering that the two cut-off frequencies of the system involved are much different ($\omega_2 \gg \omega_1$), we can obtain the value of L by considering that the cut-off pulsation ω_1 is reached when the real and imaginary parts of the impedance are balanced. We can then evaluate the capacitance C by considering that the impedance modulus is maximised at the frequency $\frac{1}{2\pi\sqrt{LC}}$. We can eventually extract the value of R_{Sub} by fitting the modulus of the impedance over the frequency span measured. This procedure provides us with a robust evaluation of the parameters of the equivalent circuit considered, and lets us obtain values that represent well the physical aspects of the circuit. The extraction of the physical parameters composing the analytical model of the inductance proposed above is presented in Fig. 2. For each quantity, we present the values obtained as a function of ρ_{Sub}. In addition, we separate devices according to the implant conditions (Q1 to Q4, and No PN), in order to emphasize their influence on the behavior of the device.

Amongst the four quantities involved, three (namely the device resistance R_{Ind}, the capacitance C and the inductance L) are experimentally constant, regardless of the substrate variations, or the buried PN junctions underneath the device measured. Furthermore, the values obtained for R_{Ind} and L match our expectations, given the resistivity of the metallisation for R_{Ind}. The absence of variation of these parameters comforts us in the robustness of the extraction of the inductance parameters, and enables us to consider with confidence the substrate resistance R_{Sub}. We can see in Fig. 2 that for a given type of PN implantation condition, R_{Sub} increases with ρ_{Sub}, (with the exception of the TR wafers), reaching a plateau for $\rho_{Sub} > 0.5$ kΩ.cm. Above this resistivity, ρ_{Sub} becomes irrelevant, the substrate behavior being determined by the PSC and the depth of the PN junctions, as expected from [1].

Furthermore, we can observe the natural FOM of an inductor that is the maximum Q_{Max} of the quality factor obtained as the ratio of the imaginary part of the impedance and its real part. We can see in Fig. 3 b) that Q is significantly improved using a HR substrate, with values increasing from

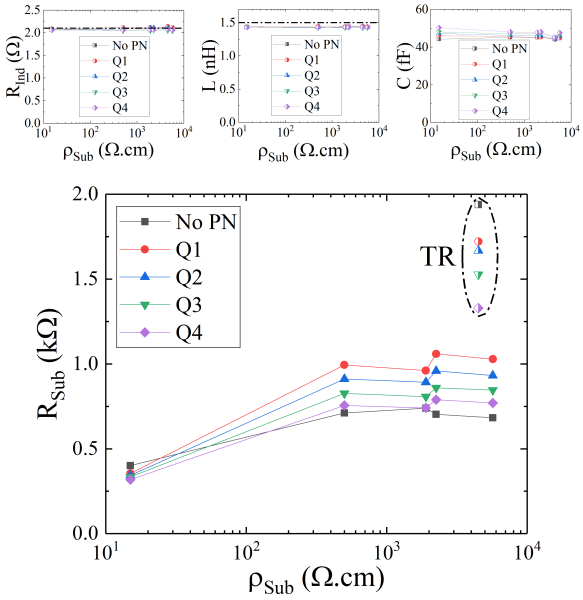

Fig. 2. Extracted parameters from small signal measurements as a function of the substrate resistivity.

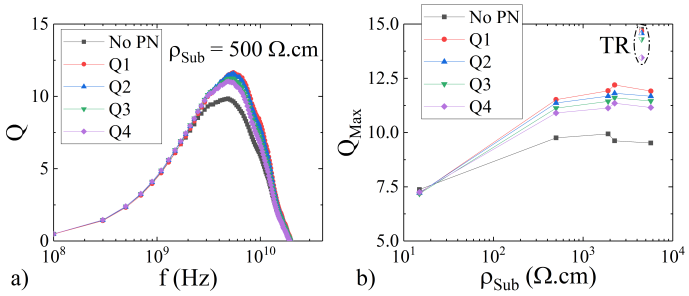

Fig. 3. a) Q as a function of the frequency for inductors with various PN conditions on a 500 Ω.cm wafer; b) Q_{Max} as a function of ρ_{Sub} for various buried PN junctions conditions.

7.5 (Std) to at least 9.5 (HR, TR) for any condition of buried PN junctions. However, as for the R_{Sub} parameter, ρ_{Sub} has a negligible influence on Q for HR substrates that do not have a TR layer, as shown on Fig. 3 a).

One can consider the impact of R_{Sub} on Q_{Max} from Fig. 4. We can clearly see that using an HR substrate enables an increase of R_{Sub} of half a decade, whereas the TR substrates increase R_{Sub} by nearly a decade. Furthermore, we can also see that despite the substrate enhancement provided by TR substrates, the ideal performance obtained in the configuration where R_{Sub} is infinite, yielding a value for Q_{Max} of Q_∞ is far from accessible. Therefore, we propose a comparison to the value of Q_{Max} one should get using a state-of-the-art 40 kΩ TR wafer (green star), which gives a current limit to aim at. Let us precise that this estimate assumes a linear variation of R_{Sub} with ρ_{Sub} for TR substrates, which is likely to provide an overestimate. It is noticeable though that both buried PN junctions, and to a larger extent TR substrates, provide a dramatic increase of Q_{Max}.

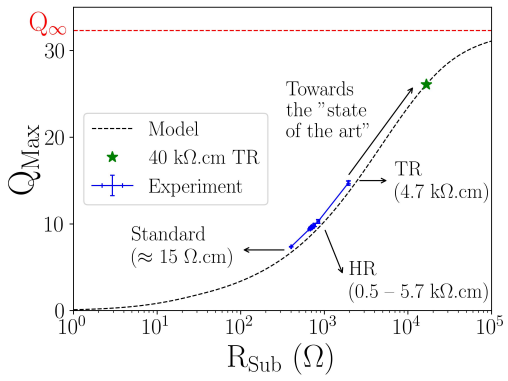

Fig. 4. Q_{Max} as a function of R_{Sub} for both experimental data and model, in regard to the limit Q_∞ corresponding to R_{Sub}=+∞. The green star represents the estimated value of Q_{Max} using a state-of-the-art 40 kΩ.cm TR wafer.

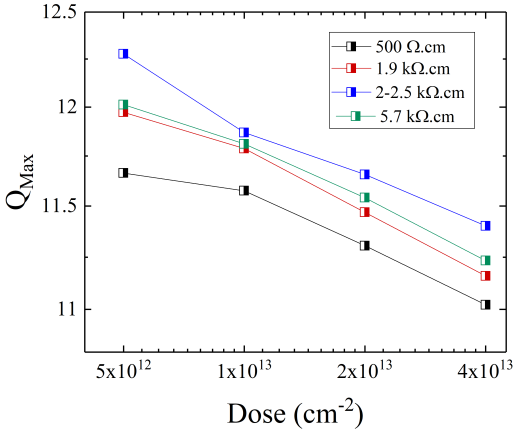

Fig. 5. Q_{Max} as a function of the dose implanted in the buried PN junctions.

IV. Impact of buried PN junctions

A remarkable feature that one can notice from Fig. 3 b) is the systematic enhancement of Q_{Max} using buried PN implants (Q1 to Q4) instead of none (No PN), for all the substrates, except for the TR wafers. The enhancement of Q_{Max} reaches 10% (Q4) to more than 20% for the best implantation condition (Q1). In order to have more insight on the dependence of Q with respect to the buried PN junctions, we represent the evolution of Q_{Max} as a function of the dose of dopants implanted under the inductance in Fig. 5. On this graph, we can see that Q_{Max} decreases when the doping dose is increased, for all the substrate resistivities. We can also point out the fact that the highest ρ_{Sub} substrate (green curve) does not provide the highest values of Q_{Max}, which emphasises the importance of considering R_{Sub} to assess the substrates performances.

In order to understand the dose dependence of Q_{Max}, let us consider the fact that in first approximation, the depletion width of the junctions depends on the sum of the active concentrations in the P and the N zones. It is therefore expected that a decreasing implanted dose increases the width of each depletion zone, leading to a more resistive layer in average. This explanation may account for the variation of Q_{Max} that is observed experimentally: indeed, a multiplication of the dose by a factor 2 induces a net decrease of Q_{Max} by approximately 0.3.

Concerning the results involving the TR substrates, one can observe that the dependance on the implants is different from the one in usual HR substrates. Indeed, any implantation decreases Q_{Max} as well as R_{Sub}, and the larger the dose the worse the degradation. This can be understood by the expected decrease of resistivity due to polysilicon doping. Additionally, we can consider the mechanisms at stake in the TR layer: the role of this layer relies on the fact that numerous traps are present, limiting the displacement of charge carriers. One can expect that by implanting doping species, the traps get occupied by the ionised impurities. The density of traps available to kill the charge transport is then decreased, leading to a R_{Sub} decrease, and a subsequent increase of the losses in the substrates, translating in a decrease of Q_{Max}.

V. Conclusion

This study shows that a simple electrical model enables to capture the behavior of an inductor, and separate the influence of the substrate losses from small signal measurements, using the parameter R_{Sub}. The beneficial influence of the buried PN junctions is also clearly shown, with an optimum to find for low doses implanted, even though it is clearly less advantageous than TR substrates. We have also pointed out that the dissipative behavior of the substrate cannot be completely overcome, even using the best techniques available currently. Therefore the performance that can be set as a goal to reach is still Q_{Max} obtained in the case of TR wafers.

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