Drain voltage impact on charge redistribution in GaN-on-Si E-mode MOSc-HEMTs

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***Abstract* — In this paper, we review the nature of traps population and the transport mechanisms in GaN-on-Si E-mode MOS channel HEMTs during High Voltage Bias Temperature Instabilities (HV-BTI) test under various temperatures (T), drain voltage stress ($V_{DSstress}$) and gate voltage stress ($V_{GSstress}$) conditions. Thanks to experimental setup using ultra-fast $I_D(V_G)$ to monitor V_{TH} during both stress and recovery phases from 10µs to several kiloseconds. The temperature dependent measurements show that V_{TH} and R_{ON} degradations are related to the same trap nature the C_N deep acceptor traps in GaN:C layer. Two different mechanisms during the stress phase are found, first C_N traps deionization, impacted by $V_{DSstress}$, then the nBTI behavior influenced by $V_{GSstress}$. It is found that high drain voltage stress (≥ 200V) induces a charge redistribution predominantly awards the drain node, while a lower drain voltage stress led to a charge redistribution in the source-gate region.**

***Keywords*- Dynamic reliability, GaN-on-Si MOSc-HEMT, HV-BTI, V_{TH} instability, Carbon in GaN**

I. INTRODUCTION

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) are promising devices for power application (650V rated) thanks to its superior physical and material properties [1], [2]. While the wide bandgap and the breakdown voltage enables a high voltage operation, the presence of a large 2-Didimensional electron gas (2DEG) with high mobility (2000 cm²/Vs) at the AlGaN/GaN interface leads to a high current density. However, one of the biggest issues of GaN-based devices is the stability of the main parameters: ON-state resistance (R_{ON}) and threshold voltage (V_{TH}) under harsh conditions [3]–[5]. These parameters degradations can affect the transistor lifetime and its dynamic performance during operation [6]. Recently a new effort focused on High Voltage Bias Temperature Instabilities (HV-BTI) helped to understand the interplay between epitaxy and the threshold voltage shift (ΔV_{TH}) and dynamic ON-resistance (ΔR_{ON}) [7]. Indeed, introducing carbon doped (GaN:C) layer to make a semi-insulating buffer is responsible for peculiar trapping mechanisms [8]. Carbon is considered as one of the main contributors to the degradation of the dynamic performance and reliability of GaN-based devices. This study presents a thorough analysis of HV-BTI degradations through temperature, drain (V_{DS}) and gate (V_{GS}) voltage dependences on V_{TH} instability during the stress and the relaxation phases.

II. DEVICES DESCRIPTION AND EXPERIMENTAL SETUP

Fig. 1 illustrates the schematic cross section of the fully recessed gate for 8" GaN-on-Si MOSc-HEMTs with a 30nm Al_2O_3 gate oxide. The different layers are grown on p-type Si substrate using Metal Organic Chemical Vapor Deposition (MOCVD). First, a transition layers are deposited dedicated to strain management followed by a Carbon doped GaN (GaN:C) layer, to ensures a vertical and lateral electrical insulation and improves GaN breakdown voltage. Then, an unintentionally doped GaN layer (GaN:UID) is deposited to form the conductive channel. An AlGaN barrier with top SiN passivation layers are deposited leading to a 2DEG at the AlGaN/GaN interface. Finally, a part of GaN:UID and the AlGaN are locally remove, the 30nm Al_2O_3 gate oxide is deposited in this recessed area using Atomic Layer Deposition (ALD) followed by the gate metal layer deposition. In this study, all the tested transistors have a gate

width (W_G) of 8mm, both gate length (L_G) 1 and 2µm are used, while the gate to drain and gate to source distances (L_{GD} and L_{GS}) are constant.

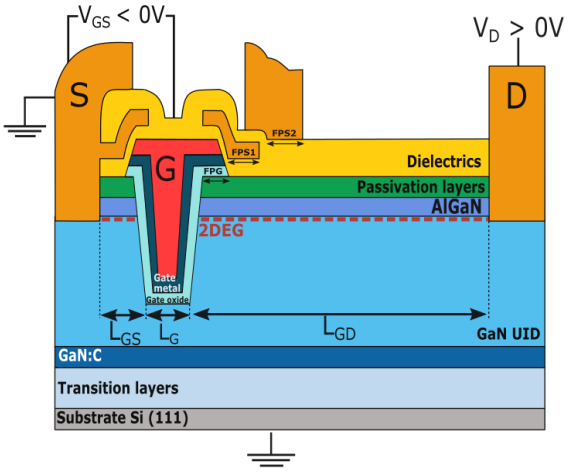

Figure 1. Schematic of the GaN-on-Si E-mode MOSc-HEMT illustrating full-recessed MOS gate with the voltage applied on source, gate, drain and substrate during HV-BTI.

The gate and drain voltage pattern of HV-BTI measurement is highlighted in Fig. 2 and is similar to the one used in [7]. During the stress phase a fixed high drain voltage stress ($V_{DSstress}$) and a negative gate voltage stress (with $V_{GSstress}$ < V_{TH}) are applied. The recovery phase was performed immediately after the end of the stress phase (with ~1µs of delay) where both gate and drain are grounded ($V_{GSstress}$ = $V_{DSstress}$ = 0V). During these phases, a logarithmically spaced V_{GS} pulse is applied to extract V_{TH} and/or R_{ON} from a fast $I_{DS}(V_{GS})$ ramp (less than 15µs to minimize the unwanted recovery during stress). Fig. 3 depicts

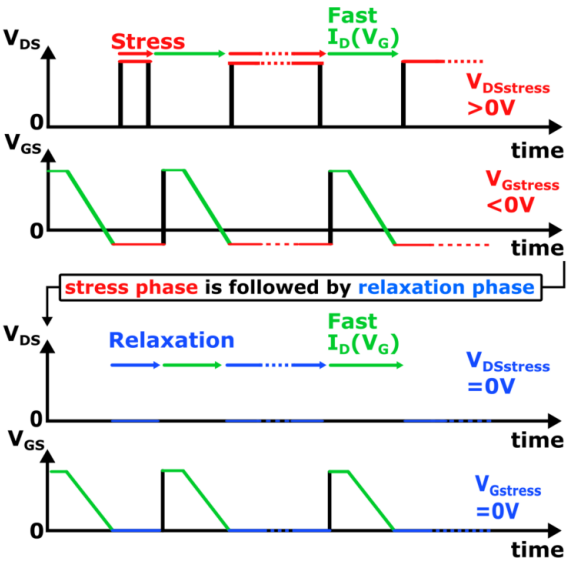

Figure 2. Chronogram showing signal transients during stress and relaxation operations of the HV-BTI test during threshold voltage measurement. An ultra-fast $I_{DS}(V_{GS})$ is logarithmically applied to V_{TH} measurement.

an example of $I_{DS}(V_{GS})$ characteristics during a gate stress of -1V and a drain stress of 100V during 10^2s (left) and during 10^2s of recovery (right) at 150°C. We can clearly observe a negative HV-BTI shift during the stress phase. Note that in your setup configuration V_{TH} is extracted in linear region with the constant current method (V_{TH} = V_{GS} @ I_{DS} = constant).

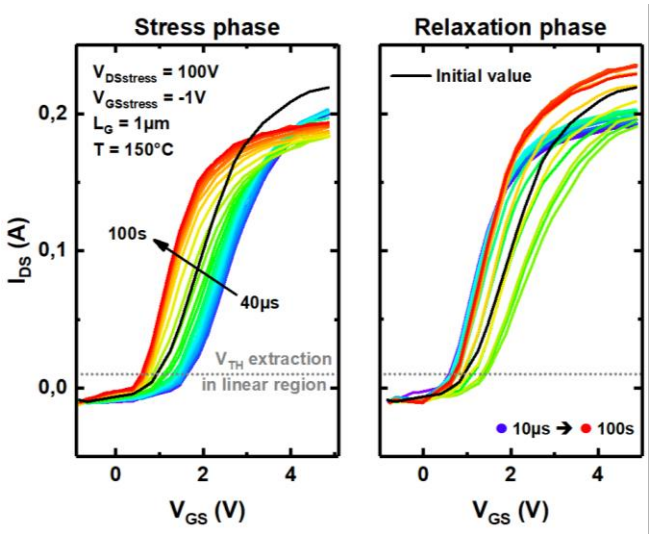

Figure 3. Ultra-fast $I_{DS}(V_{GS})$ characteristics during a stress phase at $V_{DSstress}$ = 100V, $V_{GSstress}$ = -1V during a stress and a relaxation of 100s at 150°C. The V_{TH} is extracted in the linear region @ I_{DS} = 30mA.

III. TEMPERATURE DEPENDENT ANALYSIS

ΔV_{TH} stress and relaxation transients obtained at various temperatures from 100°C to 175°C for a $V_{DSstress}$ of 100V during 10s and a relaxation time of 1000s are presented in Fig. 4. A temperature dependence is observed for both phases. During the stress phase, a strong ΔV_{TH} decrease reveals the stress time constant τ_s. At high temperature (>100°C), the degradation tends to saturate at long stress time @ $V_{GSstress}$ = -1V. While during the relaxation phase, a peak appears revealing the relaxation time constant τ_r. We can also notice that before and after this bump the ΔV_{TH} is very stable, we do not have any recovery during the relaxation phase. Thereby, both time constants are strongly activated with temperature.

To identify the nature of traps population involved, an Arrhenius analysis was carried out. First, stress and relaxation transients are fitted through a polynomial function. Then, the derivatives of both HV-BTI transients $\partial\Delta V_{TH}/\partial\log(t)$ were plotted (Fig. 5). The two-time constants τ_s and τ_r are extracted by taking the local extrema positions (minimum during stress phase and maximum for recovery phase) of the derivative curves for each temperatures (circle in Fig. 5). Finally, these minima/maxima (stress and relaxation time constant) are reported as a function of $q/(K_BT)$ in the Arrhenius plot in Fig. 6, where the ΔR_{ON} measurements results from [7] are also reported.

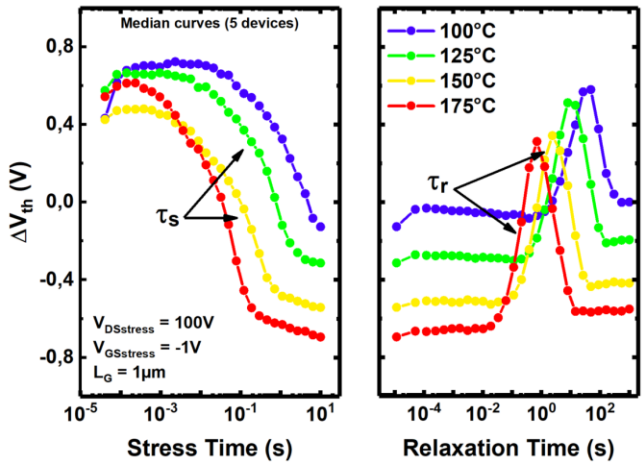

Figure 4. HV-BTI stress and relaxation transient extracted from $I_D(V_G)$ characteristics obtained for a stress of 10s at different temperatures T with $V_{DSstress}$ = 100V and $V_{GSstress}$ = -1V and during a relaxation of 10^3s. A strong ΔV_{th} variation reaveals times constants τ_s and τ_r. The curves represent a median over 5 devices.

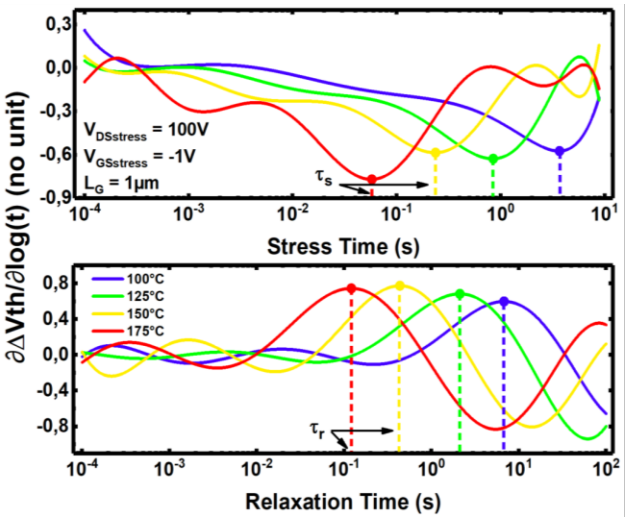

Figure 5. ΔV_{th} derivatives spectra for stress and relaxation phases. Time constants τ_s and τ_r are extracted through the local extrema (maxima and minima) of the curves at each temperature.

It can be noticed that an activation energy (E_A) around 0.8eV was found for both stress and relaxation phases. The same activation energy was found in [7] where the same test parameters was performed on dynamic ON-resistance. In the literature, several studies demonstrated that this energy is related to substitutional C traps in N sites of GaN lattice (C_N), which is a deep acceptor (0/-) with transition level at 0.8-0.9eV above the valence band [9]–[11]. We assumed that these carbon traps are responsible for ΔV_{TH} and ΔR_{ON} degradations during stress and relaxation transients.

Nevertheless, even if we obtain the same activation energy value, during both R_{ON} and V_{TH} studies, we can notice that during the stress phase two different Arrhenius localizations are identified, one for each measure type. The two different plot locations during the stress phase reveals that the ΔV_{TH} and the ΔR_{ON} refers to the same traps nature but not necessary to the same traps population. Therefore, different C_N traps are activated during ΔV_{TH} and ΔR_{ON} measurements.

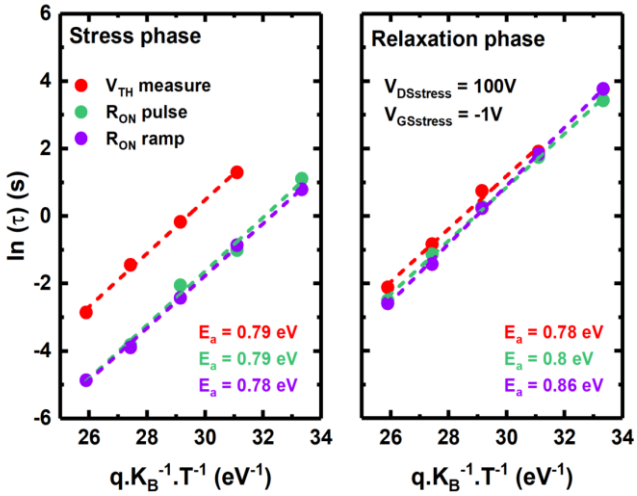

Figure 6. Arrhenius plot of time constants τ_s (right) and τ_r (left) for ΔV_{th} measurement (red plot) and for R_{ON} measurement (green and purple plot) from [6]. The same activation energy $E_A \approx 0.8$eV is extracted for both time constants and for all measurement types (V_{TH} and R_{ON}). This activation energy strongly assumed to be to C_N deep acceptor traps.

IV. TRANSPORT MECHANISMS

The influence of drain voltage on ΔV_{TH} during a stress and a relaxation time of 100s with a $V_{GSstress}$ of -1V at 150°C is presented in Fig.7. We can clearly see a strong link of $V_{DSstress}$ on ΔV_{TH} during both stress and relaxation phases. Firstly, we

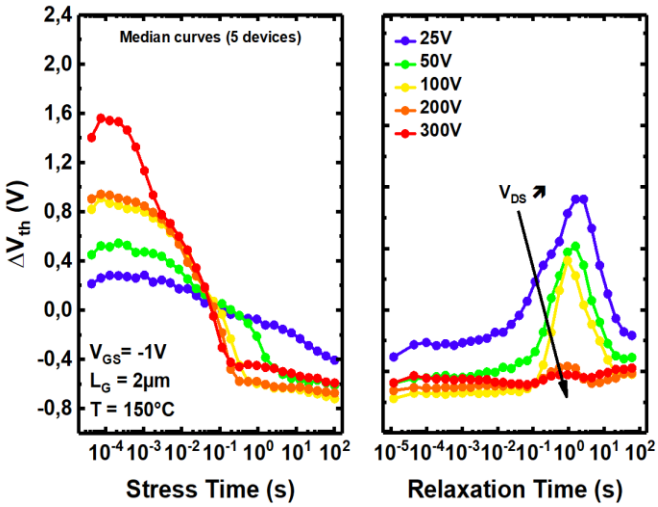

Figure 7. Drain voltage impact on ΔV_{th} for 100s of stress and relaxation at $V_{GSstress}$ = -1V for L_G = 2µm at 150°C. The curve represents a median over 5 devices.

can notice that the drain voltage increase initial ΔV_{TH} (threshold voltage in the ten/hundred microseconds of stress). While at the end of stress all transients (for $V_{DSstress}$ > 25V) converge at ΔV_{TH} ≈ -0.6-0.7 V. Therefore, drain voltage stress does not influence the final V_{TH} value. It is worth noticing for $V_{DSstress}$ from 100V to 300V that V_{TH} decrease follows exactly the same behavior. Finally, we can also note during the recovery phase that the peak amplitude with $V_{DSstress}$ up to its complete disappearance at $V_{DSstress}$ = 300V.

The influence of $V_{GSstress}$ on the ΔV_{TH} for a low and a high drain voltage (respectively 25V and 300V) is shown Fig. 8. We can clearly distinguish two different regimes during the stress phase. The first regime (left side of the dotted line) corresponds to the part where only the drain voltage affects the ΔV_{TH}. We have an initial ΔV_{TH} followed by a large decrease which is more important with $V_{DSstress}$ = 300V. These regimes have been attributed to C_N traps deionization in GaN:C layer (- → 0) under the gate [12] (illustrated in Fig. 11a). Indeed, during the first microseconds of stress (before measurement and 2-3 first points) the Fermi level alignment of GaN:C/GaN:UID leads to C_N traps ionization at the interface [13], which could explain the positive initial ΔV_{TH} impacted by the drain voltage. Indeed, a high drain voltage stress increase the space charge region under the gate and towards the drain, thus depletion area below the gate goes deeper in the epitaxy than at $V_{DSstress}$ = 25V. Thereby, the C_N trap concentration increases as well as the initial V_{TH}.

Then, these traps deionize through the transport of holes potentially from epitaxy to the 2-Dimensional Hole Gas (2DHG) at GaN:C/transition layers interface. The C_N traps deionization leads to a reduction of the p-doping effect of GaN:C and induces the ΔV_{TH} decrease. When the PN junction at GaN:C/GaN:UID interface which acts as a free hole potential barrier is removed, the charge deionization is completed. Next, a hole accumulation occurs at Al_2O_3/GaN interface which promotes nBTI behavior (as illustrated in Fig. 11b) (orange area, 2nd regime). The Fig. 8 shows that the gate voltage stress influences only the nBTI part of the V_{TH} transient during the stress phase.

Fig. 9 represents the ΔV_{TH} at the end of the stress (after 100s of stress) at various $V_{DSstress}$ as a function of $V_{GSstress}$. We can note that $V_{GSstress}$ have a strong impact on final nBTI value, but $V_{DSstress}$ does not have a lot of influence on ΔV_{TH} at the end of stress. Indeed, a strong negative gate voltage stress $V_{GSstress}$ increase the threshold voltage, which is is consistent with literature [6], [14].

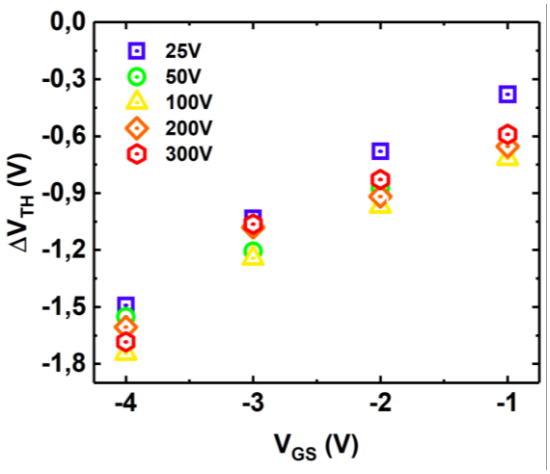

Figure 9. ΔV_{th} measured at the end of the stress phase after 100s of stress as a function of $V_{GSstress}$ for different drain voltage stress from 25V to 300V at 150°C.

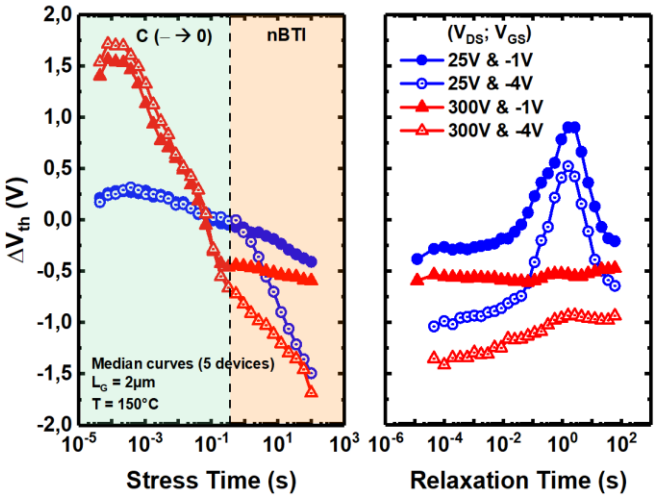

Figure 8. Gate voltage impact on ΔV_{th} for 100s of stress and relaxation for two different drain voltage stress (25V and 300V) for L_G = 2µm at 150°C. Two different regime is observed during the stress phase (1) C_N traps deionization (green) and (2) nBTI regime (orange). The curve represents a median over 5 devices.

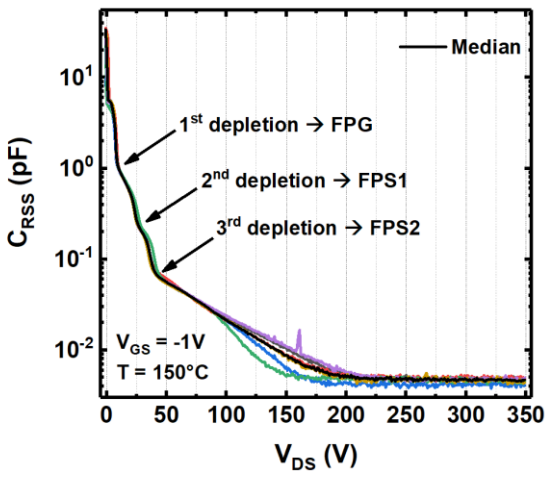

Figure 10. Experimental $C_{RSS}(V_{DS})$ at V_{GS} = -1V and T = 150°C, where field plates depletion is observed. After the FPS2 depletion the 2DEG continue to deplete until ~200V.

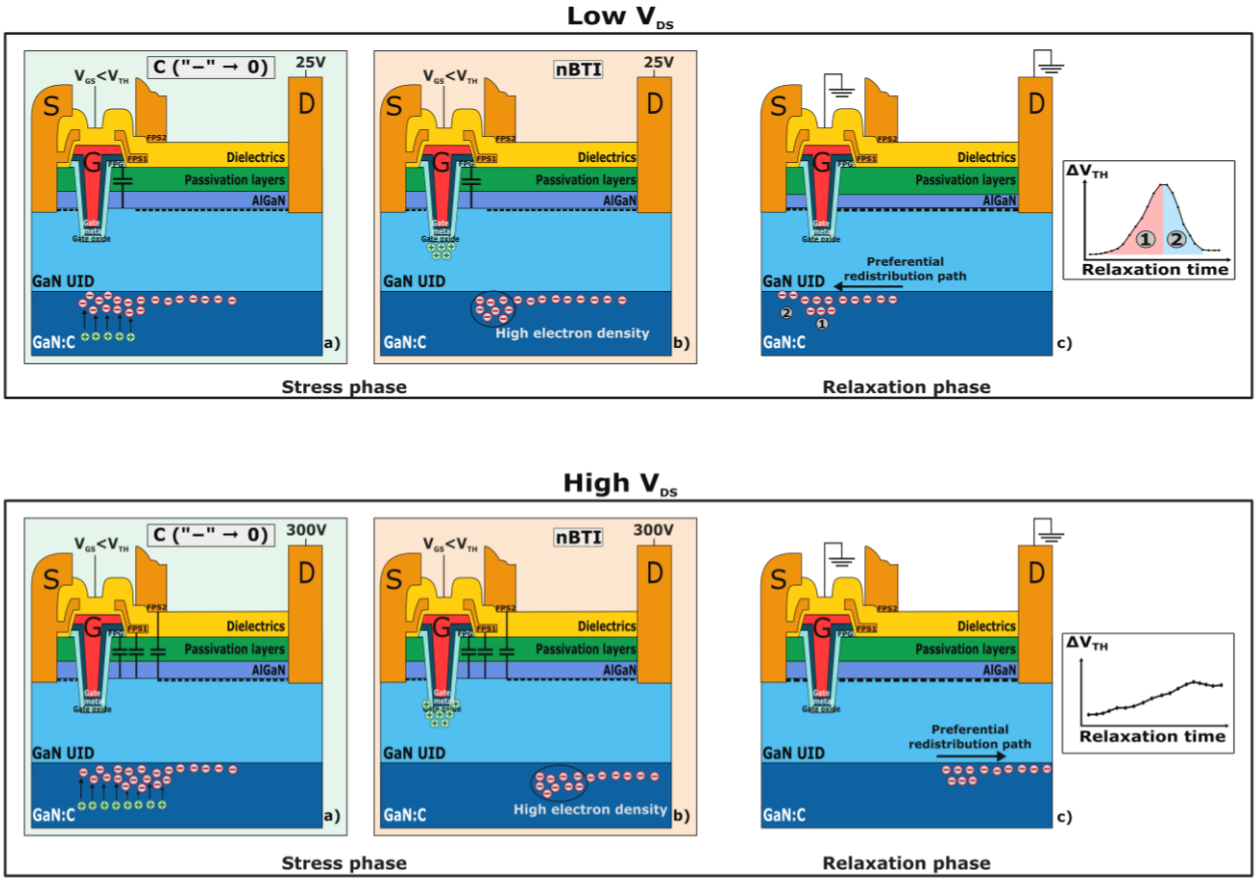

Figure 11. Schematic describing the charge density in access region during the different regime describing in Fig. 8. First, during the stress phase with (a) the C_N charge deionization occurs near the gate, (b) nBTI regime (hole accumulation occurs gate dielectric). Then (c) the relaxation phase in a MOSc-HEMT at low drain voltage stress ($V_{DSstress}$ = 25V) with only the gate field plate (FPG) activation which promote relaxation peak appearance (top) and at high drain voltage stress ($V_{DSstress}$ = 300V) with all field plates activation with no peak emerging (bottom).

Moreover, $V_{GSstress}$ does not affect the relaxation peak, which is only depends on $V_{DSstress}$. The relaxation peak disappearance can be explain by field plate activation at high voltage.

The $C_{RSS}(V_{DS})$ in Fig. 10 highlights the 2DEG depletion via field plate activation, which each bending (shifting) point correspond to the depletion of gate, source level 1 and source level 2 field plate (FPG, FPS1 and FPS2, respectively). In device, the 2DEG depletion is completes at $V_{DS} \approx 200V$, which is consistent with the relaxation peak disappearance presented previously in Fig. 7.

More generally, at low drain voltage stress field plate are not fully activated (for instance at $V_{DSstress}$ = 25V only FPG is entirely depleted). As mentioned previously, during the stress phase we have a relatively small space charge region under the gate and towards the activated field plate, consequently the majority of charge (C_N^-) are located near to the gate (Fig. 11a top). At the end of stress, we have some charges near the gate oxide and C_N layer (Fig. 11b top). We suppose that, during the relaxation phase charge redistribution occurring in the gate-source region at the GaN:UID/GaN:C interface. This charge redistribution implies a dynamic modification of V_{TH} relying on C_N^- charges travelling underneath the gate towards the source contact, leading to a backgating effect (Fig. 11c top). Whereas a higher $V_{DSstress}$ activates all field plates and leads to a strong 2DEG lateral depletion (for $V_{DSstress} \geq$ 200V). Therefore, a larger space charge region spreads until the FPS2 and the C_N^- moves further from the gate toward the drain (Fig. 11a bottom). This time, during the relaxation phase, the gate oxide and the C_N traps charges redistribution is mainly done by the drain node (Fig. 11c bottom), which removes the relaxation peak.

V. Conclusion

In this paper, we provide a thorough study of the HV-BTI instabilities in GaN-on-Si fully recessed gate MOSc-HEMTs. The influence of the temperature, drain and gate voltage have

been studied. We presumed that both ΔV_{TH} and ΔR_{ON} degradations were related to the same deep acceptor (C_N) traps localized in the GaN:C layer. We observed a strong drain voltage stress impact on the initial ΔV_{TH} and on the relaxation peak amplitude, while gate voltage stress had a huge influence on nBTI regime and accelerate the recovery. In addition, various transport mechanisms have been identified with two different path of charge redistribution. First, a low $V_{DSstress}$ leads to a redistribution path by the source node, which creates a relaxation peak transient related to carbon trapped charge redistribution under the gate. Finally, a high drain voltage stress leads to a large 2DEG depletion and the charge redistribution occurring in the gate-drain region.

ACKNOWLEDGMENT

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