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# Impact of Gate Morphology on Electrical Performances of Recessed GaN-on Si MOS channel-HEMT for Different Channel Orientations

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## Purpose of Work

This work is focused on AlGaIn/GaN MOS channel High Electron Mobility Transistors (MOSc HEMTs) with **fully recessed gate** on 200mm Si substrates (**Fig. 1**). We investigate the impact of the gate cavity **morphology** determined by both the AlGaIn/GaN **etching+wet** processes (**Fig. 2**) and the **channel orientation** (**Fig. 3**) on the ON-state performance. We present and validate an innovative analysis (based on electrical characterizations and TCAD simulations) for extracting **mobility** taking into account the two gate regions (sidewalls and bottom).

## Approach

The channel plane for these MOSc transistors [1-2] is usually GaN **c-plane (0001)**, with a **standard [1100]** oriented channel (labelled **0°**). Here for the first time we fabricated (with two processes [3-4], see **Fig. 1**) and characterized GaN transistors with different channel orientations (**Fig. 3**), from **0° to 90°** (ie [1100] to [1120]). We point out that the gate cavity shape depends not only on the etch-wet process but also on the channel orientation (**Fig. 6-8**), with two specific situations: 0° and 90° (resp. equivalent to 60° and 30° because of the GaN hexagonal crystal structure).

Extracted mobilities are typically related to the bottom ( $\mu_{bot}$ ) part of the gate cavity and only complex methods enable to evaluate sidewalls mobility ( $\mu_{sw}$ ) [6]. Here, we present and validate with TCAD simulations an innovative and fast **electrical characterization methodology** for extracting the different **mobility** contributions of the two-channel regions ( $\mu_{sw}$  and  $\mu_{bot}$ ).

## Results and Significance

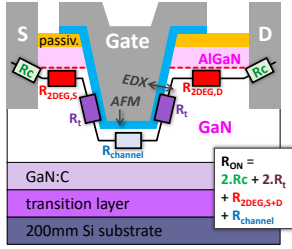
The channel orientation impact is highlighted in **Fig. 6** (measured  $V_{th}$ , SS,  $R_{ON}$  vs. orientation) and in **Fig. 8** which shows  $I_D(V_G)$  curves of 0-90° oriented devices for the two studied processes.  $R_{ON}$  reduction (-18%) is evidenced for process “with ALE & cleans” with respect to the “Reference” one. The respective contributions of the **sidewalls** and **bottom** regions are evaluated in **Fig. 9** (-50% transition resistance  $2.R_t$  and -16%  $R_{channel}$  from the  $R_{ON}$  partitioning). These improvements are due to gains for the corresponding motilities  $\mu_{sw}$  and  $\mu_{bot}$ . **Fig. 10** details the developed methodology (based on  $R_{ON}(L_G)$  curves,  $R_{ON}$  partitioning) which enables to extract separately the mobility for both regions. The method is then applied to 0° and 90° cases (**Fig. 11-14**). The final results (**Fig. 15**) show that the new process leads to +20% in  $\mu_{bot}$ , and +50% in  $\mu_{sw}$ . Similar results are obtained for the 90° orientation (**Fig.14-15**).

The ALE etching [3-4] is probably the first order parameter reducing the  $R_{ON}$  parameter for the new etching+wet process: the GaN surface is thus less damaged. This improvement appears to be more effective on the sidewalls w.r.t. the bottom region of the gate (c-plane).

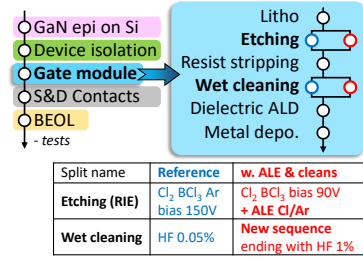
TCAD simulations [10] have been considered to assess the physical meaning of the extracted mobility values. By implementing the gate cavity shapes for the two processes and the two orientations (**Fig. 16**) and the  $\mu_{sw}$  and  $\mu_{bot}$  values at  $V_G=+6V$  (**Fig. 17**), we were able to reproduce the experimental  $I_D(V_G)$  curves (**Fig. 8-18-19**).

These results open path for in-depth analysis and optimization of power GaN transistors, in terms of etching/wet recipes, gate recess depth, temperature impact, and more aggressive gate lengths (**Fig. 20**).

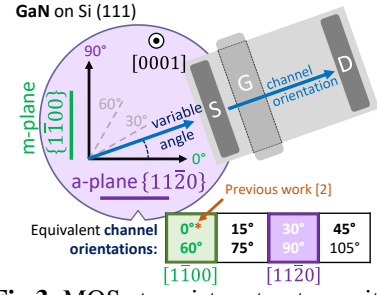
[1] P. Moens *et al.*, IEEE ISPD, 2014, pp. 374. [2] C. Le Royer *et al.*, IEEE ISPD, 2022, pp. 49. [3] C. Mannequin *et al.*, J. Vac. Sci. Technol. A 38, 032602 (2020). [4] S. Ruel *et al.*, J. Vac. Sci. Technol. A 39, 022061 (2021). [5] B. Rustemi *et al.*, SSE, Vol. 198, dec 2022, 108470. [6] R. Kom Kammeugne *et al.* IEEE TED Vol. 67, N°11, pp. 4649, Nov 2020. [7] E. B. Treidel *et al.*, IEEE JEDS, Vol. 9, pp. 215, 2021. [8] Y. Ando *et al.*, Appl. Phys. Lett. 117, 242104 (2020). [9] Y. Wang *et al.* IEEE TED Vol. 34, N°11, pp. 1370, Nov 2013. [10] M.-A. Jaud *et al.*, IEEE TED Vol. 69, N°2, 2022, N°2, pp. 669-674, Feb 2022.



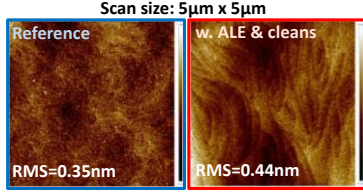
**Fig.1:** Structure of the fabricated GaN-on-Si MOSc-HEMT with fully recessed gate. The four  $R_{ON}$  components (Fig. 9) are also indicated.



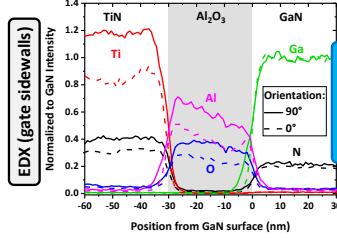
**Fig.2:** Process flow of the GaN/Si E-mode MOS channel HEMT with focus on the Gate module.



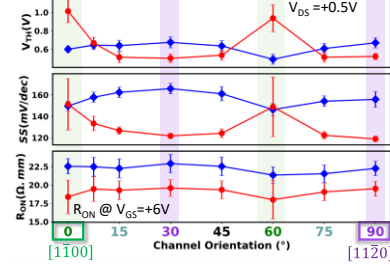
**Fig.3:** MOSc transistor structure with different channel orientations (0 to 90°) on the GaN-on-Si substrate.



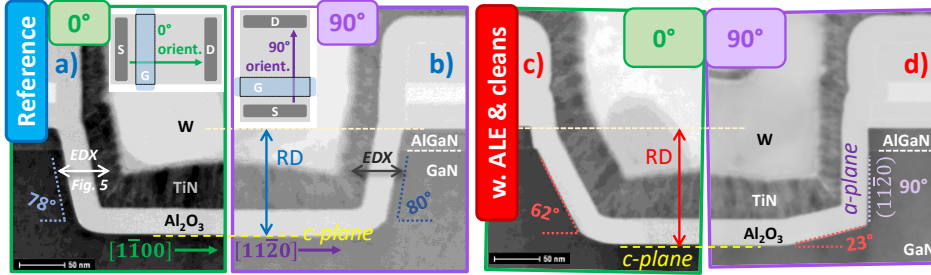
**Fig.4:** AFM images on 5nm Al<sub>2</sub>O<sub>3</sub>/GaN samples for the two splits. The ALE etching with new cleans lead to a surface with atomic plateaus (as observed on unetched GaN surfaces).



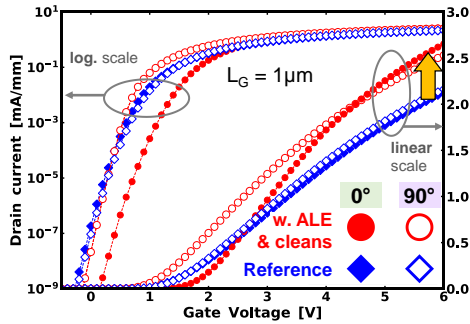
**Fig.5:** EDX profiles obtained for the reference process in the case of 0° and 90° oriented devices (same profiles for split 2).



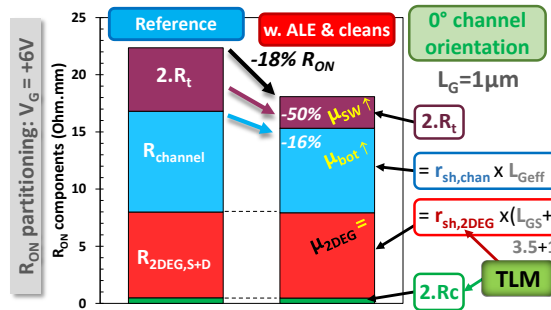
**Fig.6:** Impact of orientation angle on the extracted threshold voltage ( $V_{th}$ ), subthreshold swing (SS) and  $R_{ON}$  (wafer median, 20 sites).



**Fig.7:** TEM images of  $L_G=1\mu\text{m}$  devices (zoom on on one gate side) for two different channel orientations a-c) standard 0°, and b-d) 90°.

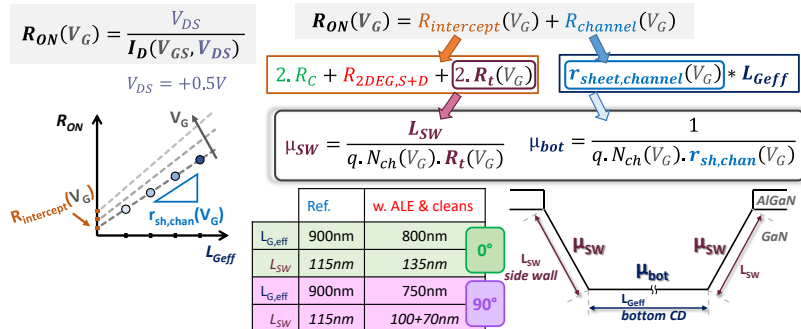


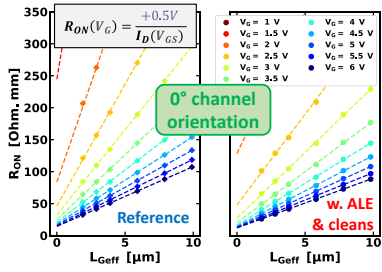
**Fig.8:** Experimental  $I_D(V_G)$  curves (wafer median values) at  $V_{DS}=+0.5\text{V}$ .



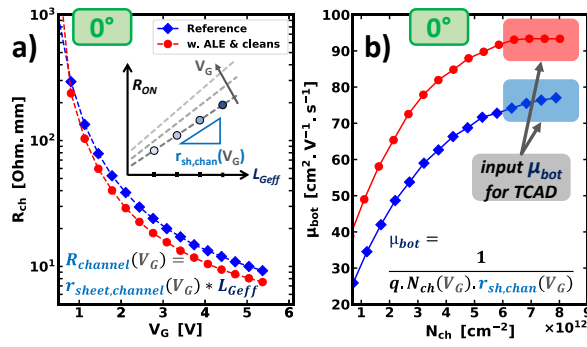
**Fig.9:**  $R_{ON}$  partitioning for  $L_G=1\mu\text{m}$  transistors (orientation 0°) obtained with the two processes (using the method from [2]).

**Fig.10:** Mobility extraction principle for the two regions of the gate (sidewalls and bottom chnnels).  $R_{ON}(L_G)$  curves combined with  $R_{ON}$  partitioning (and C(V) for electron density  $N_{ch}$ ) enable to extract separately the mobility for both regions, using the dimensions  $L_{G,eff}$  and  $L_{sw}$  from TEM images.

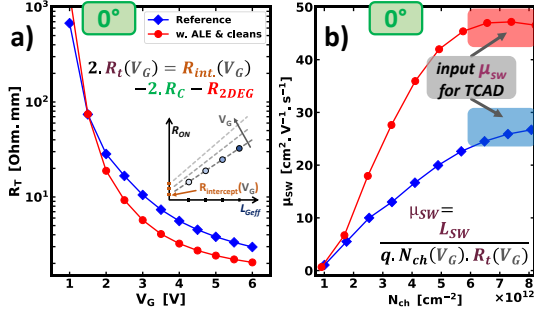




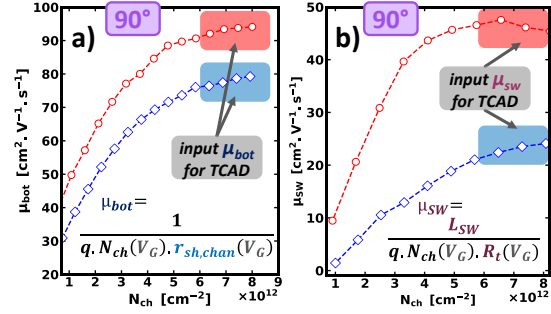
**Fig.11:** Measured  $R_{ON}(L_G)$  for different  $V_G$  of  $0^\circ$  oriented devices (wafer median, 20 sites).



**Fig.12:** Method results for  $0^\circ$  devices (for the two splits). a) Extracted  $R_{ch}$  vs.  $V_G$ . b) Electron channel mobility  $\mu_{bot}$  on the **bottom** part of the gate cavity.



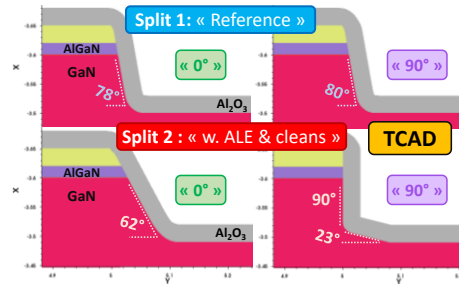
**Fig.13:** Methodology results for  $0^\circ$  devices (for the two splits). a) Extracted **sidewalls** resistance  $R_T(V_G)$ . b) Corresponding mobility  $\mu_{ch,sw}(N_{ch})$ .



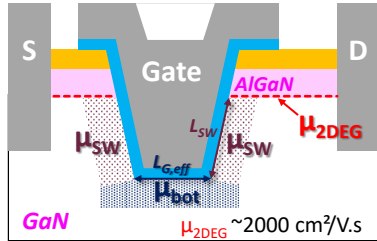
**Fig.14:** Results for  $90^\circ$  devices (for the two splits). a) Extracted electron channel mobility for a) the bottom region  $\mu_{bot}(N_{ch})$  and b) the side walls  $\mu_{ch,sw}(N_{ch})$ .

	Ref	w. ALE & cleans	previous work [6]	Vertical trench [7]	[8]	[9]
<b>GaN</b>	doped epi GaN/Si RD 125-135nm	uid epi GaN/Si RD ~130nm	uid epi GaN/Si RD ~130nm	ammonothermal GaN	uid epi/bulk GaN Norm. ON	uid epi GaN /sapphire RD 24nm
$0^\circ$						
$\mu_{bot}^*$ [1100]	76*	94*	125*	-	130*	250*
$\mu_{sw}$	27	46	-	-	-	-
	$L_G = 0.5-2\mu m$			$m$ -plane: 3	$L_G = 100\mu m$	$L_G = 22\mu m$
$90^\circ$				$a$ -plane: 6	-	-
$\mu_{bot}^*$ [1120]	78*	94*	-	-	-	-
$\mu_{sw}$	27	44	-	-	-	-
	$L_G = 1-10\mu m$					

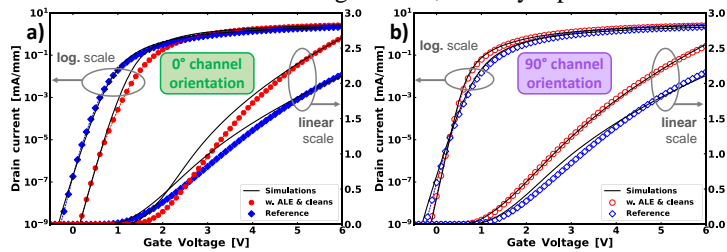
**Fig.15:** Summary table with extracted mobility values for this work (and comparison to published data, based on different GaN materials).



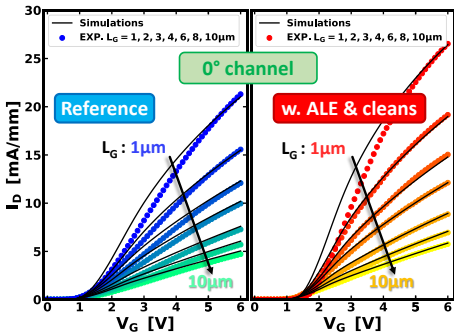
**Fig.16:** TCAD structures considered to simulate the 4 configurations, with Synopsis-Sentaurus.



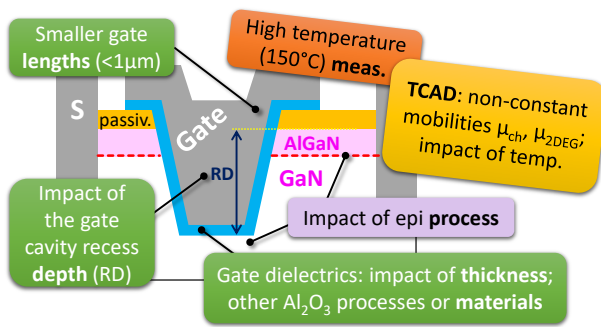
**Fig.17:** TCAD approach for taking into account the experimental mobility values (from Fig. 15).



**Fig.18:**  $I_D(V_G)$  curves comparison for  $0^\circ$  a) and  $90^\circ$  b) oriented devices onto measurements (symbols) and TCAD results (lines), at  $V_{DS}=+0.5V$  (for the two processes).



**Fig.19:**  $I_D(V_G)$  curves comparison for  $0^\circ$  oriented devices with different  $L_G$  between measurements (symbols) and TCAD results (lines).



**Fig.20:** Possible perspectives of this work (on processes, characterizations, simulations), dedicated to device physics understanding for performance optimization.