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# Engineered SiC materials for power technologies

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**Abstract**— SmartSiC™ engineered substrate are proposed to answer the power device needs for high quality, ultra low resistive materials. 150mm substrates demonstrate SmartCut™ technology potentials, opening path to defect free layers and 200mm substrates.

**Keywords**—SmartCut, SiC, SmartSiC,

## I. INTRODUCTION – SiC FOR POWER ELECTRONICS – SMARTCUT PROPOSAL

SiC Power Devices have emerged as a breakthrough technology for a wide range of applications such as traction inverter for automotive, DC/DC converter, on board charger or charging station [1]. Despite recent progress in 4H-mSiC material quality and supply continuously improving, progress regarding defect density and material performance are still needed.

SmartCut™ technology is known since decade to prepare engineered samples, industrializing up to high volume manufacturing, taking advantage of best donor and handle substrates. To answer SiC technology requirements, SmartSiC™ substrate combining a high quality, epi-ready, device layer on top of ultra low resistivity wafer is proposed. Figure 1 compares such proposal versus conventional bulk.

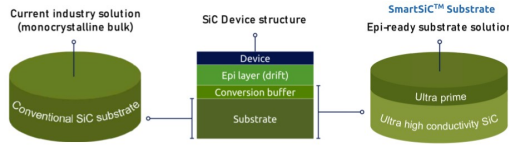


Figure 1: SmartSiC™ versus bulk mSiC substrate for power device

## II. SMARTCUT FOR SiC

Figure 2 shows how the SmartCut technology is adapted to SiC. It is based on several key steps like incoming surface preparation, hydrogen implant of the donor substrate to define a precise cleavage plan, offering state-of-the-art single-crystal SiC (mSiC) layer transfer, thinner than 1 micron. A primordial specificity of so-called SmartSiC substrates compared to Silicon on Insulator (SOI)-type products is the realization of a highly conductive bonding interface, to ensure excellent vertical conductivity through the SmartSiC substrate. The finishing steps ensure excellent roughness and thermal properties, to prepare a final epi-ready surface. The donor wafer is refreshed and re-used multiple times, opening the

path for high volume wafer production at optimized cost.

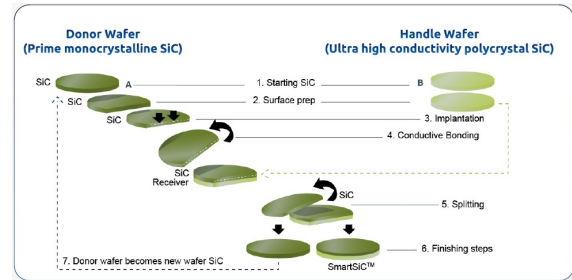


Fig. 1. SmartCut™ process description, as adapted to SiC

## III. LOW RESISTIVITY MATERIAL

Polycrystalline SiC (pSiC) handle wafer is prepared thanks to chemical vapor deposition (CVD) technique. It contributes to the environmental benefit of SmartSiC material, compares to the conventional physical vapor transport (PVT) used in the conventional mSiC bulk production. CVD growth, leading to typical micro-structure shown on Figure 3, is optimized in order to reach material target and to be compliant with SmartSiC process integration, then high volume manufacturing [2].

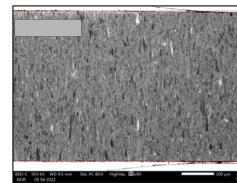


Figure3: Typical pSiC microstructure.

Thanks to high material doping, electrical resistivity of the pSiC substrate is improved by a factor of at least 4, up to 10 times, compared to conventional mSiC bulk. Figure 4 shows typical electrical resistivity mapping on both substrates.

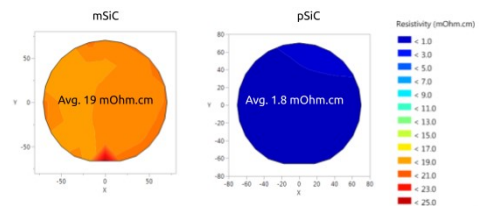


Figure 4: Resistivity mapping by Eddy Current. mSiC (left), pSiC (right)

#### IV. SMARTSiC PRODUCT ELECTRICAL PERFORMANCE

Combining pSiC substrate and bonding interface contributions, SmartSiC substrate electrical resistivity is monitored thanks to dedicated metrology, already described in ref [3]. Figure 5 highlight the typical I(V) curve measured. It confirms that SmartSiC substrate has a lower resistivity than a conventional bulk. Moreover, total vertical resistivity is improved by a factor 2 to 3 (according to total wafer thickness after device processing) [4].

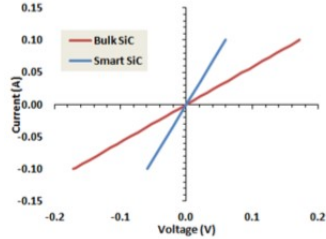


Figure 5: I(V) curves measured on SmartSiC vs mSiC bulk

Such high electrical conductivity is confirmed from room temperature (25°C) to device operating temperature (175°C). Figure 6 confirm resistivity performance is similar on the whole wafer surface. Table 1 compares electrical resistivity on mSiC, pSiC & SmartSiC wafer bonding interface over temperature range.

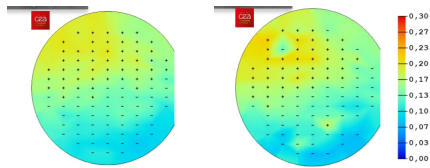


Figure 6: SmartSiC bonding interface electrical resistivity mapping, 25°C (left) and 175°C (right) (a.u)

Temperature	25°C	175°C
4H-mSiC bulk [mOhm.cm]	15 – 25	15 – 25
Bonding Interface [mOhm.cm <sup>2</sup> ]	0.003 – 0.006	0.002 – 0.006
Handle pSiC bulk [mOhm.cm]	1.5 – 2.2	1.7 – 2.5

Table 1: Electrical resistivity for each SmartSiC layer, from 25°C to 175°C

#### I. SMARTSiC QUALITY

SmartCut process, especially bonding and splitting steps may leads to surface defects on SmartSiC substrates. Such defects, also known on conventional SOI materials, are characterized as micro-voids, *i.e.* non transferred area with typical diameter in hundreds of micrometer range. Defect density is currently monitored thanks to Lasertech Sica88, using an inspection recipe adapted regarding specific SmartSiC substrate optical properties. Transferred layer defect density down to 0.1 defect/cm<sup>2</sup> and less has already been achieved, as shown on Figure 7. Future development will consider KLA Tencore SPA2, opening the path to low threshold, down to few hundred nm, surface inspection.[5].

Beyond transferred layer defect, the large zoology of defects intrinsic to the PVT process employed to manufacture SiC boules constitutes a physical barrier to achieve high

manufacturing yields. SmartCut process is known to replicate donor wafer crystal defects. As shown on Figure 8, KOH etching on donor and SmartSiC surfaces allowed to assess that crystalline defects are located at the exact same position on both wafers.

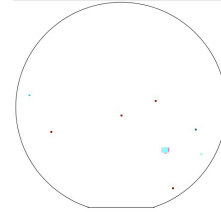


Figure 7 : SmartSiC surface defect mapping, Sica88 measurement

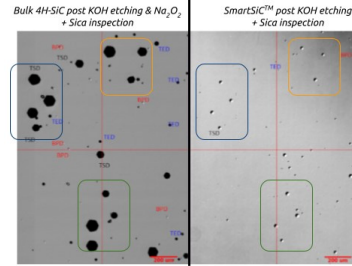


Figure 8: Crystal defect characterization, KOH decoration and Optical Microscope inspection, mSiC donor (left) and SmartSiC (right), site to site comparison

In order to improve the crystal quality of the active layer of a SmartSiC wafer, a specific BPD-free layer is growth on the mSiC donor substrate, then transferred on the pSiC handle. The new engineered substrate is called SmartSiC-Advanced. BPD density values of SmartSiCAdvanced substrates, are shown in Table 2.

Substrate	mSiC	SmartSiC Advanced
BPD density (/cm <sup>2</sup> )	~ 500	< 0.1

Table 2 : BPD defectivity density, mSiC and SmartSiC-Advanced substrate

#### II. CONCLUSION : 200MM PATH OPENING

SmartSiC substrate are prepared thanks to the combination of SmartCut technology associated to high quality mSiC donor and ultra-low electrical resistivity mSiC handle wafers. 150mm prototyping activities have demonstrated targeted performance and 200mm initial samples are now available.



Figure 3 : 150mm & 200mm SmartSiC substrate

#### III. REFERENCES

- [1] T. Kimoto, Jpn. J. Appl. Phys. 54 040103 (2015)
- [2] H. Biard *et al*, ICSCRM Conference, 2022
- [3] S. Rouchier *et al*, ECSCRM Conference, 2021
- [4] E. Guiot *et al*, PCIM Conference, 2022
- [5] E. Cela *et al*, ECSCRM Conference, 2022