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Contactless four-terminal MEMS Variable Capacitor for Capacitive Adiabatic Logic

A Galisultanov¹, Y Perrin¹, H Samaali², H Fanet¹, P Basset² and G Pillonnet¹

¹ Univ. Grenoble Alpes, CEA, LETI, F-38000 Grenoble, France

² Université Paris-Est, ESYCOM, ESIEE Paris, France

ayrat.galisultanov@cea.fr

Abstract. This paper reports the study, design, and simulation of a contactless four-terminal variable capacitor dedicated to capacitive adiabatic logic (CAL) based on silicon MEMS technology. The proposed element consists of the two electrically isolated and mechanically coupled capacitors and is used as a CAL building block. The developed contactless four-terminal comb-drive design is simulated in MEMS+® software. In order to include device model to electrical Spice simulator and speed-up transient simulation of several devices in multiple logic gates context, the received electrical and mechanical characteristics are used to fit a Verilog-A compact model. Spice-simulation results demonstrate CAL functionality, such as logic states differentiation and cascadability. We also figure out the dissipation within this device. For the selected supply voltage, 99.1 % of the energy injected in the device is recycled. The remaining energy is dissipated by mechanical damping. The first part of this dynamic dissipation is adiabatic (scalable with the ramping time), whereas the second one is non-adiabatic (does not depend on the ramping time). This dissipation is due to the loss of electromechanical coupling in the output electrostatic actuator during discharging phase.

1. Introduction

Adiabatic (smooth) switching between logic states is the basis for many approaches to energy saving [1]. In CMOS-based adiabatic logic, the dissipation per logic operation decreases by factor of ten, but still remains a few decades higher than the theoretical Landauer limit for irreversible logic (3 zJ at 300 K). Dissipation per operation in CMOS is limited by a trade-off between the non-adiabatic conduction and leakage loss caused by the internal properties of the FET transistor [2]. Adiabatic operation increases leakage loss contribution and does not affect the non-adiabatic part of the dynamic losses, which is independent of operating frequency.

To suppress the leakage, electromechanical relays have been used in the literature [3]. As they are based on metal-metal contact instead of a semiconductor junction, the leakage becomes almost negligible except in the case of nm-scale electrostatic gap [4]. Unfortunately, the main bottleneck of the relay-based adiabatic logic is the mechanical reliability of the devices, due to electrical and mechanical contact and hysteresis effect [5]. To overcome this limitation, we proposed a new logic family called Capacitive Adiabatic Logic (CAL) [6, 7]. Due to smooth switching process in adiabatic logic, the resistive elements (transistors, relays) in a voltage divider circuit can be replaced by capacitive ones. The gap-closing MEMS variable capacitor could be a good candidate for this purpose. However, a mechanical contact is required in order to have a high capacitance variation. Consequently, this solution suffers from high non-adiabatic loss [8]. On the contrary, the comb-drive MEMS variable capacitor avoids electrical and mechanical contacts [9].

CMOS-based adiabatic logic circuits basically operate with two types of architecture: Bennett clocking and the quasi-adiabatic pipeline [10]. Power supplies called power clocks (PC's) are quite different for these two architectures. In this work, we use the four-phase power clock because Bennett clocking type of architecture requires N different PC's for a N -deep logic chain.

In this paper, we keep the FET transistor notations, i.e. the input voltage is applied between the gate (G) and the ground (GND). These two terminals are isolated from the drain (D) and source (S) terminals, which form an output with a capacitance C_{DS} (cf. Figure 1). There are two possible behaviors of capacitance as a function of the control voltage. The curve $C_{DS}(V_G)$ can have a positive or negative slope. NVC and PVC voltage-controlled capacitors play the same role in CAL as NMOS and PMOS in FET-based logic, respectively. Electrical schematics of a single CAL buffer and inverter circuit are presented in [6].

The basic device of CAL consists of two electrically isolated and mechanically coupled capacitors. The design of the MEMS variable capacitor must be adapted to energy efficient charging and discharging processes. On the other hand, a logic gate, based on this element, must be capable to differentiate "0" and "1" logic states. Furthermore, the logic gate must be able to receive the logic state from the previous gate, process it and transmit the result to the next gate, i.e. to be cascadable.

2. Four-terminal variable capacitance

The built in MEMS+[®] contactless comb-drive model of variable capacitance is presented in Figure 1. This model is a modification of the concept proposed in [9]. The device is made of silicon having a thickness t equal 40 μm , the gap space g between comb-drive fingers is 2 μm , the width of the finger is 2 μm , and the finger pitch is 8 μm . The left comb-drive electrodes correspond to the input, and the right comb-drive electrodes form to the output. The input transducer has an initial overlap about $L_{in} = 15 \mu\text{m}$ between the fixed and the moving electrode. The output transducer is symmetrical and does not have an initial overlap. The gap between the fingers is about 1 μm , and is denoted by L_{gap} . These initial overlap and gap values are selected in order to have appropriate capacitance ratio in the capacitive voltage divider. The interest of this design is that the system becomes insensitive to V_{DS} when there is no overlap between the output comb-drive transducer (V_G is low).

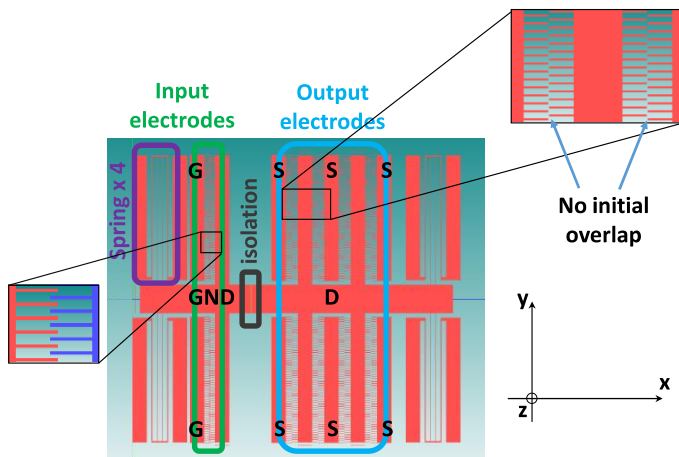


Figure 1. Picture of the contactless 4-terminal MEMS element. Length of the structure is 1.2 mm, width is 1 mm. Two capacitors are electrically isolated and mechanically connected by a 2 μm SO_2 isolation layer.

Number of input fingers N_{in} is 110,
number of output fingers N_{out} is 220,
mass $m = 4.41 \cdot 10^{-8} \text{ kg}$,
spring constant $k = 2.39 \text{ N/m}$,
resonant frequency $f_{res} = 1173 \text{ Hz}$,
damping coefficient $b = 1.16 \cdot 10^{-5} \text{ kg/s}$,
quality factor $Q = 28$.

2.1. MEMS+[®] results

The mechanical parameters extracted from MEMS+[®] simulation results are presented in the captions to Figure 1. The displacement and the capacitance-voltage (CV) curves are shown in Figure 2. In this design, low and high input signals can be distinguished by the moving mass displacement. If the input voltage is lower than 10V, there is no overlap in the output transducer and, consequently, the voltage V_{DS} does not affect the position nor the capacitance ratio. Otherwise, the overlap appears in the left part of the output (cf. upper left part of Figure 1). After that, an increase of V_{DS} affects the moving mass position x , and changes the capacitance ratio in the voltage divider circuit.

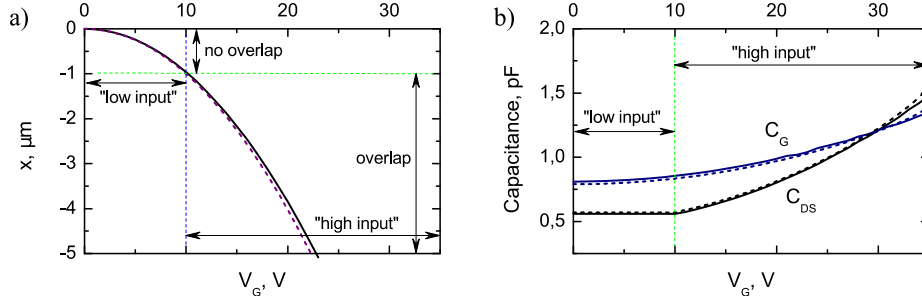


Figure 2. a) Moving mass displacement as a function of the input voltage V_G . b) Input C_G and output C_{DS} capacitances as a function of the input voltage V_G . Verilog-A model and MEMS+® simulation results are drawn as solid and dashed lines, respectively.

2.2. Verilog-A model

In order to include the MEMS device model in the electrical simulator and to speed-up the transient simulation of cascaded gates, the received CV and mechanical characteristics are used to fit a Verilog-A compact model. This system has two electrical ports and one mechanical port. The developed model includes both electrical and mechanical parts of the system. The electrical part consists of four electrical terminals described above (G, GND, D, S). The mechanical part is a simple mass-spring-damper system and can be described by the following equation of motion:

$$m\ddot{x} = -b\dot{x} - kx + F_{eG} + F_{eDS}, \quad (1)$$

where input F_{eG} and output F_{eDS} electrostatic attractive forces are calculated from:

$$F_{eG} = \begin{cases} -\alpha_1 V_G^2 N_{in} \epsilon_0 t / g, & \text{if } x \leq L_{in} \\ 0, & \text{if } x > L_{in} \end{cases}, \quad (2)$$

$$F_{eDS} = \begin{cases} -\alpha_2 V_{DS}^2 N_{out} \epsilon_0 t / g, & \text{if } x \leq -L_{gap} \\ 0, & \text{if } |x| < L_{gap} \\ \alpha_2 V_{DS}^2 N_{out} \epsilon_0 t / g, & \text{if } x \geq L_{gap} \end{cases}. \quad (3)$$

Where $\alpha_1 = 1.18$ and $\alpha_2 = 1.09$ are the fitting parameters extracted from MEMS+® results, and $\epsilon_0 = 8.854 \cdot 10^{-12}$ F/m is the vacuum permittivity. According to Equation 4 [11], the charging and discharging current through the MEMS variable capacitor is a sum of two components. The first one is the familiar capacitive current. The second one is the motional current, which describes the transfer of energy from the electrical to the mechanical domain and vice versa.

$$i(t) = C(x) \frac{dV(t)}{dt} + \frac{dC(x)}{dx} V \frac{dx}{dt} \quad (4)$$

The input C_G and output C_{DS} capacitances are calculated from:

$$C_G = \begin{cases} C_{Gp} + 2\alpha_1 N_{in} \epsilon_0 t (L_{in} - x) / g, & \text{if } x \leq L_{in} \\ C_{Gp}, & \text{if } x > L_{in} \end{cases}, \quad (5)$$

$$C_{DS} = \begin{cases} C_{DSp} + 2\alpha_2 N_{out} \epsilon_0 t (L_{out} - x) / g, & \text{if } x \leq -L_{gap} \\ C_{DSp}, & \text{if } |x| < L_{gap} \\ C_{DSp} + 2\alpha_2 N_{out} \epsilon_0 t (L_{out} + x) / g, & \text{if } x \geq L_{gap} \end{cases}. \quad (6)$$

The input C_{Gp} and output C_{DSp} parasitic capacitances are extracted from MEMS+® simulations and equal 0.12 and 0.56 pF, respectively. The C_G definition (5) is not entirely accurate in the region without overlap ($x \geq L_{in}$). However, this displacement range is out of operation regime. Consequently, this assumption does not affect the accuracy of the model. The comparison between Verilog-A model and MEMS+® simulations is presented in Figure 2. The models are in good agreement.

2.3. Energy analysis in the four-terminal device

In order to study the dynamical behaviour of the four-terminal variable capacitor, we performed transient electromechanical simulation of the circuit depicted in the inset graph in Figure 3. Only the case of maximal displacement ($|x_{max}| > L_{gap}$) is discussed. During the simulation, all energy components are calculated and the conservation of energy is checked. The selected energy components during charging and discharging process are presented in Figure 3. According to Equation 4, a part of the electrical energy is converted into mechanical energy during the charging process of C_G and C_{DS} capacitances. During the discharge, most of the mechanical spring energy stored in the system is recovered in the PC's. The energy losses in the reversible PC's are out of the scope of this paper. The difference between provided and recovered energy is determined by damping and resistive losses. However, mechanical loss dominates here, as the mechanical time constant is six orders of magnitudes higher than the electrical one (the mechanical period equals $1/f_{res} = 0.85$ ms, the electrical time constant equals $RC_{DSmax} \approx 1.5$ ns). The ratio between the recycled energy and the maximal energy provided by PC's (685 pJ) is 99.8 %. The presence of non-adiabatic dissipation is determined. The non-adiabatic dissipation is caused by the loss of electromechanical coupling in the output electrostatic actuator during discharging phase of the output capacitance C_{DS} (cf. Figure 3). The coupling disappears when $|x_{max}| = L_{gap}$, and, consequently, the system loses the stored mechanical energy:

$$E_{non-adia} = kL_{gap}^2 / 2 . \quad (7)$$

The minimal dissipated energy during one cycle is 1.2 pJ, when the ramping time $T \rightarrow \infty$. The Spice simulation allows us to verify that the proposed model is energy consistent and can be used for further CAL gates development.

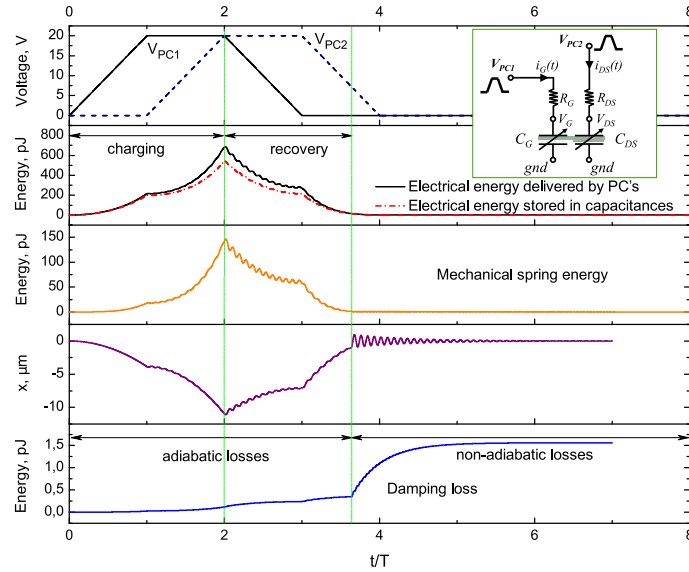


Figure 3. Power supply voltages, energy components and displacement over time. The 4-terminal test circuit is presented in the inset in the graph ($T = 10$ ms, $R_G = R_{DS} = 1$ k Ω , $V_{PCmax} = 20$ V).

3. Cascadability

The cascability of the proposed 4-terminal device is demonstrated using an array of buffer elements. The buffer chain circuit is presented in Figure 4a. The binary input logic word "1010" is transferred through four buffers, as demonstrated in Figure 4b. The input voltage amplitude is 8 V and 12 V for "low" and "high" input levels, respectively. The logic state in further gates is coded by the moving mass displacement x , induced by the input voltage. If the displacement is less than $L_{gap} = 1$ μ m, there is no overlap and, consequently, the output capacitance C_{DS} is not affected by the voltage V_{DS} due to output symmetry. It causes "low" signal in the next gate. On the contrary, if the input is "high", the displacement x is higher than 1 μ m ($V_{IN} > 10$ V). Consequently, the rise of the output voltage is able to trigger a displacement of the moving mass, transferring "high" signal to the next gate of the chain of

buffers. The holding phase is activated by the electrostatic force F_{eDS} and no additional complementary NVC is needed unlike to CMOS circuits. This effect is shown in third graph of Figure 4b. The energy recycling ratio equals 99.1 % for selected voltage levels. The "0" and "1" states can be distinguished, even if the voltage difference between them is not very high. The system demonstrates cascability for V_{PCmax} amplitude ranging from 22 to 25 V.

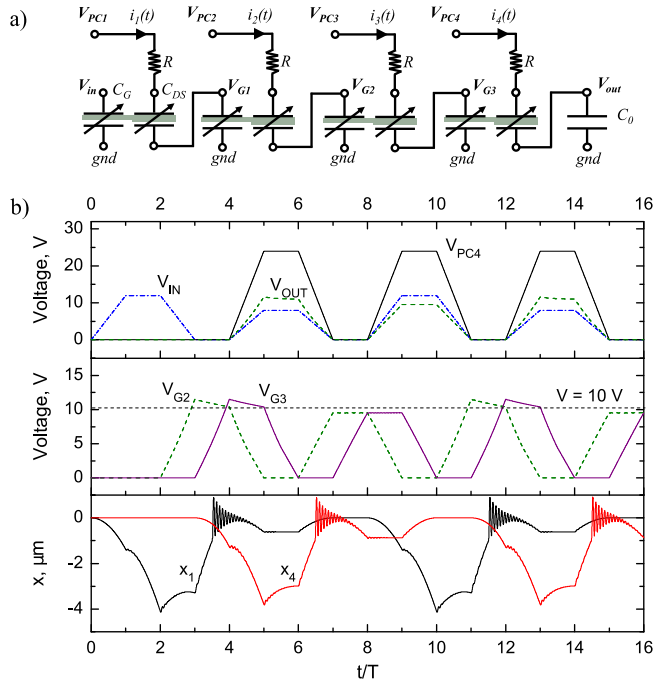


Figure 4. a) Electrical diagram of the cascade of four buffers. b) Spice simulation results: input voltage V_{IN} , V_{PC1} , output of the first buffer V_{OUT} (first graph), V_{IN} , output of the fourth buffer V_{OUT} (second graph) over time.

We used the following parameters:

$T = 10$ ms (the selected ramping time T is higher than mechanical relaxation time $Q/(\pi f) = 7.6$ ms in order to have sufficient time for the relaxation of non-adiabatic oscillations),

$R = 1$ k Ω ,

$V_{PCmax} = 24$ V,

$C_0 = 0.86$ pF.

4. Conclusion

The developed contactless design of a variable MEMS capacitor as a building block of CAL has been successfully tested and verified. Our design avoids leakage losses, in advantage to CMOS-based adiabatic logic and resolves reliability problem of nanorelay solution. An analytical compact model of the electrostatically-actuated variable capacitor has been developed. The analysis of all loss mechanisms have been done for a single device and for a cascade of four buffers. The binary input logic word "1010" is successfully transferred through a chain of four buffers. The ratio of recycled energy equals 99.1 % for chosen operating voltage. The presence of non-adiabatic dissipation in the mechanical part has been demonstrated for the presented MEMS device. For this mm-scale device the energy dissipated during one cycle is in the order of one pJ per operation. This is still far from the energy dissipated by a nm-scale FET transistor, which is in the order of one fF. However, scalability is possible and the energy dissipation for the contactless design is scaled in the cube of the size [9].

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