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In Memory Energy Application for Resistive Random Access Memory

Paola Trotti,* Sami Oukassi, Gabriel Molas,* Mathieu Bernard, François Aussenac, and Gaël Pillonnet

This work explores the innovative concept of a hybrid dual-behavior device, based on emerging nonvolatile memory technology, for both data retention and energy storage. RRAM (resistive random access memory) is considered a major candidate as next-generation memory, thanks to its promising performances in terms of scalability and CMOS process compatibility. Its working mechanisms, based on faradaic processes, motivate the study on the feasibility of operating RRAM also as energy storage element. To evaluate the energy capability, various electrochemical characterizations on state-of-the-art RRAM are presented. The highly resistive electrolyte, extremely small physical scale (nm), and current range (pA), put in quite a critical framework, far from conventional solid-state batteries. Cyclic voltammetry tests reveal that although no oxidation peak appears during the redox cycle, the cells behave as standard electrochemical storage elements when investigating the impact of the scan rate, maximum positive voltage, and area on the reduction peak. Concentration and diffusion coefficients are derived, in the order of $10^{-12} \text{ cm}^2 \text{ s}^{-1}$ and few mmol cm^{-3} , respectively, while energy storage capability amounts to $3.5 \text{ pJ } \mu\text{m}^{-2}$. Finally, design concepts are proposed, where RRAM “in-memory energy” technology would be a newfangled approach to meet the needs of various emerging and standard applications.

1. Introduction

Recent advances in fields like artificial intelligence (AI), the internet of things (IoT), virtual reality, and cloud computing have been demanding ever-increasing computational capability. Power-efficient calculation is key in any task implemented on a chip, from high-performance core computing to the edge of IoT. While process miniaturization managed to effectively reduce consumptions in the past, its effectiveness has been dropping for recent technological nodes, the overall balance in power cost coming majorly from losses over transmission lines. As a result, further downscaling is expected to soon no longer pay off the development investment, and alternative strategies

must be considered. This branch of research involves the so-called Moore than More's devices.^[1] Some attempts to ease consumption rely on on-chip integration of nanoscale energy sources,^[2,3] while others, notably in memory computing (IMU),^[4] offer a revisited architecture where computation is decentralized. Other research groups proposed the integration of energy sources in close proximity of the memory,^[5,6] or completely integrated within the memory architecture.^[7]

In this work, we explore a radically different concept, which lies on “dual-behavior” devices, able to store either information or energy, depending on the applied bias. Such capability would be greatly beneficial, allowing localized and high bandwidth energy supply to the processing unit (the memory or a dedicated arithmetic logic unit, ALU). The samples considered in our study indeed resemble ionic batteries at the nanoscale, providing ground to our inquiry of using these devices as energy sources, other than memory cells. Their operation

relies on faradaic processes; therefore, the resulting energy density is expected to well exceed that of electrostatic capacitors, possibly being comparable to supercapacitors.^[8] The diameter of the devices under study can range between 1 and $100 \mu\text{m}$, resulting in much smaller than the diameter of state-of-the-art planar supercapacitors ($\approx \text{mm}^2$),^[2] making such architecture more scalable and granular than any other state-of-the-art integrated power source. Energy storage is achievable when the device is, under a memory point of view, storing a logic 0, and could be accumulated during low logic operation activity for later use, for example, during the most power-hungry phases. These devices would also offer the advantage of placing the battery cell in close proximity to the target, meaning reduced IR drop and voltage undershoot, which develop in a typical inductive-impedance power delivery network (PDN).^[9] A broad range of applications could be envisioned, each demanding different energy requirements, with widespread specifications. The most suitable target field should be selected taking into account the output voltage, energy, and power delivered by such RRAM-based batteries. In this work, we provide an outlook on some possible implementations, with some quantified ranges in terms of energy and instantaneous power requirements. **Figure 1** reports the three main eligible domains: energy to memory,^[10] energy to logic,^[11] and neuromorphic computing.^[12–15]

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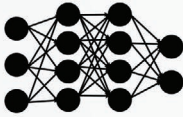
	Required Energy [pJ]	Operating Voltage [V]	Instantaneous Power [uW]	
	NAND FLASH	0.01	~20	
	NOR FLASH	100	~5	
	PCM	100	3-5	
	RRAM	1-10	2-5	
	STTRAM	0.1	1-3	
	(switching energy per cell)			
	IoT processor:			
	ARM Cortex-M0	3 - 6.4	0.4-0.7	0.64 - 240
	ARM Cortex-M0+ MSP430 compatible	1.1 - 11.7	0.19-1.2	0.4 - 735
	ARM Cortex-M3	7	0.32-0.48	56 - 497
		23	0.5-1	23 - 460
	(minimum energy per operation)			
	Synaptic technology:			
	SRAM-based [12]	27	28 nm-compatible	63 k
	SRAM-based [13]	105	14 nm-compatible	-
	RRAM-based [14]	N/A	40 nm-compatible	9.9 k
	RRAM-based [14]	N/A	180 nm-compatible	15.8 k
	RRAM-based [15]	180	130 nm-compatible	1.5 k
	(Energy per synaptic event)			

Figure 1. List of required energy, operating voltage and instantaneous power for various applications.

2. In-Memory Energy Storage Concept

RRAM is a popular emerging memory technology that relies on (a wide range of) materials, which are able, under appropriate bias, to switch their resistance value between high and low. Different resistances are associated with different logic states, namely a low resistive state (LRS) and a high resistive state (HRS). States are nonvolatile, meaning that once a resistance transition happens, the bias can be removed without occurring into the degradation of the information stored. Known as the filamentary switching effect, the phenomenon behind RRAM operation consists in the deposition and dissolution of a thin metallic filament between the device's access electrodes.^[16–18] A schematic illustration of the memory effect is reported in Figure 2. Some major advantages of RRAM technology are:

- I. high scalability (typical cell areas are $\approx 100 \text{ nm}^2$);^[19]
- II. low operating energy (down to 10 pJ per bit);^[16]
- III. fast switching speed (in the order of $\approx \text{ns}$);^[20]
- IV. high retention of the stored logic state;^[21]
- V. high cycling capability ($> 10^6$ cycles);^[22]
- VI. a common BEOL cell structure (metal–insulator–metal stack);^[23]
- VII. Compatibility with CMOS technology, by materials and fabrication process.^[24]

A typical RRAM cell is structured as a metal–insulator–metal (MIM) stack, whose middle layer is an electrical insulator that is relatively ion conductive, enclosed between an electrochemically active and inert material. The resulting configuration is an electrode–electrolyte–electrode system, in fact resembling a classical

ionic battery.^[8] Measurements of electro-magnetic-field (EMF) in RRAM have been reported in the literature,^[25,26] and an interplay of Nernst, diffusion, and Gibbs-Thompson potentials have been suggested as underlying causes.^[25] RRAM-based batteries would present the advantage of being highly scalable and dynamically allocable, which translates into the possibility of placing energy sources right next to memory blocks, supplying energy for the writing of logic states. Therefore, less power waste over transmission lines and high PDN efficiency could be achieved. An extended concept of in-memory-computing-and-energy, performed through RRAM devices, thus holds great potential.

Our farsighted concept of a memory-battery dual-behavior device is presented in Figure 2: the elements are arranged in a crossbar array^[27,28] to maximize integration density. In the envisioned design, subarrays could be dynamically assigned to perform as either memory or battery, depending on real-time needs. In a practical implementation, each element of the array shown in Figure 2 comprises a RRAM cell in series with a selection device, like a transistor or a selector in order to avoid leakage and disturbance between cells.^[16] When operated in battery mode, the charging operation follows a similar procedure to the writing of a memory cell (better details given in Section 4), while the discharging should be operated by some dedicated control circuitry. This block might be able to address multiple cells in parallel, possibly adjusting the number of selected elements in accordance with the demanded energy, in order for them to supply the energy to the load. Section S2 (Supporting Information) illustrates a system-level design for a hybrid dual-behavior crossbar-based device.

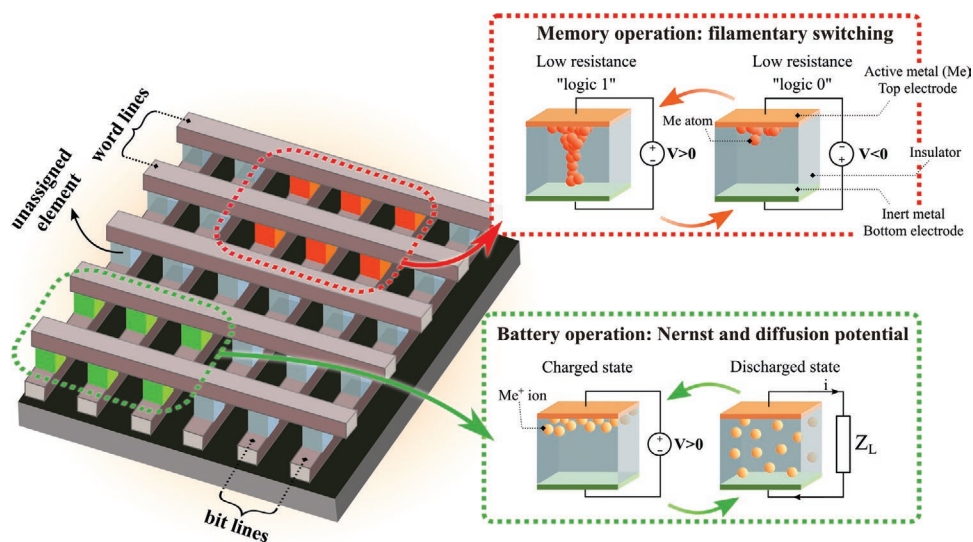


Figure 2. Innovative concept of a hybrid dual-behavior RRAM device. In the envisioned implementation, elements are placed at the intersection of word and bit lines, in a crossbar array configuration, which allows maximizing energy and memory density. In red and green, respectively, cells storing logic values and energy.

2.1. Operating Principle of RRAMS

Figure 3 reports a typical RRAM I - V curve, obtained by reading the current flowing between the cell's electrodes while sweeping the voltage across them (quasi-static operation). The device initially is in HRS (typically in a range [10^7 - 10^{11} Ω]^[29,30]), so that at point (1), the current approaches 0. Towards (2), the increasing voltage gradually enhances the oxidation of the top electrode, which releases metal cations (Me^{z+}) inside the electrolyte, in parallel reducing some Me^{z+} ions at the electrolyte/bottom electrode interface, according to the general reaction:



Atom by atom, the filament piles up. The gap between the filament tip and the top electrode grows smaller and enhances electron tunneling, boosting conduction until the filament is fully formed (3).^[17,18] At the set voltage, V_{SET} , the cell completes its transition to a low resistance state, and toggles its logic value to a logic 1. Once the current hits $I_{\text{SAT,WRITE}}$, typically around 100 μA ,^[31] the current-limiting element in series with the memory prevents further increase, in order to avoid cell damage. As a result, the current is held at the compliance value $I_{\text{SAT,WRITE}}$. The first high to low resistance transition a device experience is called forming process, and usually occurs at a higher voltage (called "forming voltage") with respect to subsequent HRS to LRS switchings, called set events, or set processes. After the cell reaches the LRS, the sweeping direction is reversed. The filament continues to bridge the electrodes until point (4), when the reactions of Expression 1 are reversed: oxidation of Me to Me^{z+} takes place at the bottom electrode/electrolyte, while reduction of Me^{z+} to Me occurs at the electrolyte/top electrode interface. The filament is disrupted at the reset voltage, V_{RESET} , at which the cell's resistance switches back to a high value.

The inset of Figure 3 shows a zoomed view of the highlighted area, with electrochemical currents in evidence, associated with the redox peaks of the reactions happening at the electrode interfaces. A non-zero voltage might be measured across the cell as a result of the ongoing reactions and ion gradients development. Valov et al. have reported measurements of open-circuit voltage across RRAM while the cell is in HRS.^[25] They motivated their findings with the arise of Nernst, Diffusion, and Gibbs-Thomson potentials between the electrodes of the devices under study.^[25] A diffusion potential resulted from a non-null gradient of charge inside the electrolyte, introduced by the release of redox ion products. Such potential can thus be externally controlled, following the activation of bias-triggered electrochemical reactions. Below the activation energy, reactions cannot continue, and ions

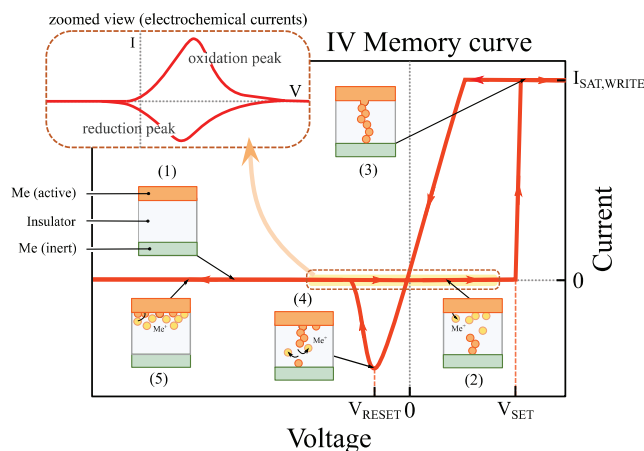


Figure 3. A typical I - V curve of a RRAM. The memory is, initially (1), in a logic "0" state (highly resistive), and switches to a logic "1" in (3), when the filament bridges the electrodes. The memory goes back to "0" in (4), when the filament dissolves. In the inset, a zoomed view showing the electrochemical currents (redox peaks).

spontaneously diffuse back to a homogeneous concentration over time, gradually nulling the voltage drop. A corresponding “re-equilibrium” current can be detected. Valov’s group reported discharging short-circuit currents, when externally grounding the electrodes after having triggered redox reactions.^[25] Although their research lies in a theoretical domain, meant to deepen the filamentary switching understanding, their findings inspired our study on the feasibility of a practical implementation of the nanobattery effect in RRAMs.

3. Experimental Section

RRAM device-under-test (DUT) stack is: CuTe₂Ge/Ta₂O₅/W.^[32–36] The samples were fabricated on 8 in. wafers, in 1R cell configuration.^[16] Three different Ta₂O₅ thickness (5, 10, and 15 nm) were produced and tested. **Figure 4** is reported a TEM picture with ESD elemental mapping. “Plug-shaped” bottom electrodes (W) were first deposited. Consecutively, the Ta₂O₅ layer was RF sputtered, adjusting the sputtering time according to the targeted thickness. The density of the Ta₂O₅ layer resulted approximately equal to 7 g cm⁻³. A 30 nm thick CuTe₂Ge alloy was deposited as the top electrode, and successively capped by a Ti/TiN layer. Seven different areas were produced (0.07 to 2.27 μm²) by adjusting the bottom electrode diameter, in a range from 0.3 to 1.7 μm, with a step of 0.2 μm. Wafer testing was performed on a Cascade microprobe station, implementing triaxial Kelvin-connected SMUs, controlled by Parameter Analyzer HP4155.

Fresh (i.e., unformed) devices have been characterized through the setup shown in **Figure 5a**, which allows investigating both memory (in quasi-static testing regime) and battery operation. In the latter case, the voltage drop across the device has to be limited below the forming value. Battery behavior was tested through cyclic voltammetry (CV), in two-electrode configuration. A linear voltage ramp biasing the access contacts was applied while reading the current flowing through the stack. In the voltage range and sweeping speed (≈1 V s⁻¹) considered for the CV tests, negligible electron

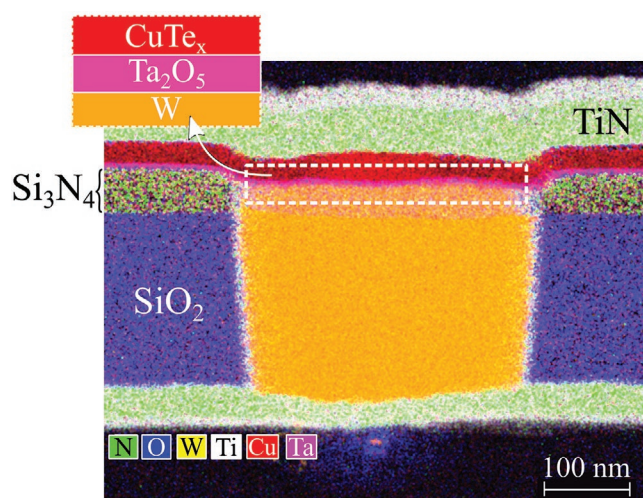


Figure 4. TEM with ESD elemental mapping picture of the sample structure.

tunneling and capacitive contributions arise, thus the measured current was assumed to be deriving mainly from electron exchange through redox reactions.

4. Results and Discussion

Memory operation was first validated; **Figure 5b** reports typical characteristics for a 5 nm sample: forming, set and reset curves are shown. Further memory characterization is reported in Section S1 (Supporting Information). Next, we proceeded to investigate the electrochemical behavior, the maximum value of the sweeping voltage, V_{end} , being limited below the forming value, which was found to remarkably increase with the thickness of the Ta₂O₅ layer: a mean of 3 V for 5 nm, 5 V for 10 nm, and >15 V for 15 nm. Results of CV tests are presented in Section 4.1, while mathematical extrapolation of diffusion and concentration coefficients is reported in Section 4.2.

4.1. Cyclic Voltammetry Results

A typical CV curve, for a 5 nm thick Ta₂O₅ sample, is shown in **Figure 5c**. A clear current peak can be observed when sweeping through V_b 's falling ramp, at approximately 200 mV. We associate such a peak to a reduction reaction of copper cations at the CuTe₂Ge/Ta₂O₅ top electrode/electrolyte interface.

Given the absence of a reference electrode, it is nontrivial to assign a specific reaction to the current peak. Aqueous solution potentials suggest that the reduction of Cu⁺ ions to Cu is the most energetically favorable.^[37] Although our (solid) electrolyte is far from an aqueous solution, some research groups hypostatized that water molecule might be incorporated inside nanopores of Ta₂O₅ due to ambient humidity,^[26] therefore aqueous potentials might still hold true. Applying this assumption to our samples, during the positive voltage scan the reaction taking place at the CuTe₂Ge/Ta₂O₅ interface could be assigned to:



Sustained by the counter-reaction:^[26,38]



At the Ta₂O₅/W interface: The reaction expressed by Expression 3 might be responsible for Cu⁺ generation when no prior copper cation is present, and afterward concurs with the reduction on Cu⁺ at the Ta₂O₅/W interface:



Upon negative voltage scan rate, the oxidation in Expression 2 would take place at the Ta₂O₅/W interface, while Expression 4, which we associate with the reduction peak observed in **Figure 5c**, occurs at the CuTe₂Ge/Ta₂O₅. It can be observed in **Figure 5c,d** that no oxidation peak appears when sweeping to positive voltages. This result agrees with what was reported in the literature for high-density Ta₂O₅ samples, where it was found that the oxide density trades with electrochemical

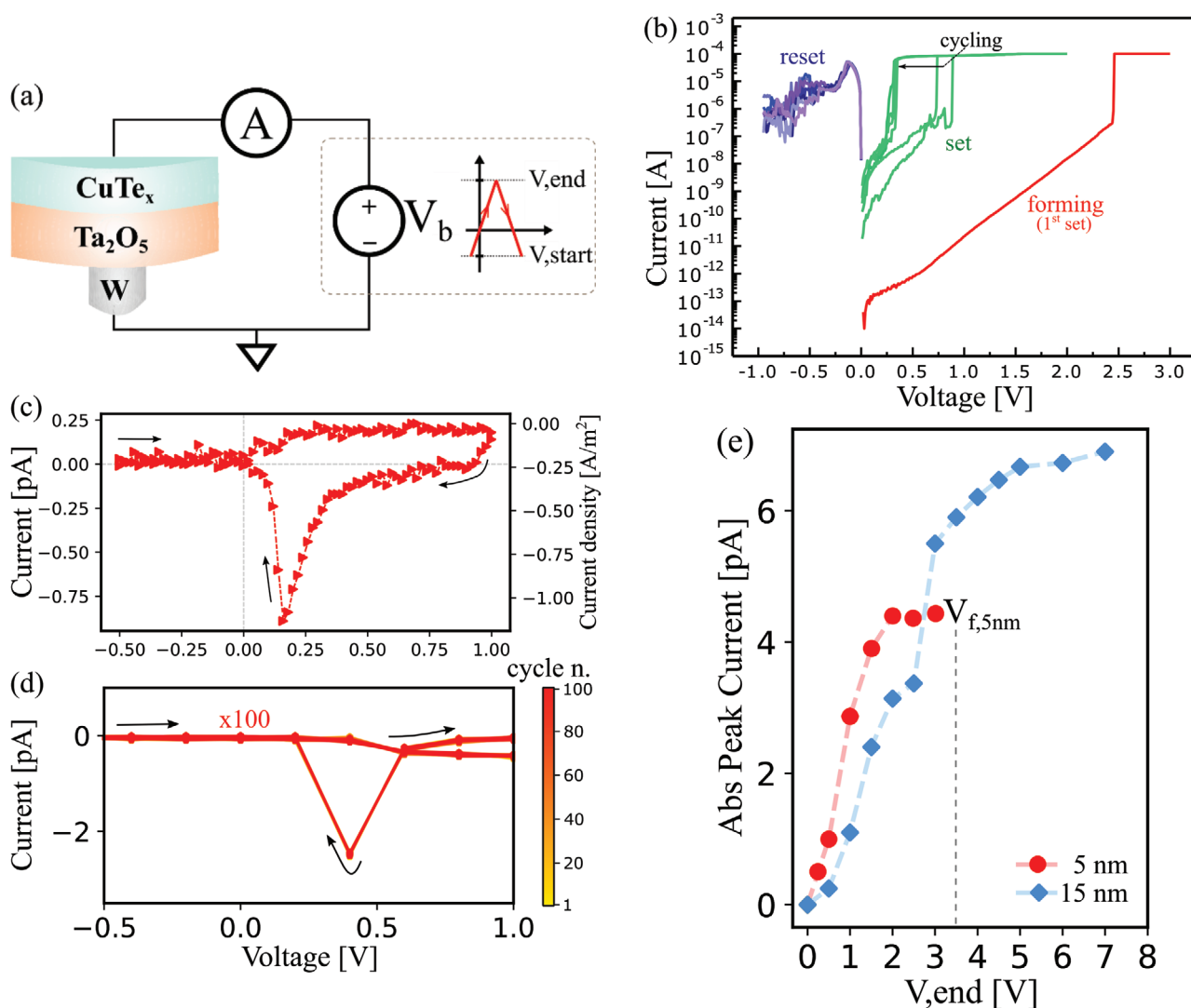


Figure 5. Cyclic voltammetry results. a) The test setup. In b) forming, set and reset curves for a 5 nm thick Ta_2O_5 sample. c) A typical voltammogram, featuring a clear current peak during the negative scan rate. In d) At lower resolution, the peak of a 10 nm thick Ta_2O_5 device over 100 cycles, the curves perfectly overimposing on each other. In e) the current peak amplitude (absolute value) versus V_{end} . Different slopes can be observed for different thicknesses, while a saturation trend for increasing values of V_{end} bends the curves for both cases.

currents, and no oxidation peak was observed above 71 g cm^{-3} ,^[26] a value that closely approaches that of our samples. Figure 5d reports 100 overlaid CV cycles for a 10 nm thick sample. The peaks appear less detailed with comparison to Figure 5a, as a lower resolution was used to speed test times. The curves perfectly overlap with one another, no remarkable change in shape is appreciable over cycling. Figure 5e reports various current peak amplitudes, each obtained by sweeping V_{end} in a range from 0 to 2 V, while keeping V_{start} fixed at -2 V . Each curve represents a different oxide thickness sample: namely 5 and 15 nm. The maximum V_{end} value is limited to 3.5 V for the 5 nm sample, as the device was formed at 4 V. For either case, the peak current at $V_{\text{end}} = 0$ was null (approaching the noise level). This result can be motivated with the lack of copper cations to reduce when no sweeping to positive voltages takes place beforehand. For $V_{\text{end}} > 0$, the relationship between voltage and current is initially ($V_{\text{end},5 \text{ nm}} < 2$, $V_{\text{end},15 \text{ nm}} < 3$) close

to linear, with the 5 nm thick case exhibiting a higher slope. For greater voltages, however, the current saturates in both cases. Our interpretation is that the cation content can effectively be increased by heightening V_{end} until some threshold value, beyond which the saturation trend sets in, possibly as a consequence of having reached the maximum solubility of copper ions inside the Ta_2O_5 electrolyte. Our results thus support the fact that, although no oxidation peak is detected during positive scan rates, some oxidation processes must be taking place nonetheless, providing copper cations which are later reduced when the scan polarity is reversed.

To further investigate the nature of current peaks in our DUT, we performed CVs at various scan rates, ranging from 160 mV s^{-1} to 5 V s^{-1} . Figure 6a shows an overlap of six curves, each obtained at a different scan rate. It can be observed that, increasing the sweep speed, the current peak amplitude increases and the voltage at which the peak is obtained drifts

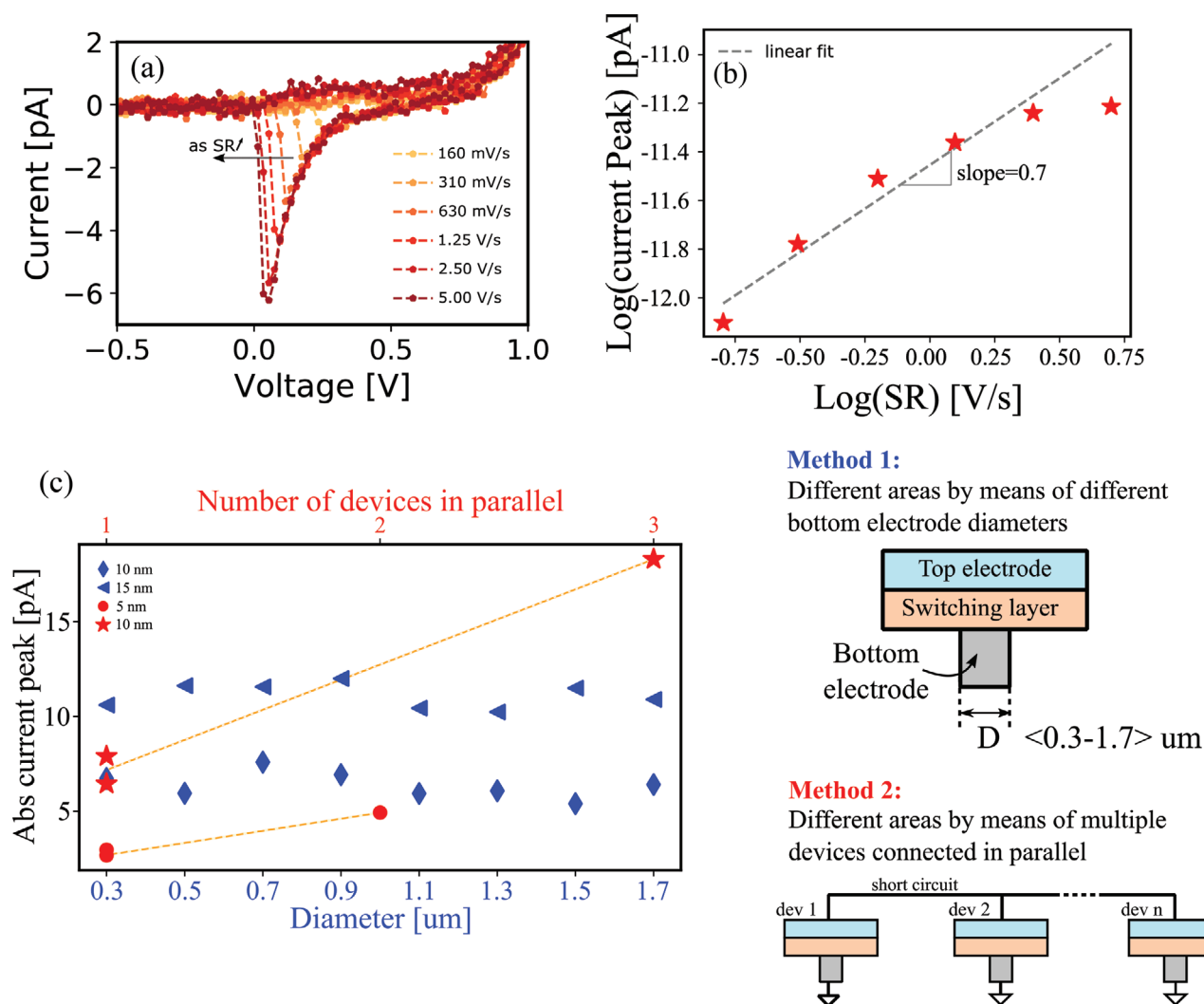


Figure 6. Impact of scan rate and area. a) In different colors, CV curves at various sweep rates, ranging from 160 mV s⁻¹ to 5 V s⁻¹. b) The amplitude of the current peak versus the scan rate. c) Trend of peak current versus area, increased either by means of a larger bottom electrode diameter (Method 1, in blue) or by multiple devices connected in parallel (Method 2, in red).

to more negative values. The shift in peak position is typical of irreversible processes, with which we identified our reactions. The Randles-Sevcik equation for irreversible processes declines as:^[39]

$$I_p = 0.4958(Fn)^{3/2}(RT)^{-1/2}Ac_0(\alpha Dv)^{1/2} \quad (5)$$

where I_p is the peak current, F is the Faraday constant, n is the number of electrons involved in the reaction, R is the gas constant, T is the absolute temperature, A is the electrode area, c_0 the concentration coefficient, α is the transfer coefficient, D is the diffusion coefficient and v is the scan rate. Equation 5 dictates a linear trend between the peak current and the scan rate. Figure 5b shows a log-log plot of current peak amplitudes versus the scan rate, along with a linear fit showing a slope equal to 0.7. Equation 5 predicts a slope of 0.5 for faradaic processes, so we associate the measured currents as mainly deriving from redox reactions. We point out that capacitive

currents should approach a slope equal to 1, and feature a box-shape behavior over the whole voltage range, which appears far from our reported case, as shown in Figure 5a. The trend of the current to the scan rate appears to deviate from linear when the voltage sweep is fastened. The bend of the curve might be explained through relatively low reaction kinetics, which cannot keep up to the pace when the potential is rapidly changing. Equation 5 also expresses a linear area-peak current relationship. We measured the trend for our samples by comparing CVs, in the same testing conditions, obtained from devices with different areas (Figure 6c, method 1). As shown in Figure 6c, we did not observe a peak current variation when testing different area samples. However, we were able to measure a linear area-peak current trend when physically connecting either two or three devices in parallel (Figure 6c, method 2). Our interpretation is that the ongoing electrochemical reactions are possibly limited to a restricted portion of the device electrolyte, in a similar manner to the resistive switching effect.^[40,41]

4.2. Diffusion and Concentration Coefficient Extrapolation

Further investigation was carried out by deriving the diffusion and concentration coefficients characterizing the reactions taking place in our samples. The recombining charge during the reduction process was first calculated by discrete time-integration of the current during the negative voltage scan:

$$Q_{\text{Cu}^+} = \partial t \left| \sum_{n=0}^N i_n \right| \quad (6)$$

where ∂t is the time interval between each sample, i_n the n th value of the current and N the number of samples collected. In order to exclude tunneling contributions, only samples in the interval [-0.2, 0.6] V were considered. We then derived the injected moles with Faraday law:

$$N_{\text{Cu}^+} = \frac{Q_{\text{Cu}^+}}{n F} \quad (7)$$

where n is the oxidation number (assumed equal to 1) and F the Faraday constant. The concentration coefficient, for our sample's cylindrical geometry, can be expressed as:

$$c_{\text{Cu}^+} = \frac{N_{\text{Cu}^+}}{V_{\text{Ta}_2\text{O}_5}} = \frac{N_{\text{Cu}^+}}{t_{\text{GeS}_2} \left(\pi \frac{d^2}{2} \right)} \quad (8)$$

where $V_{\text{Ta}_2\text{O}_5}$ is the volume of the electrolyte where the copper cations are dissolved, and d is the diameter of the bottom electrode. **Figure 7a** reports the concentration coefficient versus the scan rate: c_{Cu^+} reasonably drops with increasing v , in accordance with Equation 5, as less time is available for reactions to

generate products when the potential is swept faster. Finally, diffusion coefficients were extrapolated using Equation (5):

$$D = \frac{RT}{\alpha v (Fn)^3} \left(\frac{I_{pk}}{0.4958 A c_{\text{Cu}^+}} \right)^2 \quad (9)$$

where α has been taken equal to 0.5.^[26] Results, at different scan rates, are plotted in Figure 7b, while Figure 7c shows D versus c_{Cu^+} . It can be seen that the trend of D with v is opposite to that of the concentration coefficients, as diffusivity increases when less c_{Cu^+} ions are present. Our trends are in agreement with reports from the literature for a similar RRAM stack.^[26,42] The energy storage capability was evaluated through:

$$E_{\text{SR},i} = \partial t \left| \sum_{n=0}^N i_n V_n \right| = \partial t P \quad (10)$$

where V_n are the values of the voltage at which the current was sampled, and i_n the corresponding current samples, during the negative scan. P is the released power. Figure 7d reports estimated energy and power densities versus the scan rate. It can be seen that the energy density is decreasing when the scan rate is higher, as a result of having less available ions.

5. Summary and Perspectives

The characterization of RRAM in-memory energy devices conducted in this work allows us to draw some preliminary considerations:

1. The proposed technology allows to operate a device simultaneously both as memory and energy storage

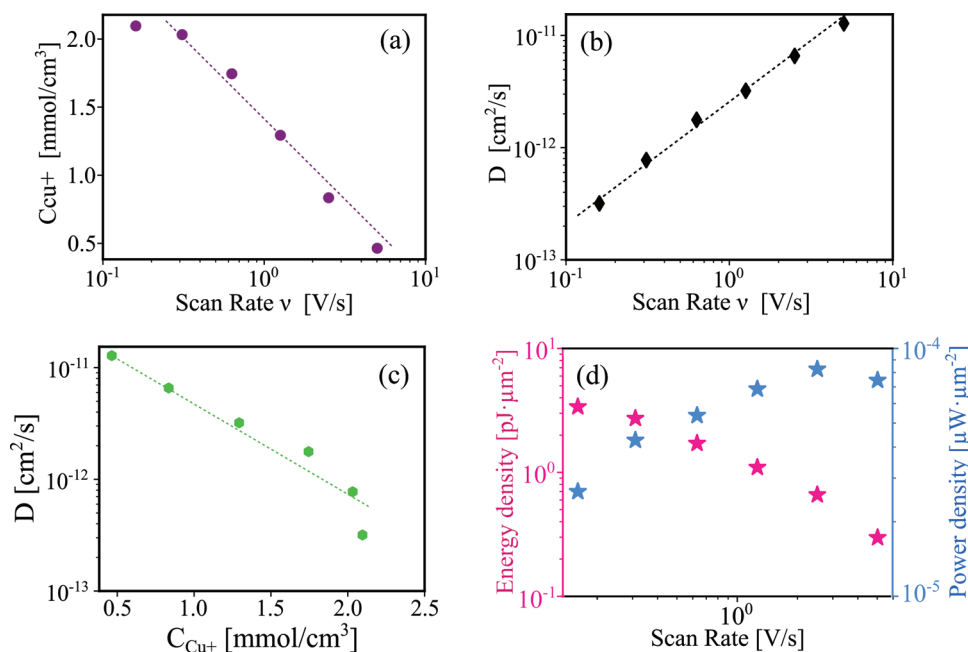


Figure 7. Electrochemical parameters. a) The concentration and b) The diffusion coefficients, versus the scan rate. In c), the diffusion coefficient versus the concentration coefficient. (d) Energy (in pink) and power density (in blue), versus the scan rate.

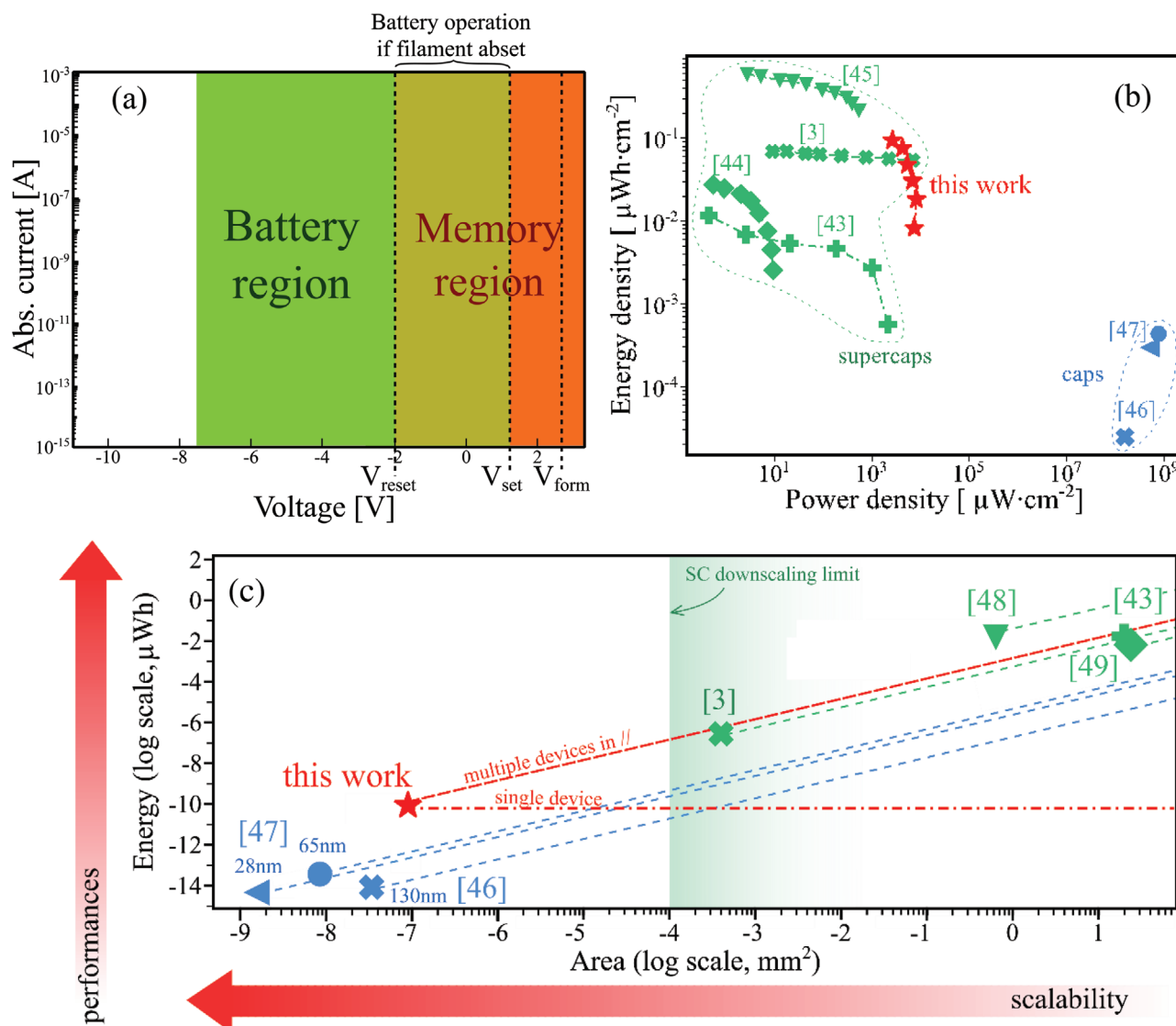


Figure 8. Specifications of RRAM-based in-memory energy devices. a) Reports qualitative operating regions of a device. b) Ragone plot. In green are reported some planar supercapacitors,^[3,43–45] in blue on-chip capacitors for different technological nodes (130 nm^[46] 65 nm and 28 nm FDSOI^[47]) and in red the value extrapolated for our work. c) Device area versus energy. The markers correspond to the energy stored at the minimum area, while the dotted lines represent energy-area scalability for some microsupercapacitors,^[3,43,48,49] on-chip capacitors,^[46,47] and our work.

element, whenever the cell is storing a logic “0.” In fact, electrochemical reactions are expected to take place either before the creation, or after the dissolution of the conducting filament. **Figure 8a** illustrates the operating regions, in terms of qualitative voltage and current domains, of such dual-behavior RRAM cell.

- II. Our study put into evidence that the faradaic processes happening inside our samples seem not involve the whole volume, as a linear trend of the current peak with the area could not be satisfied when enlarging the device diameter, but was instead verified when connecting multiple devices in parallel (Figure 8c). Consequently, the energy storage mechanism appears to be a “local” phenomenon, possibly limited to the switchable oxide region of the solid electrolyte. As a result, energy capability should be increased by

maximizing the number of devices connected in parallel, meaning that further downscaling would be beneficial to boost both memory and energy density.

- III. The estimated energy density achievable with our devices peaks around $3.5 \text{ pJ } \mu\text{m}^{-2}$ (at $v = 160 \text{ mV s}^{-1}$), while the maximum power density amounts to $80 \text{ pW } \mu\text{m}^{-2}$ (for $v = 5 \text{ V s}^{-1}$). The Ragone plot of Figure 8b benchmarks and compares our devices to other state-of-the-art integrated energy storage elements. Remarkably, the energy and power densities extrapolated appear to rival with those of integrated planar supercapacitors. Figure 8c reports stored energy versus sample area, highlighting that the energy could theoretically be linearly increased with the number of devices connected in parallel, up to values comparable to those of integrated planar supercapacitors.

Furthermore, the proposed technology (benchmarked at a minimum area of $0.07 \mu\text{m}^2$) provides the added advantage of being much more scalable, opening the possibility of realizing “deep granular supercapacitor” by means of RRAM elements.

IV. Practical measurements of reactions’ relaxation times are yet to be quantified for our study. For similar RRAM stacks at voltage ranges close to our CV tests, Tsuruoka et al. reported stable ion concentration coefficients in the order of hundreds of seconds.^[26] Furthermore, the eligibility of applications might be narrowed down to those who can benefit from relatively low relaxation times. In particular, one can consider that long relaxation times would be required for data storage application with unfrequent reprogramming, while short relaxation times could be sufficient as we address tiers on top of the memory hierarchy which require more frequent refresh or update. However, a comprehensive characterization is still to be performed in order to draw final conclusions on this aspect, as well as a detailed analysis of required relaxation times depending on the specific application.

6. Conclusion

In this work, we explored the new concept of RRAM-based in-memory energy devices, by conducting a preliminary energy storage characterization on state-of-the-art RRAM memory samples. Our study allowed us to confirm the faradaic nature of the processes taking place inside our devices, which exhibit “local” traits. Consequently, the proposed technology offers the advantage of raising both energy and memory density with downscaling. The extrapolated energy and power densities compare with SOA integrated supercapacitor, with the added benefit of being much more scalable. In conclusion, the proposed technology would well adapt to the IMC field, and has the potential of broadening its advantages by adding the energy storage feature inside the memory. Further evaluation is demanded: in particular, aiming to quantify the output voltage, columbic efficiency and experimental energy and power density capability. As a next step, new design solutions where the memory and energy performances are optimized could be explored, in order to bring the technology on the application level.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

dual behavior, energy in memory, RRAM battery

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