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Architecture and design of a room-temperature feedback loop between cryogenic Qubits measurements and control loops

Mathieu Toubeix *

Univ. Grenoble Alpes, CEA, List, F-38000 Grenoble, France
mathieu.toubeix@cea.fr

Résumé

Quantum computing has the potential to transform algorithms from superpolynomial to polynomial complexity. For example, Shor's algorithm [3] is exponentially more efficient than classical prime factorization algorithms.

To achieve this, quantum computers work with entanglement of states called quantum registers. One way of implementing qubits to form those registers is to use electron spin in semiconductor devices. This technology benefits from the maturity of the semiconductor industry and better coherence time than superconductors, currently, the most advanced qubit technology.

Nevertheless, through processes of decoherence and relaxation, these quantum registers are prone to errors. Those errors also occur during manipulation or readout of registers if physical parameters are not finely tuned. To overcome this issue, error correction and calibration are required. Both need to get information on the system with measurements, process this information at room temperature and then react. We call this process a feedback [10].

Latency is crucial for feedback, corrections must be applied before the system decoheres (~1 µs). Alongside with control and measurement, feedback needs to scale to several thousands of qubits to obtain a working quantum computer. Using FPGAs to implement feedback and its environment is the best compromise between latency (hundreds of nanoseconds), and flexibility [5].

The most mature academic FPGA-based architecture is from USTC [8] with a threshold-based feedback latency of 125 ns and an expected scaling to hundreds qubits (fig.1). Other projects are open-source [6], specialized for fast switching [4] or greater flexibility [7]. Condor project, an industrial project by IBM, will scale to 1121 qubits with a FPGA network by the horizon of 2023 [9].

We aim at implementing a scalable feedback-capable architecture for semiconductor spin-qubits. The state of the art focuses on superconducting qubits while our needs for semiconducting spin qubits are different in terms of frequencies and type of signal generations. We would like to implement more complex feedback schemes like Bayesian estimation and error correction codes. We expect a scaling to thousands of qubits while achieving acceptable feedback

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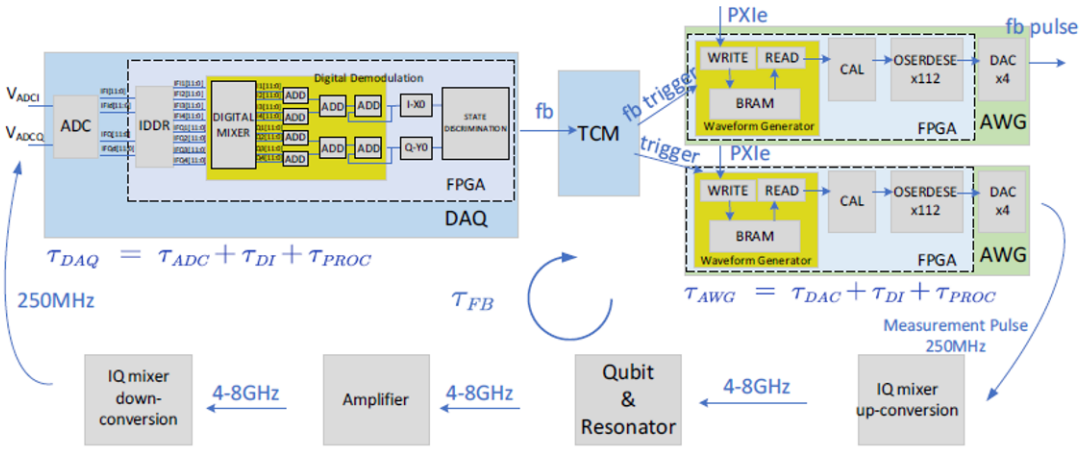
FIGURE 1 – Architecture proposed by Yang & al in 2022
Each module of the architecture like DACs, ADCs or synchronization module have their own embedded FPGA. They act has a distributed system communicating through PXIe protocol.



latencies. We will implement this architecture on the third generation RFSoC boards by Xilinx [1][2] embedding DACs and ADCs.

Mots-clés : Retroaction quantique, Architecture distribuée, Contraintes temps réel, FPGA, Optimisation

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