128-bit addresses for the masses (of memory and devices).

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128-bit Addreses for the Masses (of Memory and Devices)

Maplurinum — ANR Project ANR-21-CE25-0016
Machinæ pluribus unum: One Machine out of Many

Christian Fabre — Univ. Grenoble Alpes, CEA, LIST, 38000 Grenoble, France

HOTINFRA' 23 — Workshop on Hot Topics in System Infrastructure
June 18, 2023, Orlando, Florida, USA — Co-located with ISCA 2023

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Chandana Deshpande (Grenoble INP), Christian Fabre,
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Why RISC-V 128 bit?

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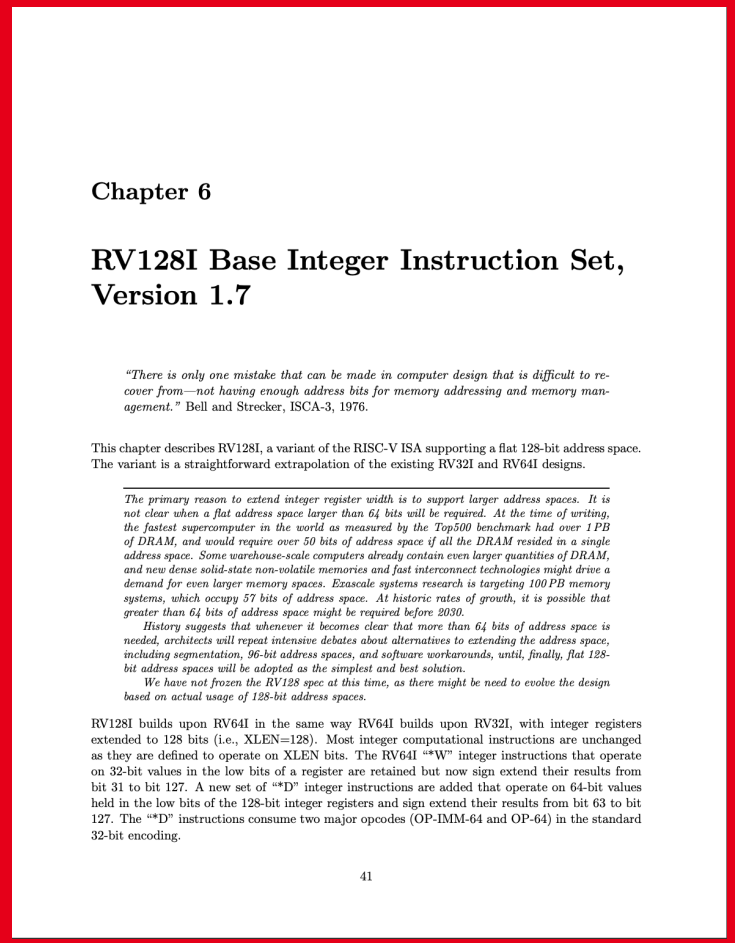

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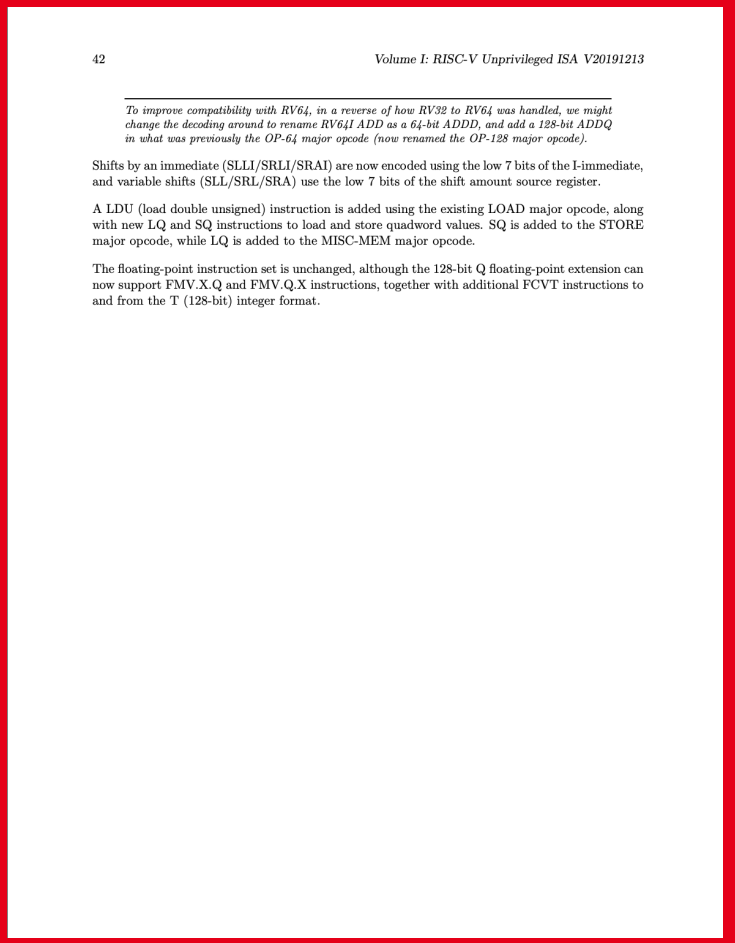

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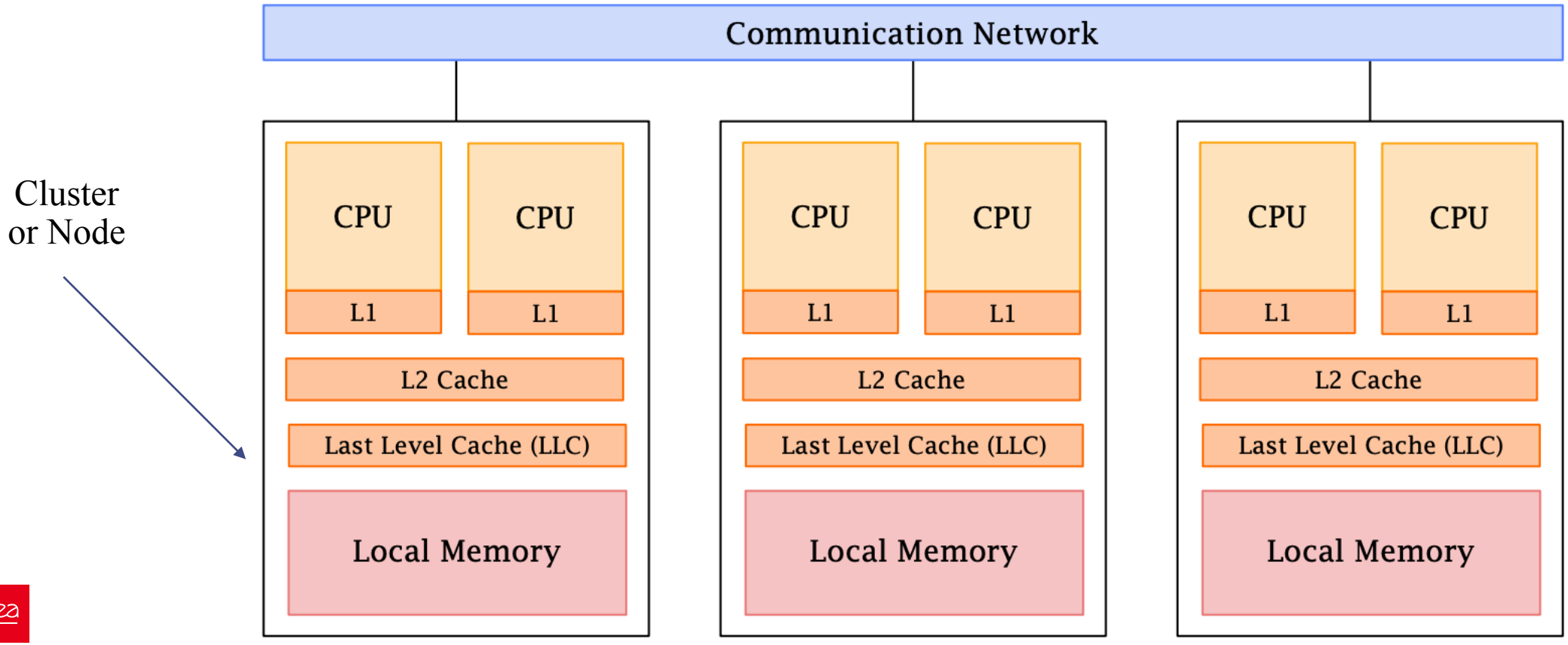
Context & Vision (1/2)

Hight Performance Computing (HPC) Hardware View

floating-point dominated computations

Supercomputers are composed of multiple shared-memory nodes connected through a high-performance communication network.



Context & Vision (2/2)

- Regular increase of total system RAM on HPC
  - The 64→65 bit threshold might be passed sometime around 2035
- Advent of byte addressable NVRAM

- What is a 128 bit software playground?
  - Now: One Linux instance per shared memory domain + MPI
  - Then: Single System Image (SSI).
  - Virtual pointers are valid across the whole machine.

- Use cases
  - “HPC”: Distributing huge dataset over clusters, floating-point compute bound
  - “Datacenter” : Temporary mappings of many shared objects by many threads

- RISC-V and ISA extensions help mitigate heterogeneity
  - Clusters might not support the same set of extensions: vector vs ML vs variable precisions etc.

- Ideas take 10-20 years to percolate, so start early!

Some Key 128 bit Issues

- OS design:
  - Single kernel will not scale on millions of cores
  - How can user and processes see the whole machine as a single entity (SSI)?
    - What abstractions to expose?
  - Data migration from cluster to cluster by VM page remapping instead of message passing across virtual spaces
  - Someone has to manage data locality
- Software tooling
  - What would be the 128 bit C programming model?
- System architecture
  - Communication network
  - Memory coherency scope:
    - Full machine scope not achievable.
    - Shall we aim at cluster scope only?
  - Virtual memory at the machine level
- µarchitecture
  - HW complexity
  - Moore/Dennard laws are MIA, so moving to 128 bit will not be as easy as old' 32→64 bit transition

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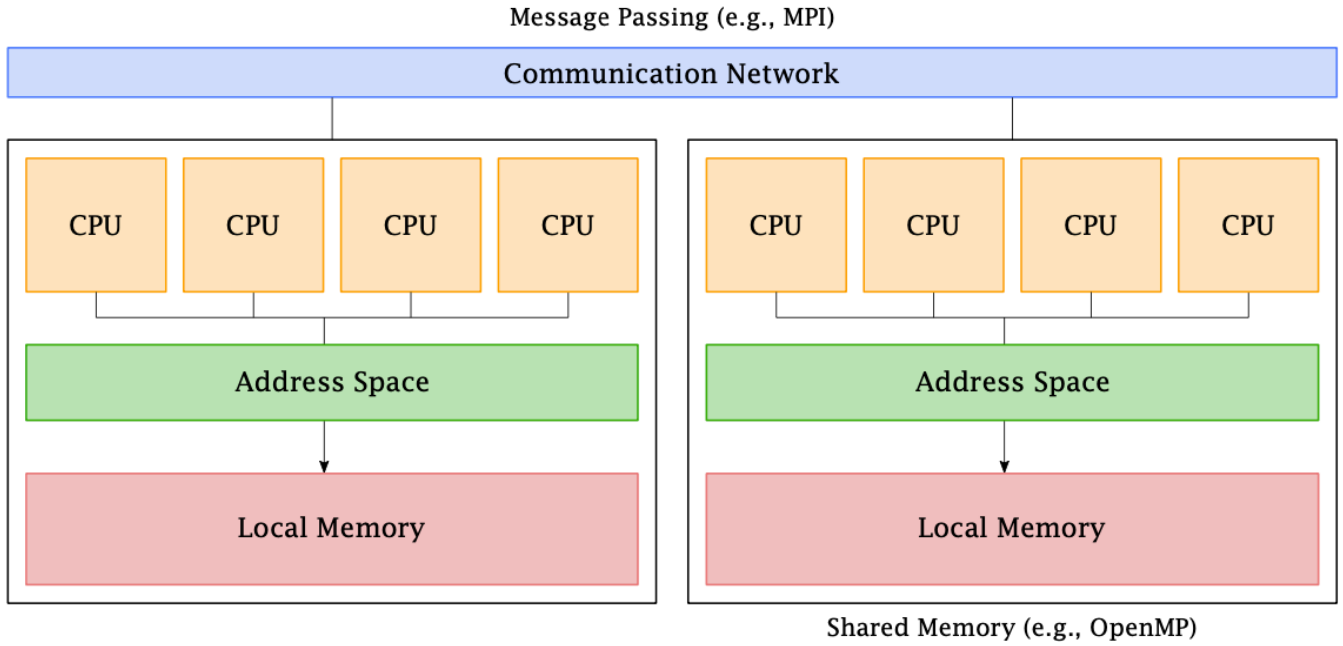
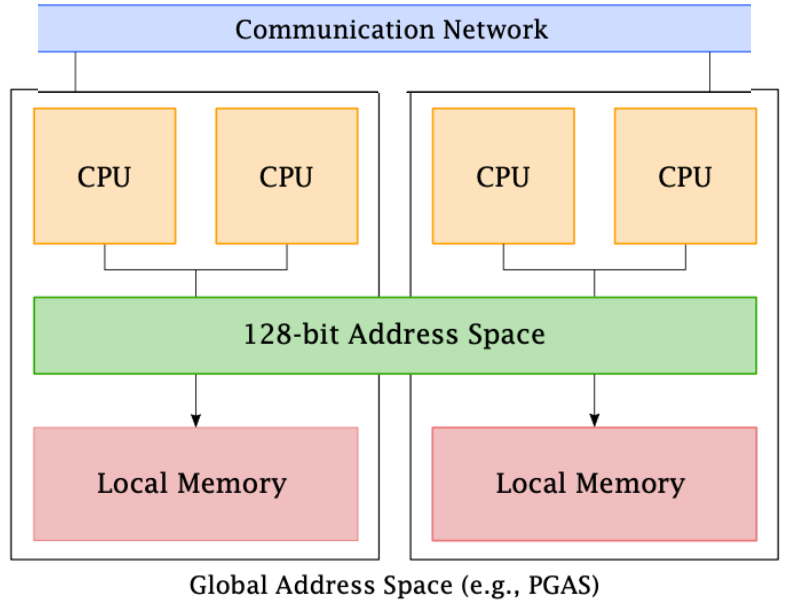
Operating System Research Avenues (1/2)



From one Linux per cluster
plus orchestration and middleware layers…



… to a machine-wide address space.
How to maintain and represent
such a virtual address space?

Operating System Research Avenues (2/2)

- Operating system at scale through multikernels:
  - One kernel per clusters
  - What is a virtual address space at the machine level?
  - Lend/borrow resources to other multikernels
- User abstractions
  - What is a machine-wide process?
  - Give view of topology to user, e.g. NUMA domains?
  - Allocate/free resources (does it need to be more than **`mmap()`** + *cpu bind* ?)
- Virtual Memory Open Questions
  - Page table organization:
    - More levels (business as usual) or novel organization?
    - Change minimum page size to 16K/ 32K or rely on superpages
  - How to ensure virtual address space consistency at the machine level
  - How to split HW/SW responsibilities for VM consistency
  - We do not have answers yet!

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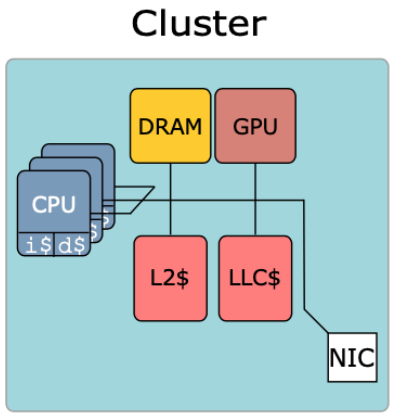
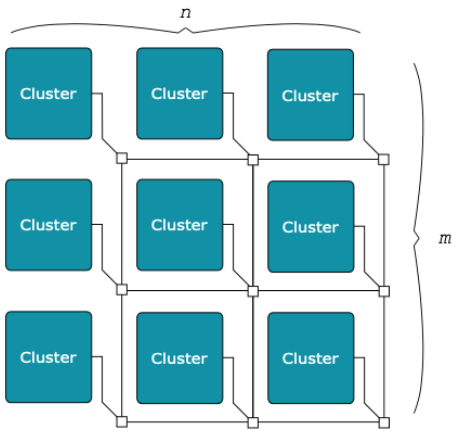
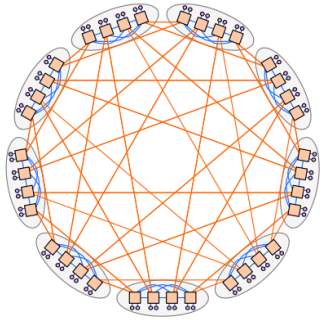
System Architecture Research Avenues

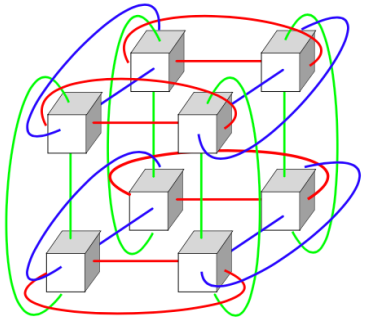




The cluster + interconnect architecture pattern is here to stay…



(a) Dragonfly



(b) Torus Fusion (Tofu)

…although the interconnect may change.

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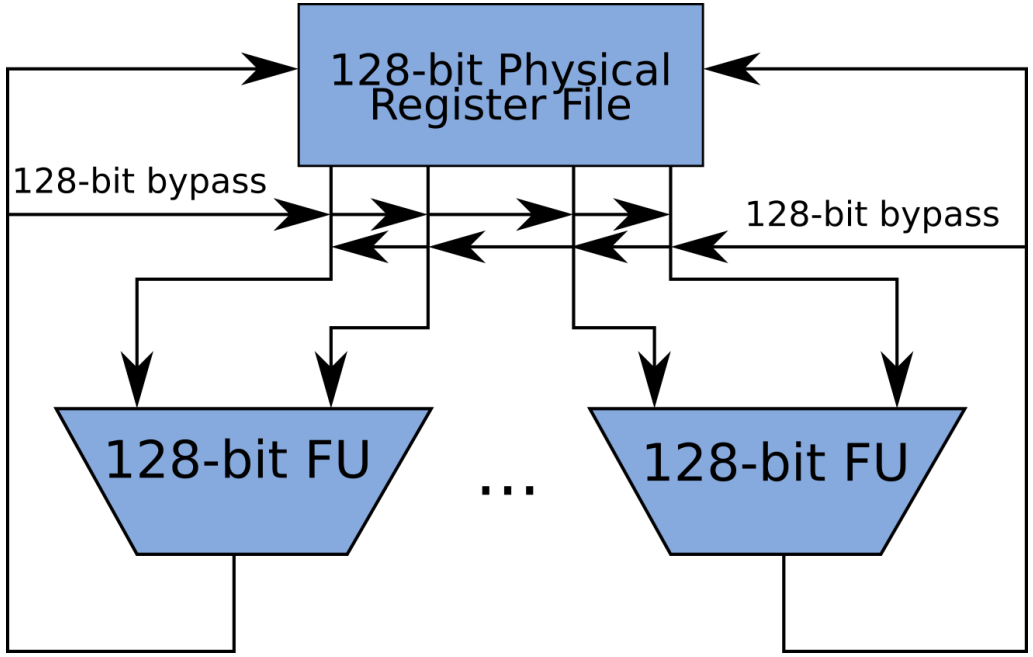
µArchitecure Research Avenues (1/3)



Some remarks:

- Implemented Virtual Addresses (VA) and Physical Addresses (PA) are not not 64 bit in current 64 bit HW
  - 128-bit transition is not 2x for µarchitecture structures that contain VA/PA, e.g. TLB tags, cache tags.
- Yet, registers, functional units, bypass network width has to double
  - This will bring latency, timing, and power costs
- Also, pointers occupy twice the space in cache memory
  - Should we increase cache line size to preserve spatial locality?

µArchitecure Research Avenues (2/3)

Problem statement — for now:

- Can we design a cost efficient transitional 128-bit µarchitecture with
  - Full 128-bit ISA support — i.e. RV128
  - Limited 128-bit data path
  - Reasonable performance

µArchitecure Research Avenues (3/4)

How we plan to address these issues?

- One key hypothesis: Get figures by compiling current C source for 128-bit.
  - `int` remains 32-bit, `long` remains 64-bit, etc.
  - Only pointer manipulation will be 128-bit
    - That is ~60% dynamic instructions on SPEC & Polybench on RV64G.
- Leverage this to divide & conquer the µarchitecture
  - 128-bit “address” cluster
  - 64-bit “compute” cluster
  - In essence, 64-bit instructions (40% dyn. insts.) will not consume 128-bit resources
- Address cluster has high value locality
  - Compress physical registers using region-based compression

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RISC-V 128 bit Toolset

Data type	LLP128
char	8
short	16
int	32
long	64
long long	128
void *, size_t, ptrdiff_t	128

Frédéric Pétrot's Github page:
`https://github.com/fpetrot/riscv-gnu-toolchain`

Software tools operational on bare metal:

- QEMU **`-cpu=x-rv128`**
  - most of it upstreamed since jan 2022.
- Binutils + gas + gld + gdb:
  - ELF128 support
  - RV128 opcodes
  - 128-bit relocs
  - *Relatively* simple thanks to **`__[u]int128_t`** native support
- gcc:
  - Instructions in machine description file
  - Only **`long long`** and pointers are 128 bit wide
- Still full of bugs, but a first step!

Conclusion: Let's define what RISC-V 128 bit will be!

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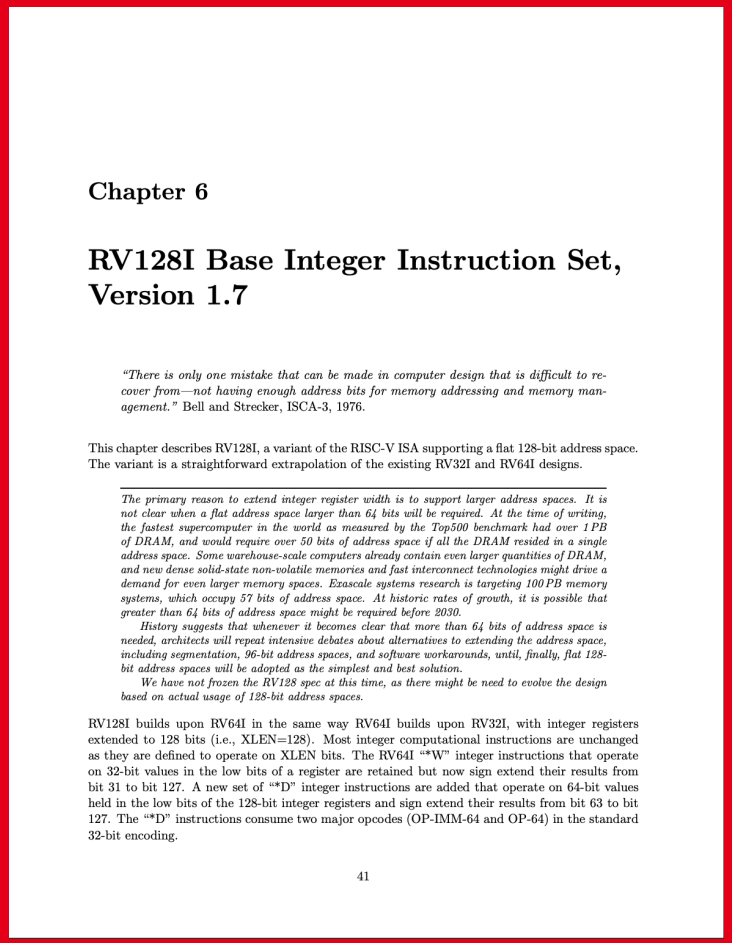

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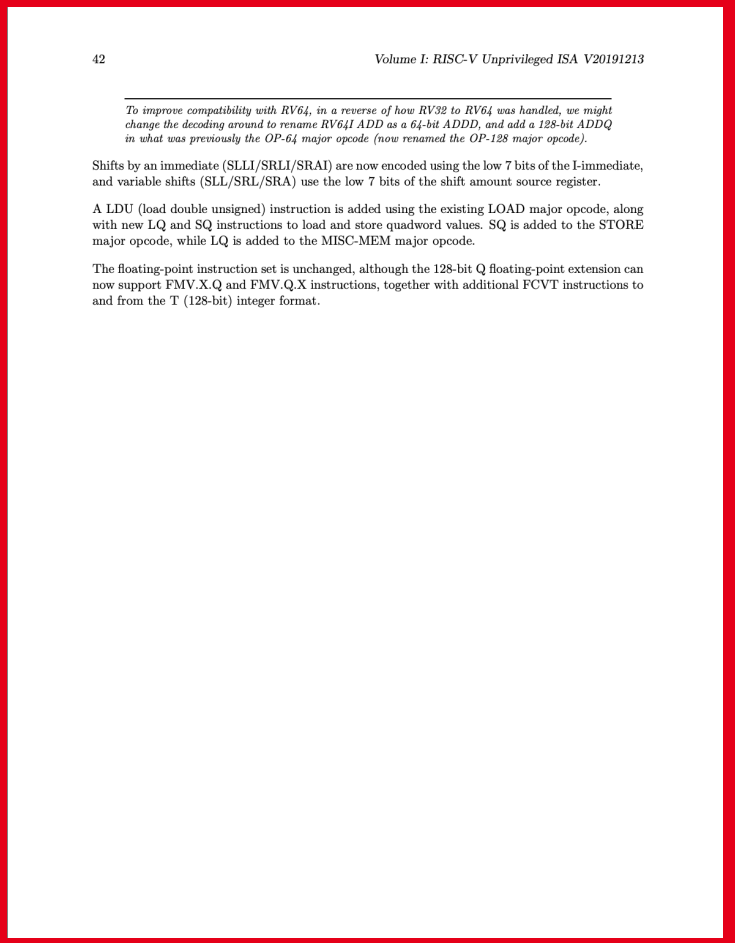

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