Characterization and Lambert-W Function based modeling of FDSOI five-gate qubit MOS devices down to cryogenic temperatures

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***Abstract* — FD-SOI five-gate (5G) qubit MOS devices are electrically characterized in linear regime down to deep cryogenic temperatures. The Lambert-W function is successfully used for the modelling of such 5G MOS devices from subthreshold regime to strong inversion. Its applicability is demonstrated down to 20 K. The 5G device is modeled as a series of five independent transistors: the "active" one, that directly controls the current, and the "external" ones, that act as access resistances. The Lambert-W function enables to accurately determine the inversion charge and the active channel resistance from weak to strong inversion. This approach allows reconstructing the drain current characteristic avoiding the evaluation of the mobility attenuation factors. The main device parameters are extracted versus temperature. Finally, the role of different scattering mechanisms has been investigated, underlying the impact of neutral defects for the gates in proximity of source and drain.**

Keywords – FDSOI, five-gate qubit device, characterization, Lambert function, modeling, parameter extraction.

I. Introduction

Quantum computing is an appealing technology for many fields, since it promises a boost in computational performances making it suitable to deal with exponentially-growing problems. In the last twenty years, many efforts have been devoted in developing solid-state qubits, and more recently, the fabrication of spin qubits based on Silicon-On-Insulator (SOI) CMOS platform has been demonstrated [1] [2] [3]. Their interest mainly relies on the possibility of converting the expertise in transistor manufacturing into large-scale qubit technology. Moreover, silicon quantum bits pave the way to the possibility to integrate the control CMOS – based electronics on the quantum processor itself [4]. Indeed, one of the main issues of nowadays quantum computers is the limitation in the number of wiring connections between the room temperature control electronics and the quantum chip. Since future quantum computers, in order to accomplish high demanding tasks, will require several hundreds or even millions of qubits, their co – integration with the classical electronics seems to be the only viable solution. Furthermore, for qubit mass production [5] [6], fast screening and selection of functional devices is mandatory, and electrical parameters extraction methods effective in a wide range of temperatures must be developed accordingly. Indeed, industrial approach to qubit manufacturing requires not only the technology to be mature and reliable, but also easy-to-use device compact models for device rapid characterization.

In this paper, we characterize a p-type FD-SOI five-gate qubit MOS transistor biased in linear regime down to very low temperatures. Particular attention is devoted to subthreshold regime at deep cryogenic temperature, where carriers are known to become degenerate, and Boltzmann statistics is not reliable anymore. Afterwards, we propose a model based on the Lambert – W function, whose validity is demonstrated, for the first time, down to deep cryogenic temperatures, fitting both the drain current and the $Y-function$ and providing the dependence of the main figures of merit with temperature. Moreover, the values of parameters such extracted are compared with those obtained using standard methods. Finally, transport scattering mechanisms are studied, in order to investigate the mobility behavior as function of the distance from source and drain.

II. Device and Experimental Details

The p-type five-gate device (5G) presented in this work is sketched in Fig. 1. It has been fabricated starting from

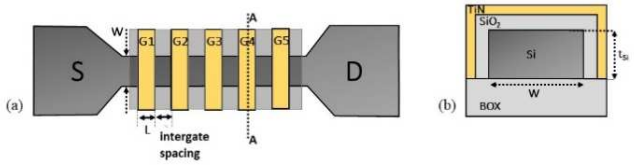

Figure 1. (a) 5G device top-view schematic. (b) AA cross-section view

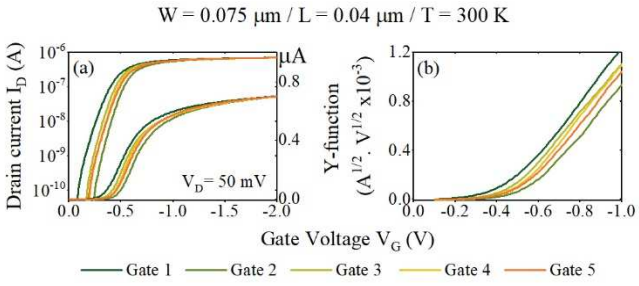

Figure 2. (a) $I_D(V_G)$ and (b) $Y(V_G)$ for every gate at T = 300K.

CEA-LETI FD-SOI NanoWire (NW) process flow [1] [3]. NWs are fabricated from $300\,mm$ SOI wafer, with $145\,nm$ thick buried oxide. The silicon film thickness is $t_{Si} = 17.9\,nm$, defining the NW height, and covered by a $6\,nm$ thick SiO_2 oxide and by a $5\,nm$ TiN metal gate (Fig.1). Si_3N_4 spacers, whose length is nominally equal to the gate one, i.e. $L_G = 40nm$, separate the gates. The channel width is $W_G = 75nm$. The device has been tested in a dilution fridge from room temperature down to 20K. Static measurements of the drain current in linear regime ($|V_{DS}| = 50\,mV$) were performed sweeping the voltage on one gate (*active gate*), while keeping the other gates (*external gates*) at a fixed

potential, namely $V_{G,ext} = -2V$. In such a way, the current was controlled by the active gate.

III. Experimental Results

A. Drain current transfer characteristics

Drain current $I_D(V_G)$ transfer characteristics for the five gates at room temperature are shown in Fig. 2(a). From $I_D(V_G)$ curves, it is clear that each gate exhibits a different threshold voltage V_{th} and a different low field mobility μ_0. Furthermore, access resistance strongly affects the behavior of the device at high gate voltages. It is worth to point out that here the access resistance comprehends both the source/drain resistances and the external gate channels. In Fig.2.b, we plot the corresponding $Y-function$, given by $Y(V_G) = \frac{I_D}{\sqrt{g_m}} = \beta^{\frac{1}{2}}(V_G - V_{th})$, where $g_m = \frac{dI_D}{dV_G}$ is the transconductance, $\beta = \frac{W_G}{L_G} C_{ox}\mu_0 V_D$ is the gain current factor and C_{ox} is the gate oxide capacitance. $Y-function$ is known to eliminate series resistance influence [7]. Both $I_D(V_G)$ and $Y(V_G)$ for different temperatures from 300K to 20K are presented in Fig. 3. Note the strong increase in the subthreshold slope as the temperature decreases (see also Fig. 4), as well as the increase of both the

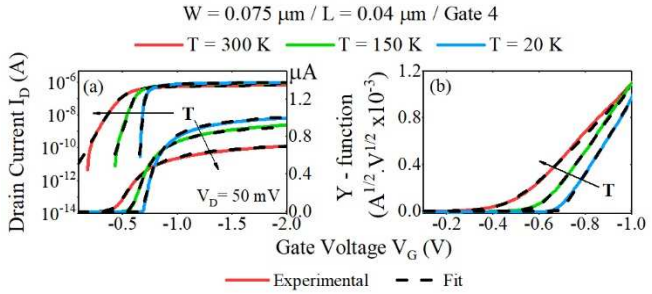

Figure 3. Experimental (straight lines) and fitted (dashed lines) (a) $I_D(V_G)$ and (b) $Y(V_G)$ curves for different temperature

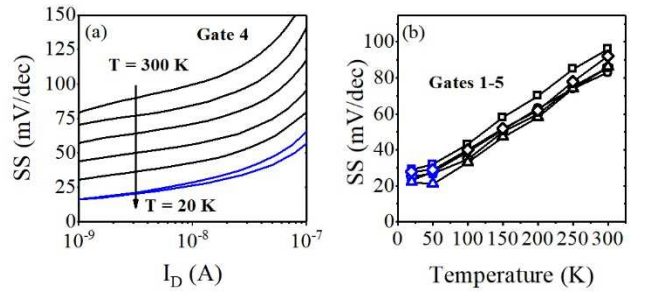

Figure 4. (a) $SS(I_D)$ for different temperatures. Below $T = 100K$ it starts to saturate. (b) $SS(T)$ for all the five gates.

threshold voltage and the drain current in strong inversion. The latter is due to the increase of the mobility μ_0, consequence of the phonon number reduction at cryogenic temperatures, as confirmed by the $Y-function$ slope, steeper at lower temperatures. Concerning the subthreshold regime, the subthreshold swing $SS = \frac{dV_G}{dlog(I_D)}$ follows the Boltzmann limit, i.e. it shows a linear behavior with temperature, down to $T = 70-80K$, before saturating to a value close to $20\ mV/dec$ (Fig. 4) [8] [9]. The trend is the same independently of the gate, and it is consistent with what is observed in standard CMOS technology. The saturation of SS at deep cryogenic temperature is due to the presence of exponential band tails in the density of states below band edge [8] [9]. Indeed, at low temperature the Fermi level falls into the band tail making the carriers degenerate. In this case, Boltzmann statistics is not valid anymore, and the metallic statistics prevails. The exponential band tails in MOSFET are likely related to potential-fluctuations-induced disorder [10] [11].

B. Lambert function based modeling

Lambert – W function allows to model the channel inversion charge $Q_i(V_G)$ using as fitting parameters both the subthreshold ideality factor n and the threshold voltage V_{th}, and, by turn, the drain current characteristic $I_D(V_G)$, for a given mobility μ_0 [12]. Here, we developed the model introduced in [13], assuming that the 5G device can be modeled in linear operation with five independent gate-controlled resistances placed in series, whose values depend on V_G (active channel) and $V_{G,ext}$ (access channels). Each resistance is characterized by different intrinsic parameters, i.e. V_{th}, n and μ_0. The active channel resistance, corresponding to gate i, is given by:

$$R_{Ch,i}(V_G, \mu_{0,i}, V_{th,i}, n_i) = \frac{1}{\frac{W}{L_G} Q_i(V_G, V_{th,i}, n_i)\mu_{0,i}} \quad (1)$$

with $Q_i(V_G, V_{th,i}, n_i) = n_i . C_{ox} . \frac{k_B T}{q} . LW\left(e^{\frac{V_G - V_{th,i}}{n_i . kT/q}}\right)$,

where k_B is the Boltzmann constant, T is the temperature in kelvin and q is the electron charge. The access resistance is computed as:

$$R_{Acc}(V_{G,ext}) = R_{ch,j}(V_{G,ext}, \mu_{0,j}, V_{th,j}, n_j) + R_{ch,k}(V_{G,ext}, \mu_{0,k}, V_{th,k}, n_k) + R_{ch,l}(V_{G,ext}, \mu_{0,l}, V_{th,l}, n_l) + R_{ch,m}(V_{G,ext}, \mu_{0,m}, V_{th,m}, n_m) + R_{Series} \quad (2)$$

where $R_{ch,i}, R_{ch,j}, R_{ch,k}, R_{ch,l}$ are the channel resistances of gates $i, j, k\ and\ l$, and R_{Series} is an additional fitting parameter to take into account the contribution of source and drain access. Since the number of fitting parameters is quite high, each gate has been considered individually, allowing the extraction of the intrinsic parameters from $Y(V_G)$ and the subthreshold current. After, the access resistance has been automatically computed according to Eq. (2), using R_{Series} as input parameter to fit $I_D(V_G)$ in strong inversion. It is worth noting that no degradation mobility laws as function of V_G have been introduced to account for current saturation at high voltages, actually dominated by access resistance effect. The fittings for both $I_D(V_G)$ and $Y(V_G)$ characteristics and for temperatures varying from 300K to 20K are shown in Fig. 3. The model successfully fits the drain current from subthreshold to strong inversion regime, allowing the extraction of the main device parameters (Fig. 5.(a)-(d)), whose values and trends are in good agreement with those extracted using classical methods. Indeed, both V_{th} and μ_0 have been extracted using the $Y-function$, while R_{Acc} has been derived from the expression of the first order attenuation factor $\theta_1 = \theta_{10} + R_{Acc}G_m$ [7], where θ_{10} is the intrinsic mobility reduction factor and $G_m = \frac{W}{L} C_{ox}\mu_0 . \theta_{10}$ has been neglected, since in such short channels the access resistance effect prevails. Finally, n has been extracted from the subthreshold swing according to $SS =$

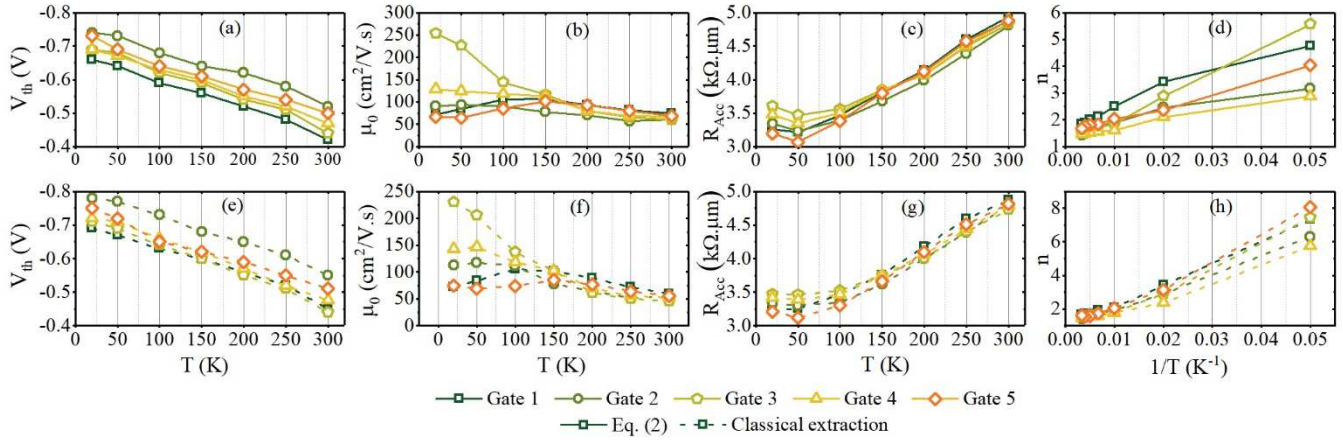

Figure 5.Parameters extracted for the every gate from room T down to 20K using eq.(2) (a)-(d) and classical extraction methods (e)-(h).

$n\left(\frac{k_B T}{q}\right) ln10$. It is important to underline that this expression of the subthreshold slope relies on the Boltzmann statistics; therefore, it is valid as far as the semiconductor is non-degenerate, i.e. down to $T \approx 70-80K$ in the present case. At lower temperatures, when SS in Fig. 4(b) saturates, the values of the ideality factor are not physically meaningful anymore [9]. n increases to keep SS constant while temperature lowers down. In the Lambert – based model, that relies on Boltzmann statistics as well, n is used as fitting parameter, and the comparison with the classical expression previously introduced has the sole scope of validating the consistency of the compact model with respect to the existing extraction methods. It must be noted that the discrepancy between Boltzmann and Fermi – Dirac statistics is mostly relevant in subthreshold region, because in strong inversion the Fermi level goes over the valence (conduction) band edge and $Q_i(V_G) \approx C_{ox}(V_G - V_{th})$.

The threshold voltage decreases quasi linearly with temperature (Fig. 5(a),(e)), independently on the gate, whereas the ideality factor n varies nearly as 1/T below 70-80K since SS is plateauing (Fig. 5(d),(h)). The low field mobility (Fig. 5(b),(f)), instead, shows different trends for different gates, revealing that the central device (gate 3) has a better mobility at low temperature. Exploiting the Mathiessen's rule it is possible to have the quantitative analysis of mobility behavior [14] [15]:

$$\frac{1}{\mu_0} = \frac{T}{300 \cdot \mu_{ph}} + \frac{300}{T \cdot \mu_C} + \frac{1}{\mu_{nd}} \quad (3)$$

where μ_{ph}, μ_C and μ_{nd} are the phonon, Coulomb and neutral defects scattering mechanisms, respectively. Eq. (3) is used to fit the experimental data (Fig. 6(a)), allowing the extraction of the different scattering mechanisms for every gate. It is clear from Fig. 6(b) that neutral defects are the limiting mechanism for gates closer to source and drain, whereas they are less impacting the central device. Indeed, the latter shows a mobility increase as the temperature is lowered down, coherently with a transport dominated by phonon scattering. These results are consistent with recent studies of mobility and transport in FD-SOI nano-devices, where it is shown that the scattering processes in highly scaled devices are led by source and drain neutral defects [14] [15].

Finally R_{Acc}, computed using Eq. (2), also shows a linear decrease with T down to $100K$, before saturating for temperatures below $100K$. In Fig. 7 are plotted both R_{Series} and $R_\beta = R_{Acc} - R_{Series}$. The latter decreases down to $T = 100K$, then it increments again for almost all the gates. This is coherent with the definition given in Eq. (1), since R_{ch} is inversely proportional to the low field mobility, that has been shown to be not very sensitive to temperature. The behavior of R_{Acc} is therefore driven by R_{Series}, that shows a metallic-like trend versus temperature.

It should be pointed out that, except for R_{Acc}, the values of the parameters extracted at room temperature are in line with standard FD-SOI MOSFET technology [12].

The highest value of both R_{Acc} and R_β below $T = 100K$ is found for gate 3, consistently with the mobility trend. Indeed, the resistance viewed from the other four gates is smaller because it includes the contribution of the central gate, which shows the highest mobility. For the same reason, the access resistance of gate 3 is the highest.

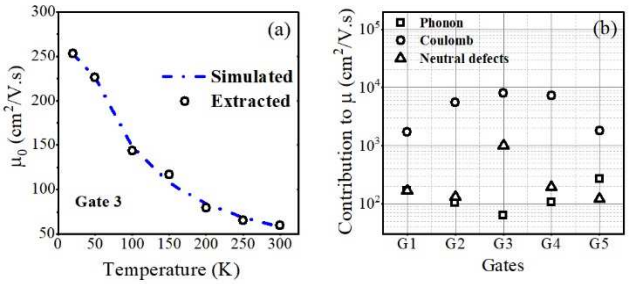

Figure 6. (a) Experimental (symbols) and simulated (dashed line) low field mobility as function of temperature. (b) Contribution of different scattering mechanisms to the total mobility

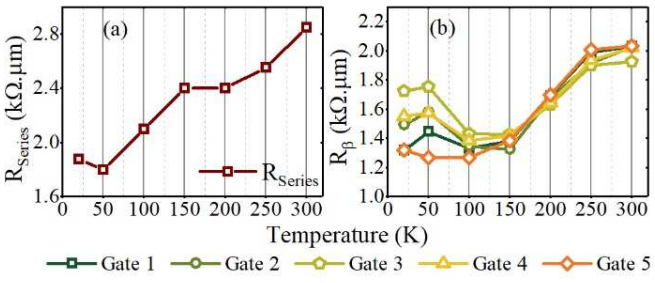

Figure 5 Series resistance $\boldsymbol{R_{Series}}$ (a) and $\boldsymbol{R_\beta}$ (b) down to 20K

It is worth to highlight that, with the exception of the central gate, the drain current increase at deep cryogenic temperature cannot be justified neither with an increased mobility nor a decreased R_β. Actually, it is mainly related to a reduction of R_{Series}.

IV. CONCLUSIONS

In this paper, we reported the functionality of a five-gate MOS based qubit device, biased in linear region, down to deep cryogenic temperature. Particular emphasis has been devoted to the subthreshold regime, where the subthreshold

slope shown the well-known linear temperature dependence, before saturating below $70 - 80\ K$. Furthermore, a compact model based on the Lambert – W function has been developed for both the drain current and the $Y - function$. Its validity has been demonstrated from subthreshold regime to strong inversion and from room down to deep cryogenic temperatures. Exploiting this model, the main device figures of merit have been extracted. Their values are in agreement with those obtained using classical extraction methods, and are in line with the state-of-the-art FD-SOI technology. Finally, the transport scattering processes have been investigated for different gates as function of temperature, highlighting different mechanisms depending on the proximity to source and drain. Consistently with previous studies, neutral defects scattering turned out to be the limiting mechanism in nano-scale devices transport.

In conclusion, we proposed a simple compact model for multi-gate MOS based qubit devices, valid in a wide range of temperatures, that could easily be extended to non-linear operation region and advantageously exploited as a characterization tool for the future qubit mass production.

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