HAL
open science

# Material and integration challenges for large scale Si quantum computing

M. Vinet, T. Bedecarrats, B. Cardoso Paz, B. Martinez, E. Chanrion, E. Catapano, L. Contamin, L. Pallegoix, B. Venitucci, V. Mazzocchi, et al.

## To cite this version:

M. Vinet, T. Bedecarrats, B. Cardoso Paz, B. Martinez, E. Chanrion, et al.. Material and integration challenges for large scale Si quantum computing. IEDM 2021 - 2021 IEEE International Electron Devices Meeting, Dec 2021, San Francisco, United States. pp.14.2.1-14.2.4, 10.1109/IEDM19574.2021.9720708 . cea-04413532

**HAL Id: cea-04413532**

**https://cea.hal.science/cea-04413532**

Submitted on 23 Jan 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Material and integration challenges for large scale Si quantum computing

M. Vinet[1], T. Bédécarrats[1], B. Cardoso Paz[2], B. Martinez[3], E. Chanrion[2], E. Catapano[1], L. Contamin[1], L. Pallegoix[1], B. Venitucci[3], V. Mazzocchi[1], H. Niebojewski[1], B. Bertrand[1] , N. Rambal[1], C. Thomas[1], J. Charbonnier[1], P.-A. Mortemousque[1], J.-M. Hartmann[1], E. Nowak[1], Y. Thonnart[1], G. Billiot[1], M. Cassé[1], M. Urdampilleta[2], Y.-M. Niquet[3], F. Perruchot[1], S. De Franceschi[3], T. Meunier[2]

[1]CEA Leti, 17 rue des Martyrs, email: maud.vinet@cea.fr
[2]CNRS Néel Institute, 25 rue des Martyrs, [3]CEA-IRIG, 17 rue des martyrs
Université Grenoble Alpes, Grenoble, France

***Abstract*—** Si spin qubits are very promising to enable large scale quantum computing as they are fast, of high quality and small. However, they are still lagging behind in terms of number of qubits. Indeed there are material and integration challenges to be tackled before fully expressing their potential.

## I. Introduction

Quantum computing is a fast evolving domain: the numbers of fabricated qubits keeps increasing and strategic roadmaps are released at a regular pace [1]. The hardware advances allows vivid discussions about whether quantum supremacy is yet reached or not [2]. So far these pioneering experiments rely on superconductors, cold atoms and trapped ions based qubits. Silicon spin qubits are still lagging behind with only two-qubit gate demonstrated so far [3] (marginally a four qubit Ge quantum processor has been build [4]). The point is that silicon (or SiGe) based qubits are believed to be very promising at individual scale: i) record spin lifetimes have been measured [5]; ii) high fidelity single and two qubit gates have been reported in a variety of silicon/silicon oxide and silicon/germanium devices [3]; iii) fast operations have been realized [5]. And very appropriately, these qubits should benefit from the maturity of the semiconductor industry to go to large scale. Fig. 1 provides a benchmark of relevant figures of merit for several experimental systems. In this paper, we will explore the material and integration challenges that are still in the way to fully exploit their potential at large scale.

## II. Silicon spin qubits

To go to large scale, most common silicon qubits (some other types have been proposed but they do not performed as well [5]) use the spin degree of freedom of an electron (or a hole) to encode the quantum information; they are named Loss Di Vincenzo qubits. The spin carrier (electron or hole) is confined in an electrostatically defined quantum well, surrounded by tunnel barriers. A static magnetic field creates the two-level system of spin up and down. To perform single gate rotations, the spins are submitted to a RF magnetic field, the only-B sensitivity is a protection against electrical noise and undesirable interactions with, e.g., phonons but makes it more difficult to manipulate. Then to build two-qubit gates, the tunnel barrier between adjacent dots is lowered controllably by a gate, to allow exchange interaction between the spins; the description of the spin qubit is schematically provided in figure 2. Measurement of the spin state is realized thanks to a spin-to-charge conversion [6]. Finally the qubit state is initialized, it can be reached by positioning the two-qubit states (up and down) above and below the Fermi level of a reservoir.

## III. Material challenges

*Channel material* hosts the quantum dots. The development of isotopically purified Si stack is needed to provide nuclear spin-free active substrates, which are key to suppress the spin dephasing associated with the hyperfine interaction, and in return to dramatically improve coherence time.

The lack of nuclear spins in the most abundant 28-silicon isotope makes it very suitable to engineer this noiseless environment. Earlier results have already shown a considerable performance improvement (T2*/T2) for a residual 29Si concentration of 800ppm [7]. For it to be widely used at large scale, not only is the supply chain still a challenge [8], but also there is a lack of specifications in terms of isotopic purity (presumably in the 10-800ppm range). In addition, the integration scheme to preserve the pristine material quality is still a question. Indeed thermal diffusion during integration tends to smear out 29Si in 28Si, see fig. 3 & 4. In bulk wafers, the strategy consists in growing thick epitaxy layers of 28Si (around 50 to 100nm). However, this technique does not work out for SOI wafers. The preferred option in this case is to build SOI wafers with a buried oxide made out of 28Si as well.

Control of the contaminants level inside and near the active channel may give rise to charged impurities and hence will largely affect the tunnel coupling as well as will increase device variability, ideally, O and C concentration below $10^{14}$ $cm^{-3}$ are targeted to limit this effect [9].

*Gate stack* - Interface roughness, charge traps, or process inhomogeneities shape the real space wave functions, hence the spin properties. It is, therefore, important to understand how sensitive the qubits are to their fluctuations in order to set constraints on the quality of materials and fabrication.. The presence of the traps firstly affects the shape of the dot as shown in fig. 5 and 6 for 2D and 1D geometries. Secondly, for electron qubits with synthetic spin-orbit coupling fields created by micro-magnets and for hole qubits with intrinsic spin-orbit coupling, early model of variability of single qubit properties (Larmor and Rabi frequencies) shows that this disorder can scatter Rabi frequencies over one order of magnitude. Charge traps have been found to be much more limiting than interface roughness [10]

These considerations provide a strong motivation for both improving smoothness and passivation of the Si/SiO2 interface to reduce variability to state-of-the-art densities ni < $10^{10}$ cm². Alternatively, switching from a crystalline/amorphous interface such as Si/$SiO_2$ to an epitaxial interface such as Si/SiGe (electron qubits) could be an option to reduce variability. In this case, extended defects such as threading defect dislocations (TDD) which are electrically active may induce an undesired "background doping". The density of such defects depends on the Ge concentration in the SiGe buffer, with state-of-the art TDD values down to $10^5 cm^{-2}$ for 25-30% Ge content.

Gate material choice is also a challenge. First, there is a need for a compatibility of the thermal expansion coefficients across the whole gate stack to avoid local potential peculiarities due to strain [11]. And secondly, because of the dimensions of the dots (around (100nm)² and below), we are in the range where random fluctuations have a strong impact on threshold voltage fluctuations (fig. 7). As for qubits, intentional source and drain doping is far away from the dots, this fluctuation strongly depends on the metal gate granularity [12].

## IV. Integration challenges

*To control* the qubit operations, one needs both to define the chemical potential of the dot and to control of the tunnel barriers between dots. 1D design relies on plunger and barrier gates alternatively spaced along a single active area. This geometry requires aggressive gate pitch (50nm and below) that can be achieved through a dual nested gate process [13]. Alternatively, figure 9 proposes a simplified integration scheme to minimize the technological developments for the transitory 1D geometry. No matter the integration scheme, gate oxides are deposited sequentially and thus cannot be both thermal, it will induce a trade-off between control and variability as discussed in the previous paragraph.

In this context, SOI structure is of high interest because the back gate is used as an accumulation gate and the plunger and barrier gate are separated from the dot by the Si channel reducing the impact of the top interface and the stringent need for low interface traps.

*Layout for read out* - To measure the spin state of a single electron in a quantum dot, we use a spin-to-charge conversion, which relies on two main physical concepts: either direct charge measurement thanks to an electrometer or capacitive measurements [6]. In both case, a double dot system is needed, schematically one dot stores the qubit information, and the other helps to read it. In addition, an electron reservoir on the side permits to load electrons in the dots. Figure 10 provides examples of layouts used so far for single and double qubits. Extension of this principle to 1D array is more or less straightforward as illustrated in fig. 8 and 9. However, this topology, with the sensor dot and the qubit on the same layer, leads to a brainteaser when it comes to 2D arrays: how to engineer an array of interconnected qubits, with an individual sensor for each qubit?

To overcome this, we proposed to leverage 3D monolithic integration, which permits placing the qubit on top of the sensor to design a unitary cell to be repeated to layout a 2D array compatible with quantum error correction, fig. 11. Electrostatic simulations [14], fig.12, show that carriers can be moved controllably between top and bottom layers.

After the quantum chip has been fabricated comes the question of its control: the challenge essentially lies in the large number of input and output signals to control and read the qubits, all inside a cryostat around 100mK. This is driving important efforts to develop Cryo-CMOS control electronics embedded at proximity of the quantum devices in the cryostat. Capacitance of the lines are of prime importance when it comes to read out [6], the interconnection between the quantum and the control electronics chips is thus crucial. The common assumption is that the two chips will be fabricated in two different technologies inducing a need for interconnecting them at low temperature. From all interconnect technologies, 3D ones are favored because of their low capacitance. Several options are possible and no choices have been made yet, the trade-off is between pitch, thermal stability, resistance and capacitance of the technology. To this end, we compared the potential and properties of SnAg microbumps and direct Cu bond interconnects, fabricated with 300 mm Si wafer technologies, for operation at cryogenic temperatures [15]. Both schemes exhibit promising thermal reliability and low temperature resistance below 50mohm, fig. 13. But with the possibility to reach ultra-fine pitch $\leq 1$ µm[16],Cu direct bonding could be of high interest to design low capacitance paths. Lastly, use of superconducting interconnects is an option to engineer the thermal coupling between control and quantum chips.

## V. Test and characterization

Qubit characterization flow is still an open debate. As for transistor, quality metrics have to be defined at different fabrication steps. It starts at the substrate level with peak mobility and interface trap density, at the quantum dot level, inter-dot tunneling barrier in operating regime, charging energy, Vt of the first electron and their respective dispersion need some quantification as well as the noise spectrum. There is an effort to correlate these metrics with room temperature MOS figures of merit (mobility, Vt…). A characterization flow aggregating room temperature parametric test, cryogenic automated testing, and dilution fridge qubit characterization is under construction. High volume cryogenic electrical probe station is an asset to provide statistical measurements; it should help going from few characterized samples per week to several thousand per day. In 2018, 2K fully automated 300mm probe station was designed by Intel and Bluefors [17]. It will be leveraged to build correlations to infer the final quantum circuit performance.

## VI. Conclusion

Silicon qubits are still behind in spite of promising features. Indeed material innovation are introduced: 28Si, low Dit and low granularity gate stack. FDSOI is an asset to reduce the impact of the interfaces by tuning the carrier position inside the dot. The integration routes require new layouts and demand for two gate level and lastly 3D interconnects are used to connect control and quantum chips with low parasitics.

## References

**[1]**https://quantumcomputingreport.com/ibm-unveils-a-quantum-computing-roadmap-that-will-take-them-to-one-million-qubits-and-beyond/,https://www.globenewswire.com/news-release/2021/06/29/2255028/0/en/Rigetti-Computing-introduces-world-s-first-scalable-multi-chip-quantum-processor.html **[2]** Yulin Wu *et al.*, Strong quantum computational advantage using a superconducting quantum processor, arXiv:2106.14734v1 [quant-ph] 28 Jun 2021 **[3]** W. Huang *et al.*, Fidelity benchmarks for two-qubit gates in silicon. Nature 569, 532–536 (2019) **[4]** N.W Hendrickx *et al.* A four-qubit germanium quantum processor. *Nature* **591,** 580–585 (2021) **[5]** P. Stano and D.Loss, Review of performance metrics of spin qubits in gated semiconducting nanostructures, arXiv:2107.06485v1 [cond-mat.mes-hall] 14 Jul 2021 **[6]** T. Meunier *et al.,* "Qubit read-out in Semiconductor quantum processors: challenges and perspectives," IEDM), (2019) **[7]** Veldhorst *et al*., An addressable quantum dot qubit with fault-tolerant control-fidelity. Nature Nanotech 9, 981–985 (2014). **[8]** V. Mazzocchi *et al*., 99.992% 28Si CVD-grown epilayer on 300 mm substrates for large scale integration of silicon spin qubits, Journal of Crystal Growth, Volume 509 (2019) **[9]** J. Klos *et al*., Calculation of tunnel couplings in open gate-defined disordered quantum dot systems, Phys. Rev. B 98, 155320 **[10]** B. Martinez, Y.-M. Niquet, Variability of electron and hole spin qubits due to interface roughness and charge traps, arXiv:2107.10902 (2021) **[11]** T. Thorbeck and N. M. Zimmerman, Formation of strain-induced quantum dots in gated semiconductor nanostructures, AIP Advances 5, 087107 (2015) **[12]** Q. Zhang *et al.,* "Experimental Study of Gate-First FinFET Threshold-Voltage Mismatch," IEEE Transactions on Electron Devices (2014) **[13]** R. Pillarisetty *et al.,* "Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology," IEDM (2018) [14] Y.-M. Niquet et al., "Challenges and perspectives in the modeling of qubits," IEDM (2020) **[15]** C. Thomas, *et al*., "Die-to-Wafer 3D Interconnections Operating at Sub-Kelvin Temperatures for Quantum Computation," *2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC)* (2020) **[16]** A. Jouve *et al.,* " 1 µm pitch direct hybrid bonding with < 300nm wafer-to-wafer overlay accuracy, " *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference* (2017) **[17]** R. Pillarisetty *et al.,* "High Volume Electrical Characterization of Semiconductor Qubits," IEDM (2019)

## Acknowledgments

This work was partly supported by the EU through the H2020 QLSI project and the European Research Council (ERC) Synergy QuCube project.

| | Superconductor | Si spin qubit | Trapped ion | Photon |
|---|---|---|---|---|
| Size* | (100µm)² | (100nm)² | (1mm)² | ~(100µm)² |
| 1qubit fidelity | 99.96% | 99.93% | 99.98% | |
| 2qubit fidelity | ~99.3% | >98% | 99.9% | 50% (measurement) 98% (gates) |
| Speed** | 12-400 ns | ~5 µs | 100 µs | 1 ms |
| Variability | 3% | 0.1%-0.5% | 0.01% | 0.5% |
| T° of operation | 15mK | 1K | 10K | 4K/10K |
| Entangled qubits | 65 (IBM) | 2 (4 - QuTech) | 32 (IonQ) | 70 (Pan-China) |

Fig.1: Benchmark of the experimental quantum platforms
* Estimation taking into account all the quantum functionalities (read out, control and initialization)
** Speed of the limiting operation between read out and measurement

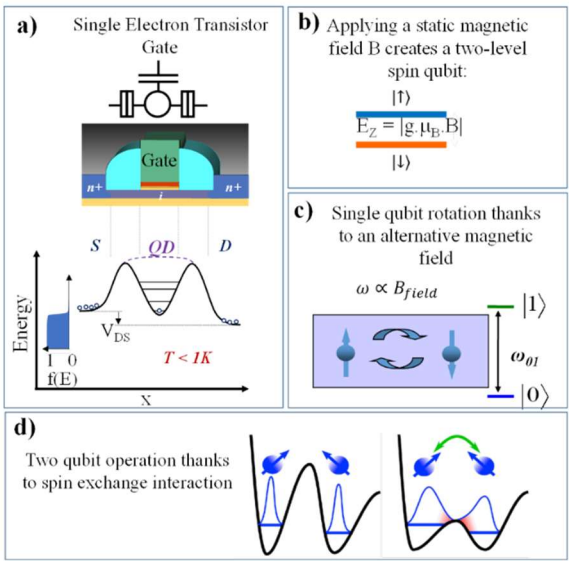


Fig.2: Description of single silicon spin qubit. a) A quantum dot is shaped under the gate thanks to nitride spacers induced barriers. One single charge is loaded in the dot. b) A static magnetic field is used to create the two-level spin qubit. c) Single spin rotation is performed thanks to an alternative magnetic field which frequency is proportional to the energy difference between spin up and down. d) Two qubit operation rely on energy exchange achieved thanks to barrier lowering between two adjacent dots.

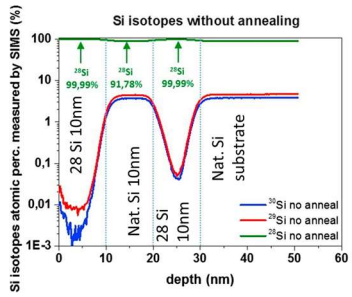


Fig. 3: Si isotopes atomic percentages from SIMS in a 28Si 10 nm/natural or standard Si 10 nm/28Si 10 nm stack grown at 650 °C, 20 Torr with 28SiH4 and natural Si2H6 on a bulk Si(0 0 1) substrate

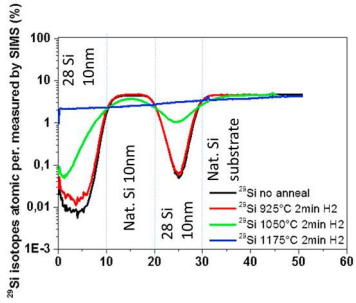


Fig. 4: 29Si atomic percentages from SIMS in the same sample as in fig.3 for different annealings used during the integration

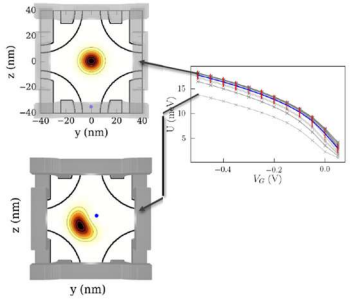


Fig.5: Left - Shape a 2D dot (wave function) as a function one single charge (in blue). Right – Charging energy for different charge disorder configurations.

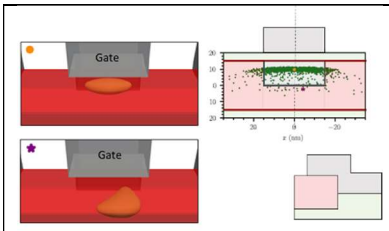


Fig.6: Iso-density surface of the squared ground-state wave function of a pristine hole device (orange point) and (b) a disordered device (purple) at ni = $5.10^{10}$ $cm^{-2}$ . Right - Distribution of the average position of the ground state for different realizations of the charge disorder at ni = $5.10^{10}$ $cm^{-2}$.The orange point and purple star are the devices from the right.

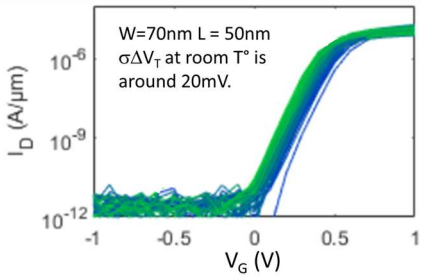


Fig.7: Id-Vg of single gate qubits measured as transistors at room temperature. The spread of the characteristics matches state-of-the-art advanced CMOS and is believed to be mostly determined by metal gate granularity (in this set of data a SiO2/TiN/poly gate stack has been used).

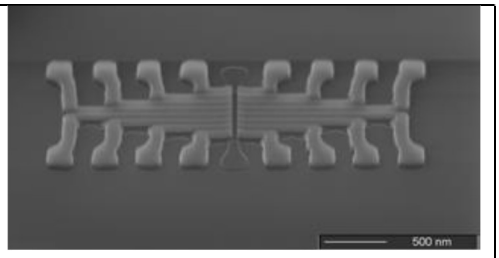


Fig.8: SEM top view of a 1D device with 8 qubits faced by 8 sensors to implement the spin-to-charge conversion required for spin read-out.

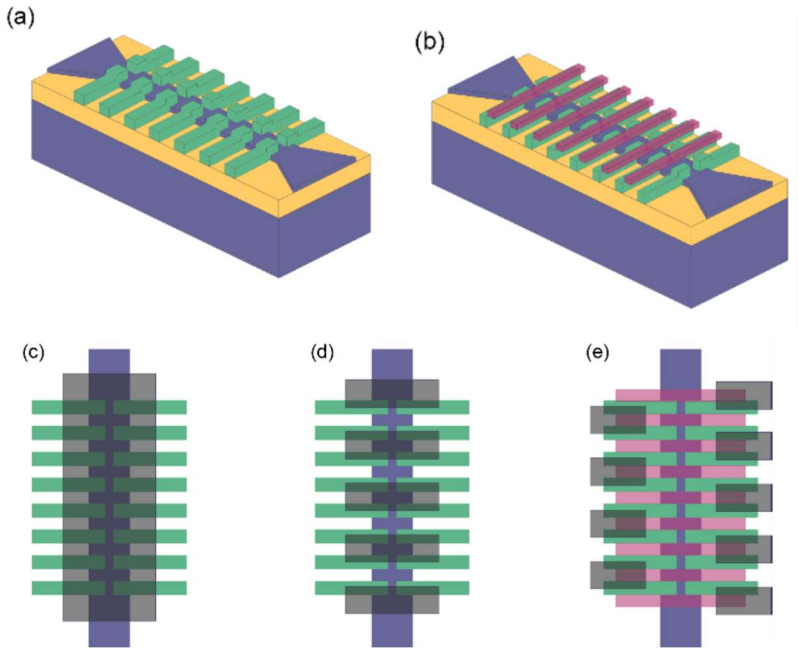


Fig.9 : Example of the integration strategy for the design of controllable qubits with exchange gates. (a) Starting point is nanowires (silicon in blue) with only split-gates in series (green). (b) A a second layer of exchange gates (in pink)is defined to allow the tuning of the tunnel coupling between pairs of split-gates. Intermediate alternative options rely on use of M1 layer to either define c) a global top gate in the Metal-1 layer (in grey) or multiple strips of metal-1 **(d)** and finally the dedicated level of exchange gates **(e)**.

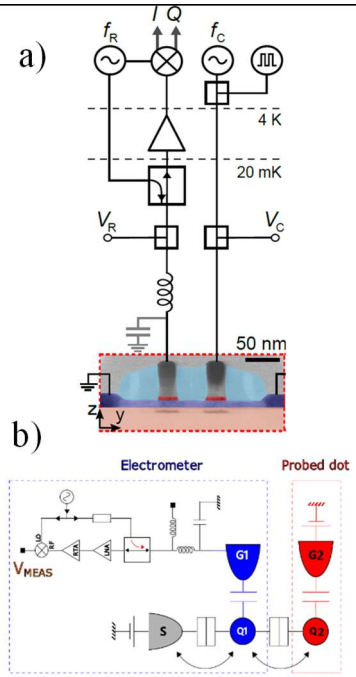


Fig. 10: a) . Si Double quantum dot system with radio frequency gate reflectometry set-up defined on the left hand side dot. b) Single quantum dot (probed dot) coupled to a close- by electrometer made out of a single dot and a single electron reservoir.

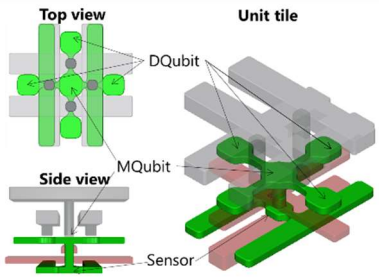


Fig.11: Unitary cell for 2D array compatible with quantum error correction. The sensor is located in a layer below the qubit and can be connected to reservoirs if needed.

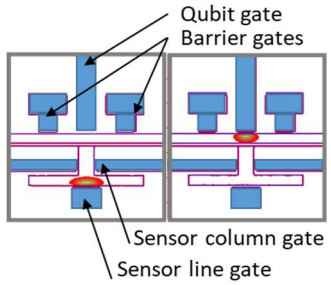


Fig. 12: 3D electrostatic simulations (assumptions and methods described in [14]) showing that in the unitary cell, electron can be moved up and down.

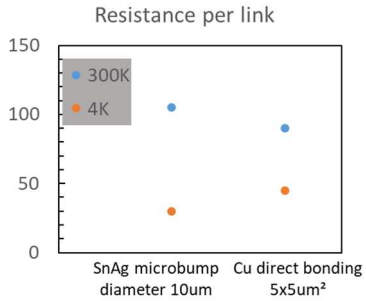


Fig.13: Resistance of SnAg microbump and Cu direct bonding at 300K and 4K. Data are from reference [15].