X ray nanoprobe for fault attacks and circuit edits on 28-nm integrated circuits

Sophie Bouat, Stephanie Anceau, Laurent Maingault, Jessy Clediere, Salvo Luc, Remi Tucoulou Tachoueres

X ray nanoprobe for fault attacks and circuit edits on 28-nm integrated circuits

S. Bouat[1], S. Anceau[1], L. Maingault[1], J. Clédière[1], L. Salvo[2], and R. Tucoulou[3]
[1]*Univ. Grenoble Alpes, CEA Leti, F-38000 Grenoble, France* – [2]*Univ. Grenoble Alpes, CNRS UMR5266, Grenoble INP, Laboratoire SIMaP, 38000 Grenoble, France*– [3]*ESRF, 71 av. Des Martyrs 38000 Grenoble, France*

***Abstract* — Ionizing radiations pose risks to Integrated Circuits (ICs) in space devices and nuclear reactors, but their effects are mitigated by specific designs and redundancy. Besides characterizing radiation faults, X-rays can be intentionally used to modify IC behavior. This study demonstrates inducing semi-permanent faults in 28 nm technology node transistors using a 50-nm nanoprobe beam from the European Synchrotron Radiation Facility. Precise X-ray flux control enables targeted perturbation of transistors without invasive attacks, expanding applications to circuit edits and fault attacks. Cheaper and more accessible X-ray beams enable inducing similar effects, though on older technologies for the moment.**

***Index Terms*— CMOS integrated circuits, cybersecurity hardware, , ESRF X-ray nano-beam, laboratory X-ray source, single transistor fault, technology node, Total Ionization Dose (TID) effects, X-ray attacks, circuit edit, Focused Ion Beam.**

I. Introduction

In the space or nuclear applications, ionizing radiations can dramatically damage Integrated Circuits (IC) by macroscopically altering the contents of memory cells [1] –[4] or any other ICs structures. Shielding techniques, such as the use of X-ray-absorbing materials or packaging modifications, can attenuate the X-ray radiation before it reaches the sensitive components of the IC. Design considerations, such as layout optimization, introduction of guard rings, and implementation of radiation-hardened architectures, can also mitigate the impact of X-ray-induced effects. However, such perturbations have never so far been used as a tool for modifications on devices or to attack ICs. More specifically, there are many X-rays generators that would perturb or modify integrated circuit, in a controlled way in order to induce specific faults or to modify a precise part of the circuit. Two main applications are targeted. First, in the cybersecurity field [5] , there are many means of attacks on hardware devices such as smartcards: disturbances by laser illumination [6] , [7] , generation of short electric pulses on the power supply or clock [10] , focused ion beam (FIB) probing [11] . X-ray attacks could constitute a new path for attacking circuits as will be demonstrated below.

On the other hand, circuit edit [12] , the process of modifying or repairing electrical circuits within semiconductor chips, plays a critical role in the development and optimization of integrated devices. Circuit edit encompasses a range of methodologies tailored to achieve modifications at the microscale. These methodologies enable corrections, debugging, and customization of ICs. Various techniques, such as laser microsurgery, laser analysis [8] , electron beam lithography, or focused ion beam (FIB) technology, are employed based on the specific requirements of the circuit edit process. This paper aims at showing that X-ray irradiation could be used for circuit edit, targeting specific transistors, with a lesser invasive technique. Indeed, X-rays is hardly absorbed into device IC and can directly perturb a transistor, keeping the editor away from all the invasive etching, depackaging steps.

In 2017, experiments conducted with a nano-focused beam on the European Synchrotron Radiation Facility (ESRF, Grenoble) have shown that it is possible to erase information contained in a single Flash or SRAM memory cell on an old 350-nm technology node [14] . Non-focused X-ray beam generated by regular laboratory equipment is known to erase Flash and EEPROM memory cells [2] , faulting at a random position a single transistor [15] . It can be used to study circuits behavior in space under the effect of natural X-ray irradiation, such as the CMOS-ICs that are sent in satellites [9]. Other studies have investigated the effects of X-illumination on circuits on laboratory equipment [16] [18] , or on electronics devices working in large-scale facilities environment [19] . These studies are not attacks focused on a transistor and X-rays are either used as a means of inspection or retro-design or to study the harmful effects of irradiation [20] .

It is within this framework that attacks are performed with the nano-focused beam from the ESRF on current technology nodes such as 28 nm technologies (the last planar technologies before the FinFETs [21]). It is possible to quantify the needed doses to fault semi-permanently a single transistor, in many parts of the IC, registers, SRAM or FLASH memories. X-ray attacks are also conducted with a laboratory X-ray source on 350-nm technology CMOS-ICs to compare with attacks made on the same CMOS-ICs at the ESRF earlier [14] .

II. European Synchrotron Radiation Facility

A. Experimental details

The ESRF (European Synchrotron Radiation Facility) produces an ultra-bright X-ray beam. Few specific beamlines are able to produce a nano focused X-ray beam. Amongst them, the ID 16 B beamline is a hard X-ray nanoprobe dedicated to nano-tomography and spectroscopy [23] . In this work, the focused beam is used as a weapon against electronic devices. The X-ray energy delivered at ID 16 B can be 17.5 keV or 24.7 keV, with a flux around 10^{10} photons/s and a minimum focused beam size of approximately 50 nm.

Computer interfaces have been developed to monitor the state of transistors in the targeted devices, either after each attack or by a continuous reading of the device during the attack. CMOS-ICs are switched-on during the attacks, except

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when it is indicated that they are switched-off intentionally.

B. 28-nm CMOS device

Most of the circuit modifications are done on 28-nm specific CMOS chips. This device is a RISC-V microcontroller featuring dedicated test zones for flip-flops and SRAM denoted as Block 5 and Block 6 on Fig. 1. These fundamental blocks serve as effective demonstrations of the modification potential across various components of digital circuits. Additionally, the physical layout of the device is known, facilitating the precise targeting of specific transistors. These flip-flop and SRAM cells can be directly programmed and read thanks to a dedicated Serial Peripheral Interface (SPI).

C. X-ray nano-beam attacks

This 28-nm CMOS-IC is attacked with the ESRF X-ray nano-beam at the ID 16 B beamline. Precise X-ray beam positioning is the key to ensure that a single transistor is irradiated. To position the nano-beam before an attack, the optical image observed with the in-line visible light microscope of the experimental setup is not accurate enough (Fig. 1 on the left). At ID 16 B, fluorescence maps can be measured with sufficient accuracy to visualize the upper metal structures and position very precisely the nano-beam (Fig. 1 on the right).

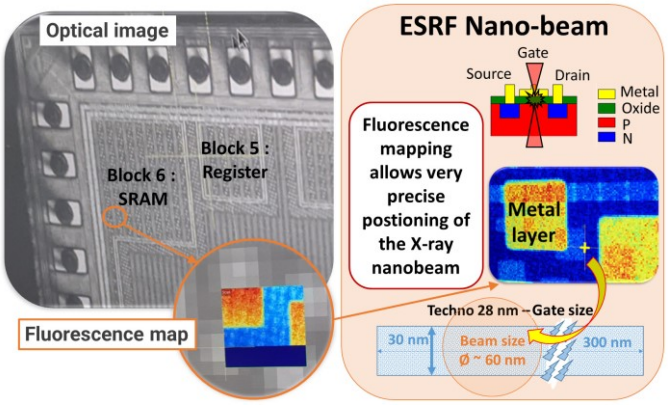

Fig. 1. On the optical image (on the top left), fluorescence maps (on the bottom left and on the right) are realized to target transistors at different positions, thanks to the visualization of the upper metal structures of the CMOS-ICs.

D. Irradiation effects on transistors

Fig. 2 presents the schematic diagram of the flip-flops in this device. The extremly small beam size (50 nm in diameter), allows for the precise addressing of individual transistors. In the area of interest, the smallest transistor exhibits a gate size of 30x200 nm. The literature extensively describes the effects of Total Ionization Dose on transistors: p-type transistors become blocked as the radiation dose increases, while n-type transistors experience leakage. The faults resulting from X-ray attacks are categorized as semi-permanent since their impact can persist anywhere from a few days to several months, depending on the dose.

To induce circuit modifications, the focus was placed on the last two inverters within the flip-flop structure. Fig. 2 illustrates the four transistors comprising this double inverter at the bottom. By understanding the effect of X-ray radiation on each transistor type, the overall impact on the entire gate can be anticipated. For example, if X-rays are targeted at the last n-type MOS transistor, it will gradually begin to leak current. This leakage may arise due to a decrease in its threshold voltage and/or leakage occurring in the surrounding Shallow Trench Isolation (STI) regions. Consequently, the n-type MOS transistor draws current from the V_{SS} supply. As a result, after a specific dose, the output Q of the gate becomes stuck at V_{SS}. It appears that this current leakage surpasses the normal current drawn from the p-type MOS transistor. A similar reasoning can be applied to the n-type MOS transistor in the penultimate inverter, but in this case, the output Q of the gate becomes stuck at V_{DD}.

When the p-type MOS transistor in the last inverter is subjected to irradiation, the gate output consistently remains at V_{DD}. The blocked p-type MOS transistor is no longer capable of driving the gate output to V_{DD}, causing the gate to become stuck at V_{SS}.

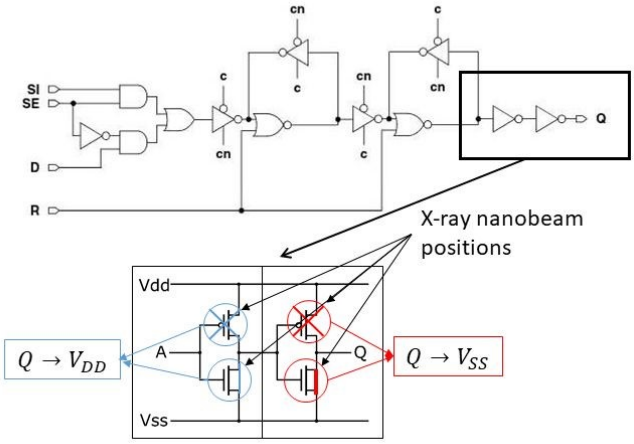

Fig. 2: Top: Schematics of the whole flip-flop of the device. Bottom: Zoom on the four transistors that were attacked in this article with the observed behavior after sufficient irradiation time.

In Block 6, the implemented SRAM cells consist of regular 6-transistor configurations. During the attacks, p-type transistors were targeted, leading to the possibility of individual SRAM cells getting stuck either at V_{DD} or V_{SS}, depending on the position of the transistor within the cell.

E. Quantitaitve analysis

Thanks to high photons flux at ESRF, single transistors can be faulted in few seconds, at different positions in the register and in the SRAM of the 28-nm technology node device. The mean number of photons needed to fault a single transistor is evaluated for each single transistor fault and the dose is calculated with SiO_2 density and absorption coefficient at the energy of 17.5 keV or 24.7 keV, depending on the X-ray energy used for the attack.

The doses calculated to fault a single transistor are presented in Fig. 3. A dose around seven times higher is required to fault

a single n-type transistor in a register than p-type transistors in a SRAM. In both architectures, a huge disparity is found between switched-off and switched-on devices (Fig. 3): when the CMOS-IC is switched-off during the attack, a dose almost 3 (8) times higher is necessary to fault a single n-type (p-type) transistor in the register (in the SRAM).

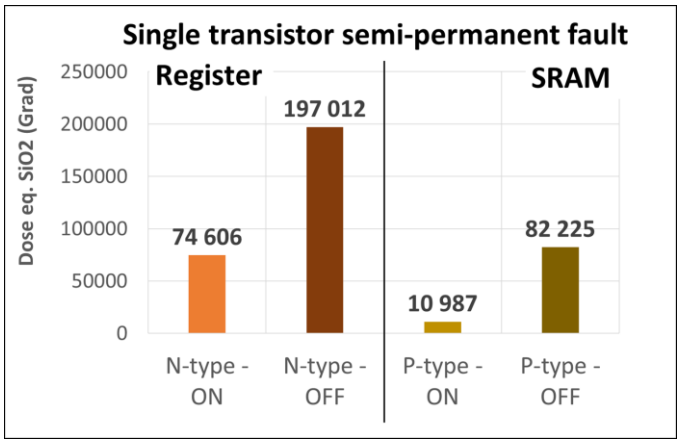

Fig. 3. Single transistors are faulted at different positions in the register (left) and in the SRAM (right). When the CMOS ICs are switched-off during the X-ray irradiation, the needed dose to fault a single transistor is quite higher than for the switched-on devices.

F. Discussion

Transistors are sensitive to radiation damage induced inside silicon (Si) and silicon oxide (SiO_2) [19], [22], [24], [25], [26], [27]. Floating-gate MOS transistors are even thought to be used as radiation sensors, even though irradiation causes degradation of electrical properties [28]. Ionizing radiations such as X-ray radiations are responsible, among others, for an increase of leakage current and charge losses at the interface Si/SiO_2, the formation of an electron-accumulation layer below the Si/SiO_2 interface and a decrease of breakdown voltage [26]. These damages are resulting from the generation of electron-hole (e-h) pairs in oxides during irradiation [19], [22], [24], [25], [28]. Auxiliary oxides such as shallow-trench-isolation (STI) and spacer oxides are thought to be responsible for Total Inoization Dos -induced performance degradation of modern CMOS-ICs [21].

In the 28-nm technology node devices irradiated at the ESRF, register and SRAM transistors are attacked in such a way that they are sustainably faulted, that is passed for n-type transistors and blocked for p-type transistors. For the first time, single n and p-type transistor semi-permanent faults are reported for such a low-size technology node. As doses are quite higher than in literature (Fig. 4), TID effects probably occurs in the gate oxide rather than in the STI and spacer oxides, even if the beam size is larger than the channel length (Table 1).

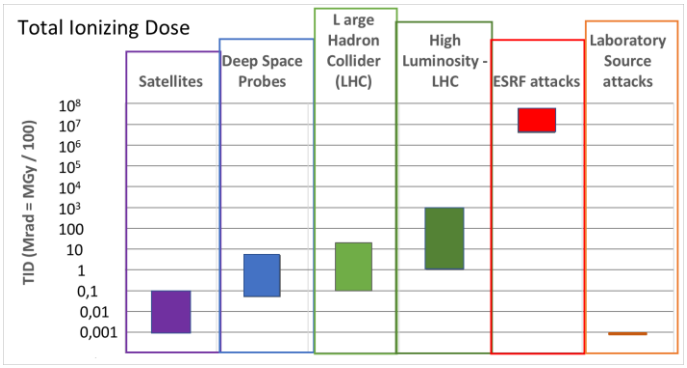

Fig. 4. Approximate radiation levels to which electronic circuits are exposed depending of applications: the ESRF and laboratory source attacks are presented in this study while the other situations are reproduced from [21].

For both register and SRAM structures, the switched-off transistors are found to be more resistant to TID effects than switched-on ones (Fig. 3). This is consistent with results from literature, which points out the importance of bias conditions during irradiation [21], [28]: if no electric field passes through the oxides, the recombination rate is maximum in oxides surrounding the attacked transistor, thus decreasing radiation-induced damages. A higher dose is thus necessary to fault a switched-off transistor.

N-type transistors attacked in a register are found to be more difficult to fault than p-type transistors attacked in the SRAM (Fig. 3). Although p-types transistors are known to be more sensible to irradiation than n-type ones [21], [24], this dose difference is also related to length (L) and width (W) differences between n and p-type transistors (able 1):

- Narrow channels (that is smaller W) are known to be more affected by TID [24]: in Fig. 5 (top graph), p-type transistors in the SRAM, which are narrower than n-type transistors in the register, are faulted with a smaller dose.
- Transistors with smaller channel length are known to be more resistant to TID [21]: in Fig. 5 (bottom graph), n-type transistors in the register, which have a smaller length than p-type transistors in the SRAM, are faulted with a much higher dose.

28 nm	W (nm)	L (nm)
Register n-type	210	30
SRAM p-type	66	40
350 nm	W (nm)	L (nm)
FLASH FG transistor	1500	350

Table 1: Length (L) and width (W) for the different attacked transistors in the different CMOS-ICs.

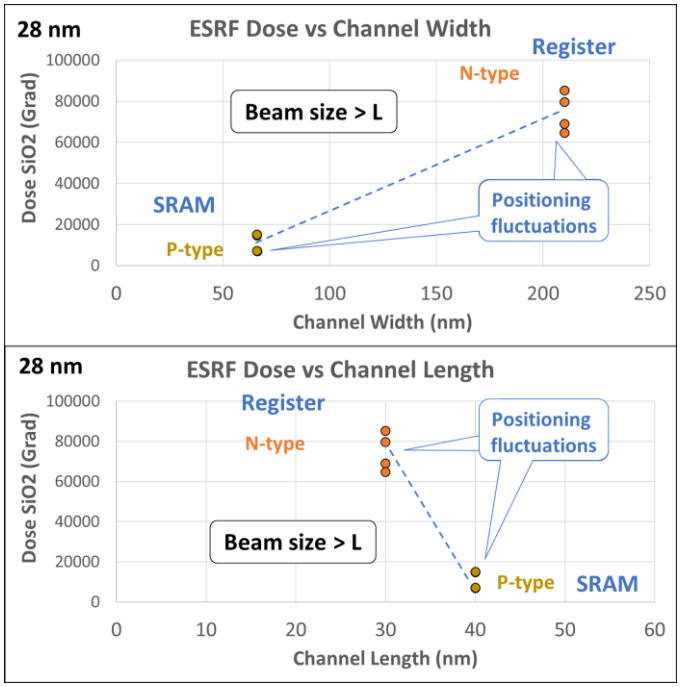

Fig. 5. Narrower channel transistors are more sensitive to TID (top graph): a smaller dose is needed to fault the smaller W transistors. When the length is smaller, transistors are more resistant to TID (bottom graph): the smaller the channel length, the higher the dose needed to fault transistors.

Circuit modifications at the single transistor level of a modern technology IC is demonstrated thanks to a very powerful X-ray nanobeam. However, for a wide dissemination of such circuit modifications, a more common and cheaper irradiation tool shall be assesed. The following part of this paper deals with the possibility to use regular laboratory X ray source for circuit modification.

III. Laboratory X-ray source IC modifications

A. Experimental details

A laboratory tomograph is used as the X-ray source. It is an "EasyTom XL Ultra 150-160 micro/nano-CT scanner" from RX-Solutions SAS (Chavanod, France). It consists of a Hamamatsu nanotube, which can be mounted either with a molybdenum target (Mo, emission line Kα at 17.5 keV) or with a tungsten target on a diamond window (W, emission lines L between 10 and 11 keV), and a LaB_6 cathode. X-ray beam emitted by the laboratory source is very divergent so a 50-µm thick lead mask with a 1-µm diameter hole is placed in front of the source to serve as a focus hole. The device under test is positioned just behind the focusing hole to benefit from the smallest possible X-ray beam diameter. Very precise piezo-inertial motors are used to control the positioning of both the CMOS-IC and the metallic mask, to ensure a perfect alignment of the source-hole-CMOS-IC assembly. With the voltage and current conditions, the X-ray energy delivered by the laboratory tomograph is roughly 6.4 keV, with a flux around 4 x 10^4 photons/s measured with a Amptek CdTe spectrometer (surface: 25 mm^2 and CdTe thickness: 1000 µm) at 75 mm from the source. With the 50-µm thick lead mask drilled with a 1-µm diameter hole, the maximum beam size has a diameter of approximately 2 µm at the sample level.

Same computer interfaces as at the ESRF are used on the laboratory source to follow the IC behavior during the attack.

B. Laboratory X-ray source attacks on a 350-nm node

CMOS-ICs with a technology node of 350 nm are attacked with the laboratory tomograph. The ATMEGA 128 P devices are attacked in their Flash memory in which there is a large number of floating-gate transistors (FG transistors). To ensure a good positioning of the hole in the lead mask, the targeted FG transistor is located relative to the gold bondings, visible both in optical microscopy and on radio images (Fig. 6).

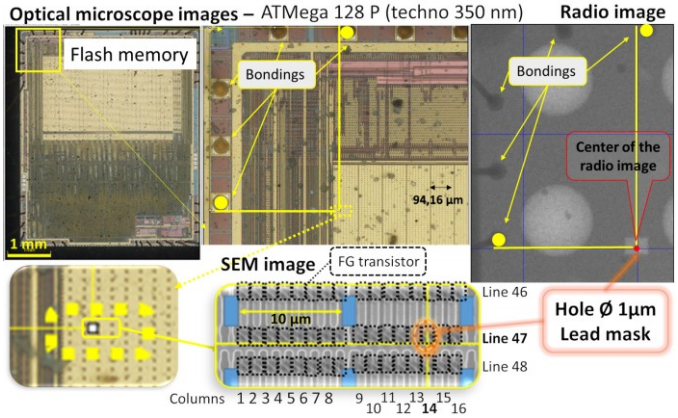

Fig. 6. Positioning technique to target a FG transistor in a 350 nm CMOS-IC, using the gold bondings visible both on the optical and on the X-ray images.

This allows the hole to be positioned exactly above a FG transistor (the one situated line 47, column 14 in Fig. 6). With this positioning technique, the targeted FG transistor is detected to be faulted at the exact expected position. Again, faults are semi-permanent and can be erased only by annealing or waiting several months at ambient temperature. The mean number of photons needed to fault a single FG transistor is evaluated for the laboratory tomograph and for the one obtained with the ESRF nano-beam earlier [14]. The calculated doses needed to fault a single transistor are shown in Fig. 7. There is a huge difference in needed doses to fault a single FG transistor between the ESRF and the laboratory source. With the laboratory source, the same kind of difference between switched-on and switched-off devices is found: when the ATmega is switched-off during the attack, a dose 2 times higher is necessary to fault a single FG transistor in the FLASH memory.

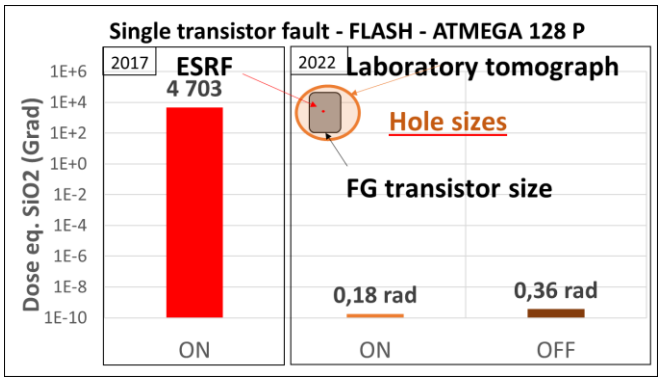

Fig. 7. Huge differences in doses needed to fault a single FG transistor inside a 350-nm technology node ATMEGA 128P are found between the ESRF |14] and the laboratory source.

C. *Discussion*

In the 350-nm technology node CMOS-ICs, semi-permanent single transistor faults are made with a controlled positioning of the attack.

Again, a higher dose level is found to fault a switched-off device compared to a switched-on one, pointing out the importance of bias conditions during irradiation, in accordance with results from literature [21], [28].

A huge difference is found in needed doses to fault a single FG transistor between the ESRF and the laboratory source. This is due to differences in irradiated surfaces (inset in Fig. 7): only a small surface of the gate oxide is irradiated at the ESRF, whereas the FG transistor gate oxide, the STI and spacer oxides are entirely in the X-ray flux with the laboratory source. The TID effects are known to be considerably increased by STI and spacer oxides [21]. The results presented here are consistent with a gate oxide TID effect at the ESRF: a much higher dose is needed at the ESRF to fault the same single FG transistor than with the laboratory source. As expected, with the laboratory source, the level of TID obtained to fault a single FG transistor is comparable to literature for FG [13] or for regular transistors [22], [24] (see also Fig. 4).

IV. Conclusion

Thanks to a 50-nm nanoprobe beam from the European Synchrotron Radiation Facility, we demonstrate the modifications of single transistors to induce semi-permanent faults, on a modern technology node: 28 nm. For the first time, a single transistor is faulted inside a 28-nm technology node CMOS-IC, both in the SRAM and in registers, with the ESRF nano-beam. Doses needed to fault a single transistor are quite higher than in literature: this can lead to the conclusion that TID effects probably occurs in the gate oxide rather than in the STI and spacer oxides. Compared to the n-type transistors inside registers, the SRAM p-type transistors are found to be more sensible to X-ray irradiation, probably due to their length and width differences. Both in SRAM and in register, when the CMOS-IC is switched-off, a higher dose is needed to fault a single transistor: when the device is off, no static field can separate e-h pairs as when the device is on, thus leading to the highest possible recombination rate and delaying TID effects.

For the first time with a laboratory source, it is possible to fault semi-permanently the exact targeted single FG transistor using a metallic mask with a 1-µm diameter hole, in the FLASH memory of a 350-nm technology node CMOS-IC. Again, a higher dose is needed to fault a single FG transistor when the device is switched-off than when it is switched-on. In these CMOS-ICs, a huge gap in doses to fault a single FG transistor is found between the laboratory source and the ESRF. With the laboratory source using a lead mask with a 1-µm diameter-focusing hole, all the FG transistor and its auxiliary STI and spacer oxides are within the X-ray flux so that TID effects are much more important than with the ESRF nano-beam, where the irradiated surface is limited to a small part of the oxide gate. Thus, with the ESRF nano-beam, gate oxide TID effects are responsible for the single FG transistor fault.

This paper demonstrates the possibility to modify a single transistor in a controlled way on a modern technology IC (28-nm). Real attacks on devices shall be demonstrated but the fundations of such an attack works out. In the same manner, if the circuit edit needs to modify a single transistor, we believe that X-ray nanoprobe can be used with a much easier and a higher success rate thanks to its non-invasive way of modification. However, the ESRF nanobeam is seldom available and still expensise. Thus, the same kind of attack were successful performed on a less demanding tool, albeit with a less aggressive techonology nodes.

Further work will try to demonstrate these single transistor faults on a 28 nm, without the use of an expensive means of modification.

Acknowledgment

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