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# A 42.24 Gb/s Channel Bonding Up-Converter with integrated multi-LO generation in 45nm CMOS

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**Abstract**—This paper presents an energy-efficient wideband V-band channel-bonding up-converter. The circuit, fabricated in 45nm CMOS RFSOI technology is composed of four lanes and an output hybrid combiner based on differential coupled lines. The circuit has four I and Q inputs and each one gets up-converter to a different channel at V-band at the output. The four required LO frequencies (58.32, 60.48, 62.64 and 64.48 GHz) are generated on-chip using high integer number frequency multiplication from a common reference input at 2.16 GHz that sets the channel spacing. Four-channel 64-QAM modulation is demonstrated with a total data rate of 42.24 Gb/s and 9.9 pJ/b.

**Keywords**— V-band, channel bonding, high data rate, 64-QAM, LO generation, CMOS 45nm

## I. INTRODUCTION

The current trend towards increasing wireless data rates (DR) driven by the requirements of 5G and future 6G networks, among others, is pushing the transceivers towards ultra-broadband architectures and the carrier frequencies towards higher frequencies in the mmW and sub-THz spectrum, such as the D-band, in the quest of more available bandwidth (BW). Therefore, in order to attain 100 Gb/s and higher DR, channel BW in the order of a few tens of GHz is required. Handling this BW from the baseband (BB) to the RF is really challenging and usually requires high power consumption. An alternative is to address separately the total required band using channel bonding architectures, as the example transmitter (TX) shown in Fig. 1. This architecture allows reducing the bandwidth of the BB interfaces and the fractional BW of most of the RF up-conversion circuitry. The first channel-bonding and up-conversion step in this architecture is implemented by a multi-channel circuit operating at V-band band that is the goal of this work. Wideband transceivers at 60 GHz have been proposed in the recent years [1]-[6] mainly driven by IEEE 802.11.ad and 802.11.ay standards. These circuits could be suitable also as the first up-conversion stage of the architecture in Fig. 1 but most of them are built using a single large BW BB interface ([2], [5], [6]) or the multiple channels used are connected to separate outputs ([1],[3],[4]).

In this work, it is presented a multi-channel TX circuit composed of four up-conversions lanes from BB up to four adjacent channels around 61.56 GHz integrating a 4-ways output combiner. Conversely to previous works, the whole band composed of four 2.16 GHz spaced channels is provided at a single output. The circuit includes four LO generators based on high-order integer-N frequency multiplication, all obtained from a lower input reference frequency that sets the channel spacing. The aim of this circuit is to use low sampling frequency (2..3 GS/s) digitizers on the digital baseband processor (DBB) unit to save power.

## II. CIRCUIT DESCRIPTION

The overall block diagram of the proposed circuit is highlighted in Fig. 1. The architecture used for each of the four lanes is shown in Fig. 2. The main building blocks are described in the following.

### A. LO generation

The four LO signals required are generated using the integer frequency multiplication technique described in [8]. Each LO generator is composed of a pulsed oscillator followed by a couple of injection locked oscillators used as active-regenerative filters to reduce adjacent channel LO spurs. Each stage is separated by buffers. Four LO frequencies are generated: 58.32, 60.48, 62.64 and 64.48 GHz. All four generators use the same input REF IN that is set to 2.16 GHz and 0 dBm.

### B. Up-conversion section

The I and Q BB inputs of each up-conversion lane are fed to a couple of differential active 2<sup>nd</sup> order low-pass filters based on biquad Tow-Thomas architecture with controllable gain as shown in Fig. 2. The BB signals are up-converted to 60 GHz band using an I/Q mixer. The different phases of the

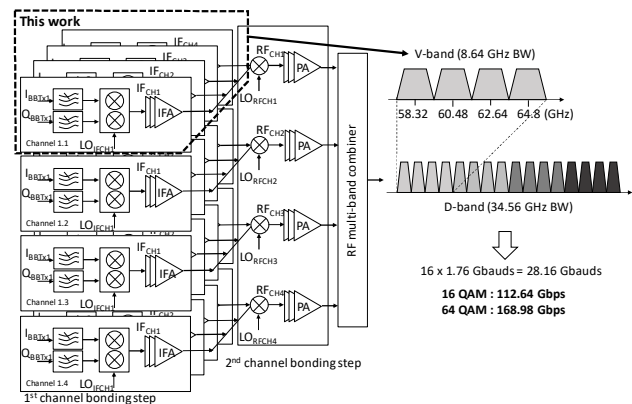


Fig. 1 Ultra broadband channel bonding TX architecture.

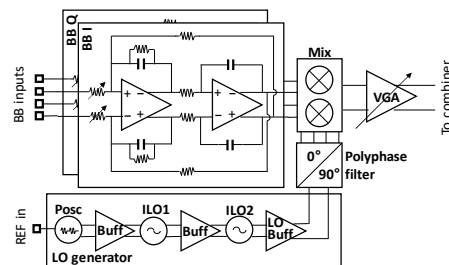


Fig. 2 Block diagram of one of the four up-conversion lanes of the IC.

LO for each mixer are generated from the differential LO signal using a polyphaser filter. The mixers are coupled to the next stage by transformer loads. The output of the mixer is amplified with a variable gain amplifier (VGA) implemented using a common source pseudo-differential stage with switchable cascode transistors. The BB filter has two steps of 4.5 dB of gain each (three gain states), whereas the VGA offers 3 steps of 2 dB each (four gain states), resulting in a total of 15 dB of gain control for each of the up-converter lanes.

### C. Output combiner

The outputs of the four lanes, each one covering a different frequency channel at 60 GHz are combined using a 4-ways hybrid implemented with differential coupled lines, as shown in Fig. 3. The optimal differential impedance of the lines is found to be 60 Ohms. Therefore, some of the open ports are terminated with a couple of 30 Ohms resistors, and the others are connected to the differential output of the VGA of each lane. The output port is transformed to single-ended mode using a transformer terminated with a stub to match the output to 50 Ohms. Due to the different linear length between each input port and the output, the insertion losses vary depending on the inputs, and are simulated to be 8.7, 8.3, 7.9, and 7.2 dB for channels inputs 1 to 4, respectively.

## III. EXPERIMENTAL RESULTS

The four channels up-converter is implemented using a 45nm RFSOI technology and has an area of  $2 \times 3.5 \text{ mm}^2$  (see Fig. 4). The circuit has C4  $\mu$ bumps and is flip-chipped on a test board as shown in the inset of Fig. 5. The output is available through an end launch connector that along with the output line introduces around 4 dB of loss in the band.

### A. LO generation

In order to observe the LOs at the output of the circuit, the I and Q DC offset is intentionally unbalanced. The results are shown in Fig. 6 where the four LO frequencies, each one corresponding to one of the BB lanes, are observed at the output. The figure also shows the phase noise as measured on these signals achieving -100 dBc/Hz and better phase noise @ 1 MHz frequency offset for all four LO signals.

### B. Continuous wave measurements

Continuous wave (CW) test results are shown in Fig 7. The left panel shows normalized output power for both USB and LSB tones for varying input BB signal frequency, for the three gain steps that can be configured at BB. The filter cut-off frequency is 900 MHz, resulting in rejection at the adjacent channel better than 30 dB, which is enough to suppress the signal replicas generated by the DBB DACs. Figure 9, right shows output power and gain (after embedding input and output losses) for one of the channels of the up converter as a function of the BB input power. Since this circuit is intended to be used as the input stage of a higher frequency channel bonding TX as shown in Fig. 1, the output stage has been sized to deliver a power level compatible with the input 1dB compression point of that circuit, including some back off. This corresponds to a power per channel of -22 dBm resulting in a total  $P_{OUT}$  for the four channels signal of -16 dBm at the maximum gain setting. The figure shows the power level and gain of other VGA

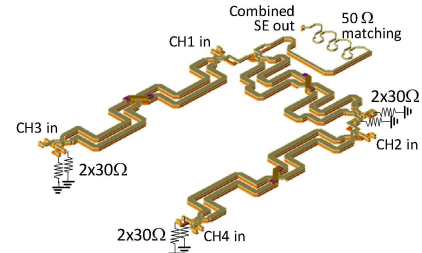


Fig. 3 4-ways differential hybrid combiner.

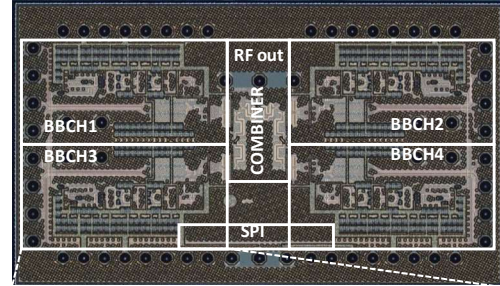


Fig. 4 IC microphotograph with zoomed detail of one of the lanes.

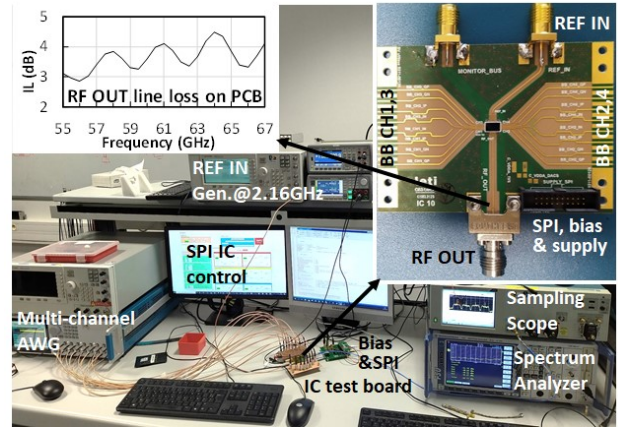


Fig. 5 Experimental set-up and details of the IC tes board.

gain settings as well. Figure 8, left shows the measured gain for a single tone frequency sweep in all the four BB inputs. The gain of all lanes is set to maximum. The different lanes provide a different gain to the output mainly due to the different IL of the 4-way combiner. Channel-to-channel leakage has been measured to be less than 30 dBc.

### C. Modulated signal tests

Four I/Q differential BB signals are generated using a multi-channel arbitrary waveform generator (AWG) as shown in Fig. 5. The sampling frequency is set to 2.5 GS/s and each BB signal is modulated with a baud rate of 1.76 Gbauds. The I and Q differential outputs of the AWG are connected to the IC inputs through the connection board shown in Fig. 5. The total BB losses are measured to be 1.8 dB per single ended channel. The output of the circuit is digitized using a 75 GHz BW, 200 GS/s sampling scope. An off-line DBB receiver is implemented in Matlab. It retrieves the samples from the scope and demodulates the signals providing metrics such a BER and EVM. Figure 8 right shows one example of output signal in the time domain, as sampled by the scope, and its spectrum. Compared to the left figure, the output level of the different lanes has been equalized using the gain control capabilities. The four

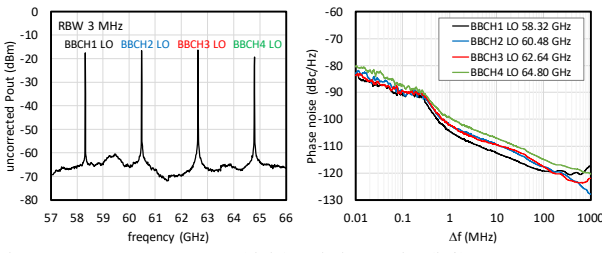


Fig. 6 LO generators output (right) and phase noise (left).

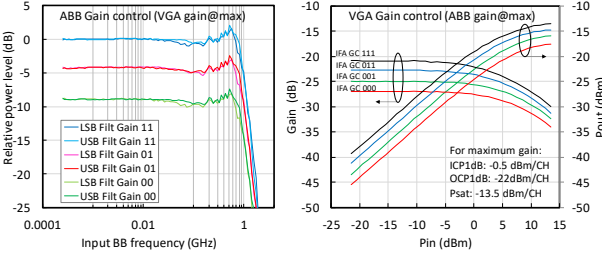


Fig. 7 CW results for one of the lanes (CH3) of the up-converter IC.

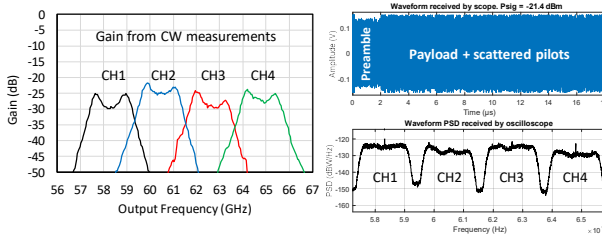


Fig. 8 CW gain for all four channels (left) and outut signal for modulated BB inputs (right).

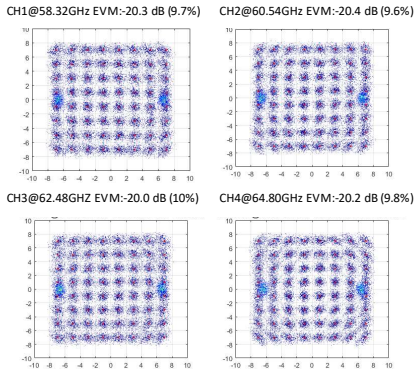


Fig. 9 Output 64-QAM constellations for 4x1.76 Gbauds/CH.

constellations obtained for 64-QAM modulated input BB

signals are shown in Fig. 9 as measured from the output signal. EVM is equal to or better than 10% for all channels.

#### IV. DISCUSSION AND CONCLUSIONS

In this work a four-channel BB to V-band up-converter is demonstrated. To the best of the author's knowledge, it is the first time a full channel-bonding transmitter with integrated multi-LO generation and wideband output combiner is presented. Compared to previous works [2]-[7] (see Table I) it is the one combining the largest number of input BB channels with the lowest BB bandwidth (1.18 GHz in I and Q), requiring lower sampling frequency and therefore leading to lower power consumption for the digital BB interfaces. Its energy efficiency (9.9 pJ/b) is one of the lowest in the literature, and is only outperformed by [3] and [6] that require a much larger BB BW, and therefore higher energy consumption for the digital interface, and [5] that implements a digital polar TX but on separate output channels and without including the LO generation. A total data rate 42.24 Gb/s is demonstrated in a single output at V-band for four channel carrying 1.76 Gbauds, 64-QAM modulated signals each. This circuit is intended as the first channel bonding and up-conversion stage of a higher frequency TX but it is suitable as well for IEEE 802.11ay standard if combined with an external V-band power amplifier.

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TABLE I. COMPARISON WITH THE STATE OF THE ART

Ref	Datarate (Gb/s)	Modulation	# BB ch.	BB BW/ch. (GHz)	P <sub>OUT</sub> (dBm)	Integrated LO gen./Out combiner	P <sub>DC</sub> (mW)	P <sub>DC</sub> /Tx lane (mW)	Energy cons. (pJ/b)
[2]	3	ASK	3	2.16	5	Yes/No	153	51	51
[3]	28.16	16-QAM	1	2.16	4	Yes/No	251	251	8.9
[4]	42.24	64-QAM	2	42.24	7	Yes/No	544	272	12.9
[5]	27.8	16-QAM	2	27.8	n.a.	No/No	210	105	7.6
[6]	50.1	64-QAM	1	50.1	7.3	Yes/No	169	169	3.4
[7]	4.6	16-QAM	1	4.6	12.5 <sup>a</sup>	Yes/No	230	230	50
<b>This work</b>	<b>42.24</b>	<b>64-QAM</b>	<b>4</b>	<b>2.16</b>	<b>-16</b>	<b>Yes/Yes</b>	<b>420</b>	<b>105</b>	<b>9.9</b>