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***Abstract*—Limit your abstract to one paragraph and keep it short. In the Keywords section, include a few keywords from: http://www.ieee.org/organizations/pubs/ani_prod/keywrd98.txt**

***Keywords*—ceramics, coaxial resonators, delay filters, delay lines, power amplifiers.**

I. Introduction

Wireless transmitters for high-data rate wireless links are receiving increasing interest as building blocks for the next generation communication network [1]-[5]. Most of them target the D-band due to the large bandwidth (BW) available at those frequencies. However, these architectures have to face challenging trade-offs between power consumption, occupied bandwidth, and transmitted power due to the high path loss and the feasible modulation schemes that can be used for large-band channels, which is usually limited to 4 or 6 bits/Hz.

This work presents a wireless link system demonstration based on a wide-band channel bonding transmitter chipset combined with a high-gain antenna. Channel bonding (or channel aggregation as defined in [1]) is selected for the up-converter architecture from baseband (BB) to the D-band because this approach allows to optimize the signal fractional bandwidth at each frequency conversion step without limiting the total emitted signal band. This allows to reduce the power consumption at all system levels, including the digital interfaces.

The developed transmitter covers a band of 17.3 GHz by up-converting 8 baseband channels of 2.16 GHz each. It is based on two different 45nm CMOS integrated circuits (ICs). The first one performs a four channel up-conversion and channel aggregation from I/Q BB up to an intermediate frequency (IF) band around 61.56 GHz,The second IC is a two channels up-conversion and channel bonding D-band transmitter. The channel bonding operation at IF is implement on-chip using a passive hybrid 4-ways combiner whereas the channel bonding operation at D-band is realized over-the-air through the antenna. The antenna is based on a transmitarray planar lens illuminated by a two-port source antenna implemented in the same module than the D-band IC and fabrication using low-cost printed-circuit board (PCB) technology. The combination of all these elements allow to implement a 57.6 Gb/s wireless link over 42 cm by sending 16-QAM modulation with 1.8 Gbaud per baseband channel with low energy consumption (27.4 pJ/b). The link is demonstrated with a commercial D-band receiver inside a hardware-in-the-loop full system level validation platform.

II. Transmitter Architecture and Building Blocks

The transmitter is composed of two units of the BB to IF up-converter connected to the two-channel IF to D-band TX IC, as shown in Fig. 1.

A. Baseband to IF channel bonding TX

The BB to IF up-converter and channel bonding IC (see Fig. 2) is composed of four similar lanes each one taking one I/Q differential BB input. Each lane includes a 2nd order filter, an I/Q up-conversion mixer and and IF amplifier. They also and include a local oscillator (LO) generator unit each. The four LO frequencies are set to 58.32, 60.48, 62.64, 64.8 GHz so the four BB channels get up-converter to adjacent channels at IF around 61.56 GHz. The outputs of the four lanes are combined using an on-chip passive 4-ways hybrid that has 8 dB of average losses across the IF band with ±1 dB of channel-to-channel variation. The IC is flipchiped on a connectorized board as

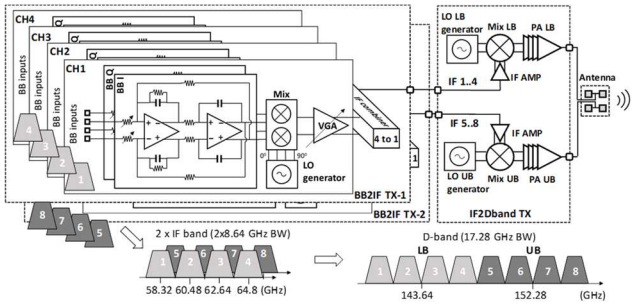

Fig. 1. Transmitter module block diagram composed of 2 units of BB to IF up-converters and an IF to D-band transmitter feeding a two-port source antenna.

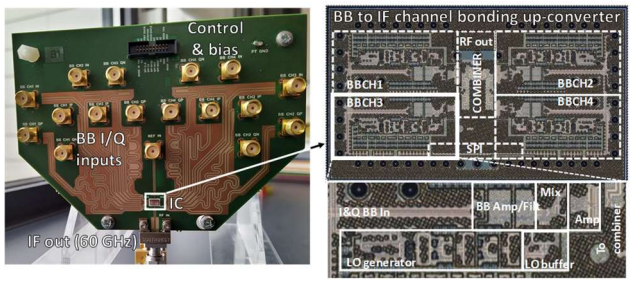

Fig. 2. BB to IF up converter board and IC photograph.

shown in Fig. 2. It is fabricated in 45nm CMOS SOI technology and occupies an area of 2×3.5 mm^2. It consumes 495 mW of power from a 1V supply. The maximum gain from any of the BB inputs (I or Q) to the combined output is -26.5 dB. This gain includes 1.5 dB of losses in the input BB connections and board traces and 4 dB on the IF output trace and connector. Each lane has 9 and 6 dB of programmable gain variation at the BB filters and IF amplifier, respectively. The output compression point for the maximum gain is -22 dBm per channel. Please note that when all channel are combined the total output power is 6 dB higher. The gain value is designed to account for large dynamic range at the BB input (in the range of a few hundreds of mV) and low enough IF power for not saturating the D-band transmitter.

One of the main limitations of channel bonding architectures is the channel to channel interference. They can caused basically to two mechanisms. First of all, the LO spurs at adjacent channel frequencies produce some leakage from channel to channel. The spurs are due to the LO generator architecture that is based in frequency multiplication as in [6]. In the case of the proposed transceiver, this LO leakage meachanism has been measured to be less than -30 dBc in any of the channels as shown in Fig. 3a. Secondly, the Nyquist replicas of the BB signals may fall on the adjacent channel. Fig. 2 shows the IF output spectrum for 1.8 Gbauds modulated BB signal inputs. They are generated using a multi-channel AWG with a sampling rate of 2.5 GS/s (please note that each I and Q BB signals has a BW of 900 MHz). The 2nd order filter of each lane filters out some of the replicas, but does not completely eliminate them, as shown in Fig. 3c. The signal to interferer ratio (SIR) between the wanted channel and the replicas is measured to be 20 dB in the worst case (e.g by comparing Fig. 2b and 2c for CH1 and CH2). That SIR is enough for 16-QAM but is limiting for 64-QAM. This limitation can be easily overcome in future versions of the IC by increasing the filter order.

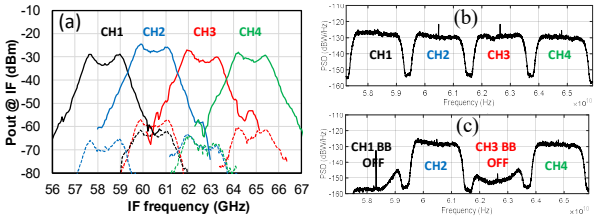

Fig. 3. (a) Single tone characterization of the BB to IF Tx. The continuous line are the main response for each BB channel input and the dashed lines the leakage to adjacent channels due to LO spurs. (b) Typical IF output signal for modulated BB inputs when all BB inputs are ON and (c) when only CH2 and CH4 BB inputs are ON.

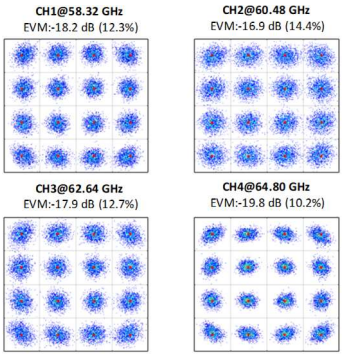

Fig. 4. IF output constellations for 16-QAM, 1.8 Gbauds BB inputs. IF signal power is -24 dBm.

B. *IF to D-band channel bonding TX*

The IF to D-band up-conversion and emission is implemented by a two-channel TX module based on [7]. Each IF lane is composed of an IF amplifier, an up-conversion mixer and a power amplifier (PA). In the fabricated IC prototype, both IF signals are taken from the same connector and then splinted on-chip for simplicity. The LO signals for each lane are generated on-chip using the same frequency multiplication technique of [6] with frequencies 82.08 and 90.72 GHz, respectively. The D-band TX brings each of the IF input signals to adjacent sub-bands (LB and UB) located at 143.34 and 152.28 GHz, respectively, covering a frequency span of 17.28 GHz. The two bands are provided at separated outputs and connected to a two ports, 2×2 patch antenna implemented in the same PCB board where the IC is flip-chipped as shown in Fig. 6. This antenna serves as the focal plane source for a transmitarray (TA) planar lens that implements passive beamforming in the boresight direction as also shown in the figure. The TA is similar to [8]. The measured antenna gain is 25 dBi with a very wideband response from 139 to 159 GHz. The antenna also implements over-the-air power combining by radiating in the broadside direction both sub-bands. The measured 1dB compression point EIRP of the D-band TX module is shown in Fig. 6a. An average of 26.5 dBm is radiated across the full band.

III. D-BAND LINK AND OVER THE AIR TESTS

A point-to-point link is implemented using a commercial receiver (Rx) with 4 and 8 dB of average gain and NF (see Fig. 6b). It is completed with a 20 dBi standard horn antenna.

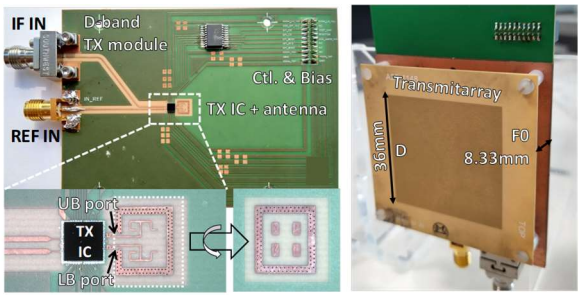

Fig. 5. D-band TX module and antenna.

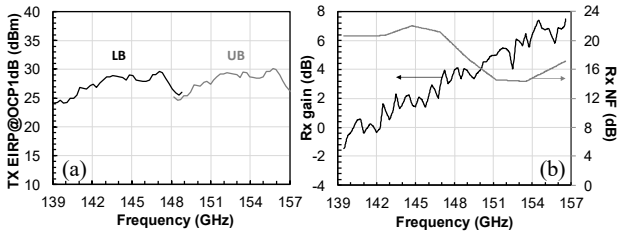

Fig. 6. (a) EIRP at the 1dBCP of the D-band TX module. (b) Measured gain and noise figure of the commercial Rx.

The maximum link distance is calculated taking into account the 1dBCP EIRP than can be radiated by the TX and a back-off of 10 dB. Such a large back-off is necessary for multi-channel modulated signals since the combined time-domain multi-channel signal has larger peak-to-average ratio than the individual channel signals. The target BER is 10^{-2} takin into account that acceptable packet error rates can be achieved once a suitable forward error correction (FEC) code is applied [9]. Taking this into account the link budget calculation shown in Table 1 can be stablished resulting in a RX SNR of 21 dB for 42 cm link range. Some margin is left for other contributions to the error vector magnitude (EVM) that should be of -14 dB for the target BER and 16 QAM modulation.

Next the TX and RX and mounted on plastic supports and connected to lab equipment in order to implement a full baseband to baseband link as shown in Fig. 7. The digital baseband (DBB) section of the TX is implemented using a multi-channel arbitrary waveform generator (AWG). Each one of the four BB I and Q differential input signals is generated using a sampling frequency of 2.5 GS/s. The baud rate is 1.8 Gbauds and a 0.18 root rised cosine digital filter is used at the last stage of the DBB TX. Each BB channel signal is organized in a frame with 50 symbols each one compose of 512 samples (this corresponds to the FFT length) and preceded by a preamble with QPSK modulation used on the RX DBB for channel, carrier frequency offset (CFO) estimation and I/Q imbalance estimation and correction. The payload includes BPSK modulated scattered pilots (not shown in the constellation results) used for slow phase variations tracking at the RX DBB. The two channel bonding TX boards are connected using V-band connectors and a waveguide to minimize the losses. In some experiments a V-band LNA followed by a mechanical attenuator are used to sweep the IF signal power level at the input of the D-band TX.

The RX, which consist on a wideband down-converter mixer, is placed at 42 cm from the TX TA. The LO used or the RX and the reference generator used for the internal LO generators of the TX are not synchronized. The RX provides a down-converted signal on the band DC to 20 GHz. This signal is sent to a 50 GS/s sampling scope for digitization and next read by the RX DBB. Both the TX and RX DBB are implemented in Matlab. The AWG generates continuously a train of frames of 18 µs of duration spaced by 2 µs at each BB output. The scope triggers on the rising section of the frames preambles received at the RX and sends the data to the Matlab DBB RX that performs off-line demodulation and parameters extractions (signal power, EVM, BER, residual I/Q and CFO mismatch calculations, etc.)

Some results of received signals are shown in Fig. 8 and Fig. 9. They correspond to the IF signal shown in Fig. 4. The RX signal power values indicated in the figures are in average 4 dB weaker at the RX antenna aperture once the RX gain shown in Fig. 6b is subtracted. The signal power for the different channel varies in part due to the frequency response of

Table 1. Link budget analysis.

Parameter	Per channel	Full band
BW (GHz)	2.16	IF: 2×4×2.16 RF 8×2.16
BB I or Q diff. peak amp. (mV @ 100 Ω)	750	
BB I or Q rms amp. (mV @ 100 Ω)	270	
BB to IF up-converter gain (dB)	-29	
IF signal power (dBm)	-30.4	-24.4 (×2)
D-band TX gain (dB)	37	
EIRP@1dBCP (dBm)	16.4	25.4
Back-off (dB)	10	
EIRP for IF power (dBm)	7.4	16.4
Path Loss @ 42 cm (dB)	68.4	
Rx antenna gain (dBi)	20	
Rx NF (dB)	18	
Rx Signal @ antenna aperture (dBm)	-41	-32
Rx Noise @ antenna aperture (dBm)	-62	-53
SNR	21	
Margin for BER 10^{-2} on 16-QAM (dB)	7	

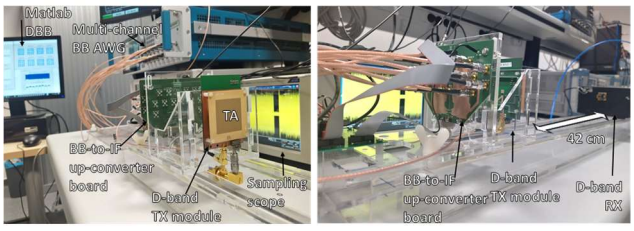

Fig. 7. Point-to-point D-band link set-up.

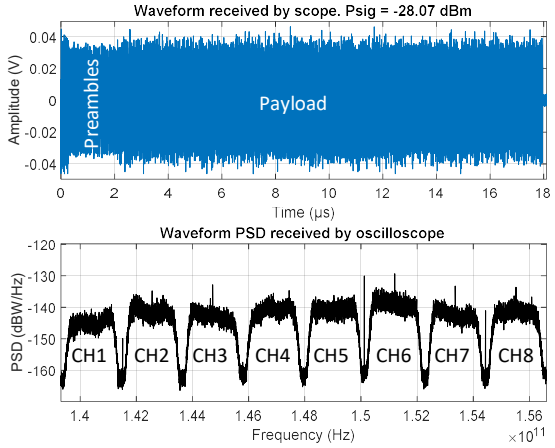

Fig. 8. RX signal in time and frequency domain.

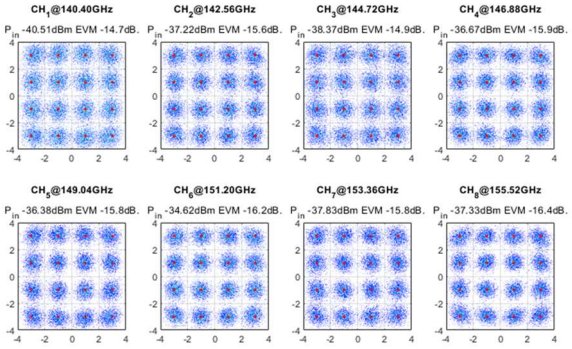

Fig. 9. RX 16-QAM constellation for 1.8 Gbauds.

Table 2. Performance comparison of recent D-band transmitters integrated with antenna systems.

Ref.	[3] TMTT'22	[4] ISSCC'22	[5] JSSC'22	**This Work**
Package Technology	LTCC Interposer	Radio on PCB	Radio on PCB	**Radio on PCB**
ICs Technology	22nm FDSOI + 0.25 InP HBT	130nm SiGe BiCMOS	45nm RFSOI	**45nm RFSOI**
Tx architecture	Single channel BB to D-band direct conversion External LO@15 GHz	2x2 Channels RF Beamformer	2x4 RF Front-end + IF Beamformer External LO@22 GHz	**BB-to-IF multi-channel upconverter + channel bonding RF Front-end with integrated LO generation**
Antenna system and gain (if applicable)	Antenna on LTCC (linear 8 patch array) 12 dBi	Antenna on Glass (2x2 patch array)	Quartz Superstrate (2x8 patch array)	**Antenna on PCB (2x2 patch)+ Transmit Array on PCB 25 dBi**
Frequency (GHz)	131-137	130-150,150-165	136-147	**140-158**
EIRP@1dBCP*/Psat** (dBm)	27.5**	18**	17.5*	**26.4***
#Channels × Ch. BW (GHz)	1 × 6	1 × 6	1 × 3	**8 × 2.6**
Tx Pdc (mW)	760	1060	1848	**1580**
Peak data rate (Gb/s)/Modulation	30 (64-QAM)	30 (64-QAM)	10.5 (64-QAM)	**57.6 (16-QAM)**
EIRP @ Peak data rate (dBm)	21	8	10.5	**16.4**
Link distance (cm)	15	NA	65	**42**
Link efficiency (pJ/bit/m)	168	NA	271	**65**

the TX module (see Fig. 6a) and in part due to the frequency dependent gain of the RX. The BB to IF controllable gain is set differently for each channel on the first TX IC in order to obtain a uniform channel power at IF, but there is no per channel gain control on the D-band TX IC that allows for compensating the D-band components frequency response. Nevertheless the RX DBB measured channel power varies less than ±2 dB among channels, with the exception of CH1 that is affected more severely by the drop of the RX downconverter gain. The EVM is all channels is better than -14 dBm. For the signals of Fig. 9, the overall BER measured by the DBB is 6×10^{-3}, confirming the link budget analysis of Table 1.

Note that there is some LO peaks observed in the center of the channels (also in Fig. 4). They are due to residual DC-offset on the I and Q signals of the BB to IF up converter lanes that results in some LO leakage. The large spur between CH5 and CH6 is an artifact of the commercial down-converter RX mixer.

IV. Discussion and Conclusion

The presented TX chipset and module is compare with other recent D-band transmitters, most of them also having been demonstrated with over-the-air measurements. The work of [3] presents and interesting combination of CMOS TX with external InP PA to increase the output power. The energy efficiency is comparable to our work but they are not fully exploiting the large band available at D-band since they use a single 6 GHz channel. The works of [4] and [5] also use relatively narrow band and their energy consumption is larger because they implement phased arrays. The transmitter proposed in this work offers the larger data-rate among the other recent works as well as the best link efficiency of 65 pJ/b/m leveraging on high-gain, low cost antenna based on a transmitarray and wide-band, energy efficient channel bonding architectures. Furthermore, the channel bonding architecture enables to implement adaptable transceivers because some lanes can be switched off, including the digital signal processing and interfaces, if the peak data-rate is not required. This allows to scale the power consumption with the data-rate and keep a nearly constant energy efficiency, conversely to the other full-band, single channel architectures such as [1]-[5].

The main drawback of the proposed approach is that the fixed beam TA does not allows for beam-steering. This limitation can be overcome by using controllable transmit arrays based on recent developments such as [10].

References

[1] Dascurcu *et al*., "A 60GHz Phased Array Transceiver Chipset in 45nm RF SOI Featuring Channel Aggregation Using HRM-Based Frequency Interleaving," *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2022, pp. 67-70.

[2] S. Callender *et al*., "A Fully Integrated 160-Gb/s D-Band Transmitter Achieving 1.1-pJ/b Efficiency in 22-nm FinFET," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3582-3598, Dec. 2022.

[3] A. A. Farid *et al*., "A Fully Packaged 135-GHz Multiuser MIMO Transmitter Array Tile for Wireless Communications," in IEEE Transactions on Microwave Theory and Techniques, vol. 70, no. 7, pp. 3396-3405, July 2022.

[4] M. Elkhouly *et al*., "Fully Integrated 2D Scalable TX/RX Chipset for D-Band Phased-Array-on-Glass Modules," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, 2022, pp. 76-78.

[5] S. Li *et al*., "An Eight-Element 136–147 GHz Wafer-Scale Phased-Array Transmitter With 32 dBm Peak EIRP and >16 Gbps 16QAM and 64QAM Operation," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 6, pp. 1635-1648, June 2022.

[6] A. Siligaris *et al*., "A Multichannel Programmable High Order Frequency Multiplier for Channel Bonding and Full Duplex Transceivers at 60 GHz Band," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2020, pp. 259-262.

[7] A. Hamani *et al*., "A 56.32 Gb/s 16-QAM D-band Wireless Link using RX-TX Systems- in-Package with Integrated Multi-LO Generators in 45nm RFSOI," *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2022, pp. 75-78.

[8] J. L. Gonzalez-Jimenez, *et al*., "A D-band high-gain antenna module combining an in-package active feed and a flat discrete lens," in *Proc. 52nd Eur. Microw. Conf. (EuMC)*, pp. 784-787, Sept. 2022.

[9] T. T. Nguyen-Ly, et al., "Analysis and Design of Cost-Effective, High-Throughput LDPC Decoders," in *IEEE Tr. on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 3, pp. 508-521, March 2018.

[10] Venkatesh et al., "A high-speed programmable and scalable terahertz holographic metasurface based on tiled CMOS chips".in *Nature Electrononics*, vol. 3, pp. 785–793, 2020.