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Disruptive TRX Design for the D-band

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Cédric Dehos, Fabrice Chaix, Pierre Courouve, Guillaume Robe,
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and Nicolas Cassiau

Abstract—This paper presents an architecture for broadband wireless transceivers operating in the D-band with the aim of covering tens of GHz of band over the air with a limited bandwidth per channel at the baseband. The main idea is to combine several baseband channels in a multi-channel radio-frequency (RF) signal. This is in contrast with the more conventional trend of using a single channel from baseband (or intermediate frequency) to RF. In this work, the main challenges introduced by this type of broadband channel bonding architecture are analyzed and some solutions are provided. A prototype implementation in CMOS 45 nm RFSOI technology and low cost PCB technology is used to illustrate the potentialities of this disruptive approach.

Index Terms—xxx.

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I. INTRODUCTION

IN the race to increase the wireless data rate to satisfy the growing demand in connectivity and capacity of current and future communication systems and networks, the D-band, located between 110 and 170 GHz, is becoming a strong candidate as the first wireless frequency band able to offer throughputs that are competitive with optical fiber communications. The goal is to be able to provide a data-rate of 100 Gb/s or higher at distances up to a few hundreds of meters, which are common requirements of fronthaul/backhaul links for 5G and beyond 5G networks [1,2]. Other applications include shorter distance links for kiosk or docking fast downloading and medium distance links to replace cables in a data center or even guided links using dielectric waveguides to connect the baseband unit to the remote radio head at the mobile network or fixed wireless internet access points [3].

In this context, maximizing the spectral and energy efficiencies are key objectives. The maximum data rate that can be achieved by a wireless link is ultimately limited by the available bandwidth (BW) and the noise according to the Shannon capacity limit [4]. Figure 1 shows the maximum attainable data rate for a set of

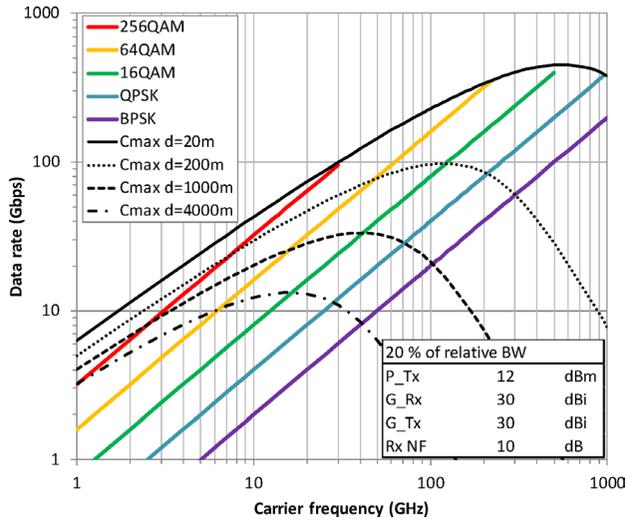


Fig. 1. Maximum link data rate as a function of carrier frequency according to the Shannon capacity limit for a 20% fractional bandwidth channel.

reasonable link parameters shown in the figure inset. In this figure, a reasonable fractional BW of 20% is considered for all carrier frequencies. The figure compares the maximum capacity of the channel for different modulation schemes. Interestingly, the peak capacity is achieved for 16-QAM at different distances and carrier frequencies. It is worth noting that 100 Gb/s can be achieved at 200 m using 16-QAM modulation. Therefore, a BW in the order of a few tens of GHz is required to achieve the 100 Gb/s data rate.

In this work, channel bonding architectures are proposed as an energy efficient alternative to conventional broadband single channel transceivers operating at the D-band. They support tens of GHz of RF BW but with much smaller baseband (BB) BW than other competing approaches. Section 2 introduces the proposed channel bonding – or channel aggregation – architecture as well as the main challenges. Section 3 presents some examples of implementation of the proposed transceiver architectures. Section 4 covers experimental point-to-point links results

and the conclusions of this work and perspectives are summed up in Section 5.

II. CHANNEL BONDING TRANSCEIVERS

The basic idea behind the proposed architecture consists of building the wide-band signal sent over the air by combining multiple narrower band channels. This principle is illustrated in Figure 2, where a total RF BW of 34.56 GHz is obtained by combining 16 channels of 2.16 GHz band each. The figure shows the transmitter (TX) section; the receiver (RX) is just a mirror version. Instead of bringing the 16 channels directly from BB to RF band, a two-step up-conversion scheme is preferred. It allows reducing the number of required local oscillator (LO) signals. Indeed, by grouping the BB channels in bundles of four channels and implementing a first up-conversion to intermediate frequency (IF), only four LOs are required, assuming all bundles of four BB channels share the same IF. Next, the four IF signals (containing four BB chan-

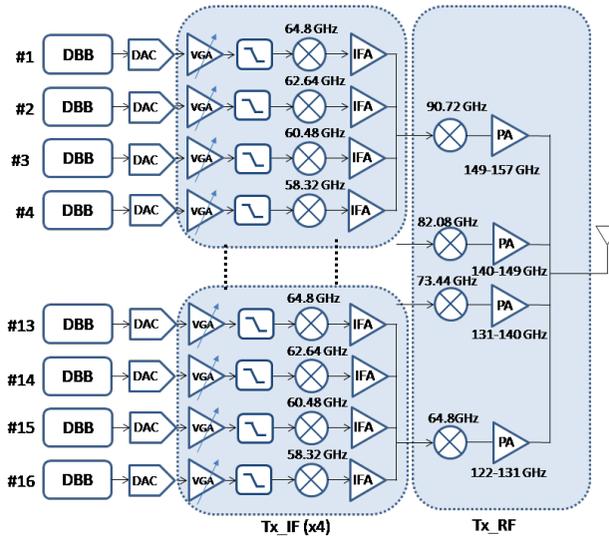


Fig. 2. Channel bonding TX architecture.

nels each) are converted to four different sub-bands at RF. This requires four additional LO frequencies. In this way, the up-conversion of the 16 BB channels only requires eight LO signals.

The careful selection of the frequency plan allows for a further property of the proposed transceiver architecture shown in Figure 2. All LO frequencies are integer multiples of the same number, 2.16 GHz, which corresponds to the channel spacing. This allows generating all LO signals using integer-N frequency multiplication [5] from the same common input reference. This technique has been proved to be very effective in generating multiple LO signals with adjacent channels spurs smaller than -25 dBc [6,7]. This feature is important since channel-to-channel interference in this type of transceivers should be kept below -20 dBc in order to enable a good enough signal to interference plus noise ratio (SINR) for high order modulations such as 16-QAM or 64-QAM [8]. Phase noise (PN) is also a limiting factor for high order modulations. The investigation of [8] indicates that the PN at 1 MHz

offset from the carrier and the noise floor should be better than -98 dBc/Hz and -120 dBc/Hz, respectively, in order to degrade the SINR by less than 1.5 dB.

One additional challenge for this type of architecture is the way the different channel bonding operations are performed. In the proposed architecture shown in Figure 2, two channel bonding operations need to be realized. The first one happens at IF (V-band) and in the implementation of [9] it is realized using an on-chip hybrid coupler at the expenses of around 9 dB of insertion losses. The second one is done at RF (D-band) and several options are possible, such as on-chip [10], in-package [11], or over the air power combining [12]. From all these options, over-the-air power combining is the most power-efficient, as shown in [12].

III. CHANNEL BONDING TX AND RX EXAMPLES

Several implementation examples of channel bonding TX and RX modules and circuits are presented in the next sub-

sections. They are used in the point-to-point link experiments presented in Section 4.

Baseband to IF up-converter

The first implementation example corresponds to the first up-conversion and channel aggregation step of the TX architecture in Figure 2. This circuit is used to generate each one of the IF signal four-channel bundles described in Section 2. The circuit block diagram and micro-photograph is shown in Figure 3. It constitutes four lanes with the same structure. Each lane contains an LO generator and a I/Q up-converter composed of a couple of I and Q active filters, an I/Q mixer and a voltage controlled amplifier (VGA). The output of each lane contains the corresponding BB channels up-converted to a different channel at the IF band, as shown in Figure 3. The four lane outputs are combined on-chip using a differential hybrid coupler. More circuit details can be found in [9]. The circuit is fabricated using a 45 nm RFSOI process and consumes 475 mW from a 1 V supply, occupying an area of $2 \times 3.5 \text{ mm}^2$.

IF to D-band TX and RX modules

A first version of a two-channel TX and RX D-band circuit was implemented in 45 nm RFSOI technology. The block diagram, circuit microphotographs and module boards, including the antennas, are shown in Figure 4. The TX realizes the up-conversion and channel bonding operation for the two uppermost D-band sub-channels of the transmitter shown in Figure 2. The two IF signals are taken from the same circuit input for testing simplicity. The RX realizes the down-conversion of the same two uppermost D-band sub-channels but provides them at separate IF outputs. Both circuits are mounted on a four-layer PCB module integrating the antennas. Each of the two D-band ports of the ICs (outputs for the TX and inputs for the RX) is connected to a separate sub-array of a four-patch square antenna array implemented in the back-side of the PCB. These in-package antennas are intended to be combined with planar lenses to realize a high gain in the order of 30 dBi. More details about the antenna system can be found in [11,13] and the circuits are described in detail in [14].

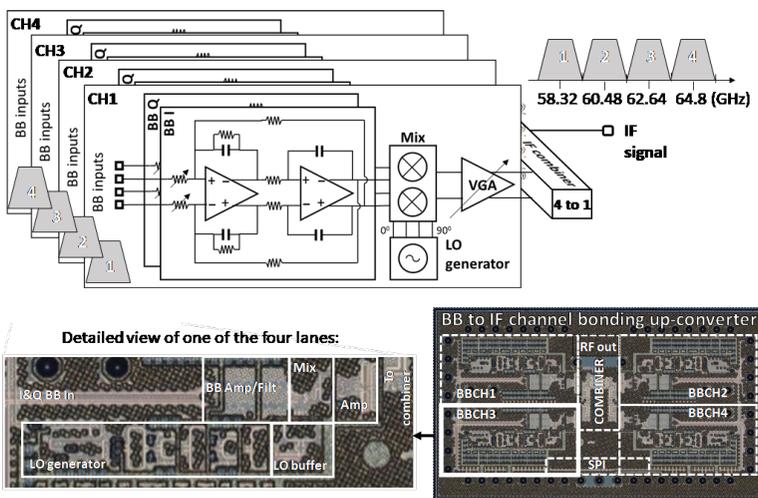


Fig. 3. BB to IF band up-converter and channel bonding circuit implementation.

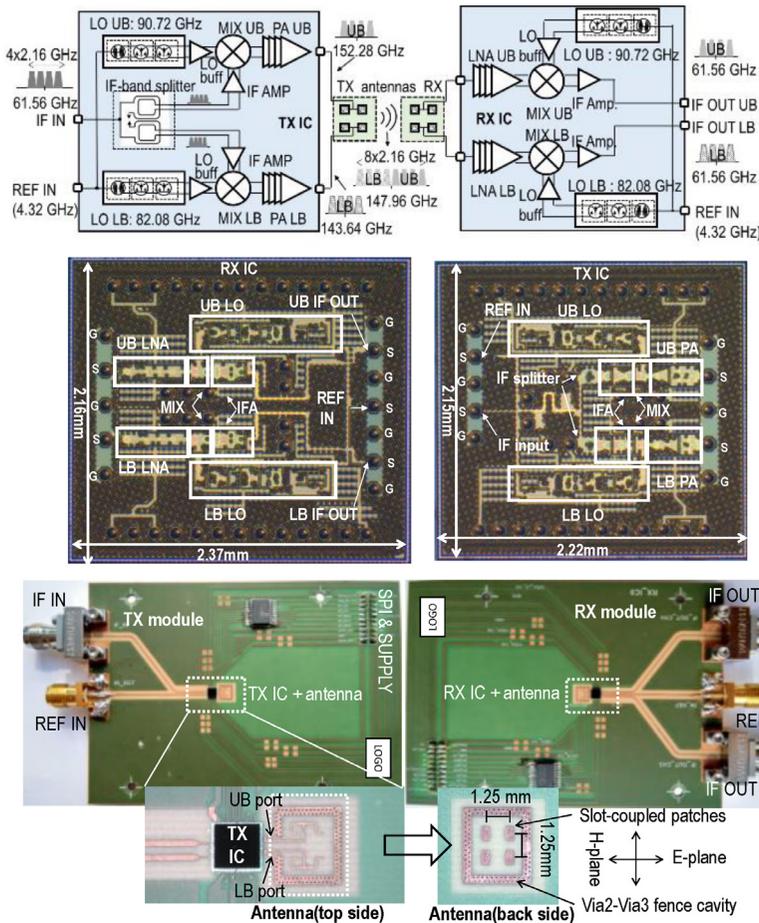


Fig. 4. D-band TX and RX modules and circuits.

The summary of TX and RX single tone measurements are shown in Figure 5 (note that the gains from IF to RF in the figure do not include the flat lens antenna gain). The effective isotropic radiated power (EIRP) at the 1 dB compression point achieved by the TX module (including the transmit array lens) is 26.4 dBm. For a multi-channel signal using high-order modulation the back-off should be larger than for single-channel signals due to a higher peak-to-average power ratio. A back-off of 9 dB has been found to be required for 16-QAM multi-channel

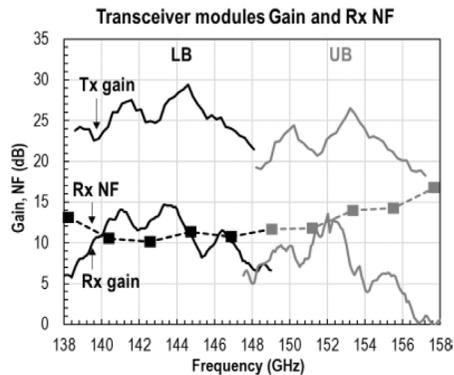


Fig. 5. D-band channel bonding TX and RX module frequency domain characteristics.

modulations in our system, resulting in an effective TX EIRP for modulated signals of 7.4 dB. The receiver module has a noise factor (NF) that varies from 11 to 15 dB across the band. The power consumption of the TX and RX circuits are 600 mW and 400 mW, respectively.

LO generation

The multiple LO signals required in the circuits presented in Sections 3.1 and 3.2 are all generated using the same technique based on integer-N frequen-

cy multiplication described in [5]. The four LO signals required for the first up-conversion operation are shown in Figure 6. The PN at 1 MHz offset is better than -100 dBc/Hz and the PN noise floor is better than -120 dBc/Hz. The LO signals for the second up-conversion step (the two highest frequency LO frequencies) are shown in Figure 7. The PN at 1 MHz offset is also smaller than -100 dBc/Hz and the PN noise floor is better than -125 dBc/Hz. Additionally, LO spurs in the adjacent channel frequencies are smaller than -30 dBc in the worst case. All these

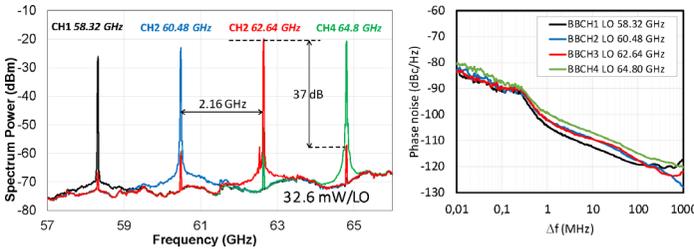


Fig. 6. LO signals spectrum and PN for the BB-IF up-converter.

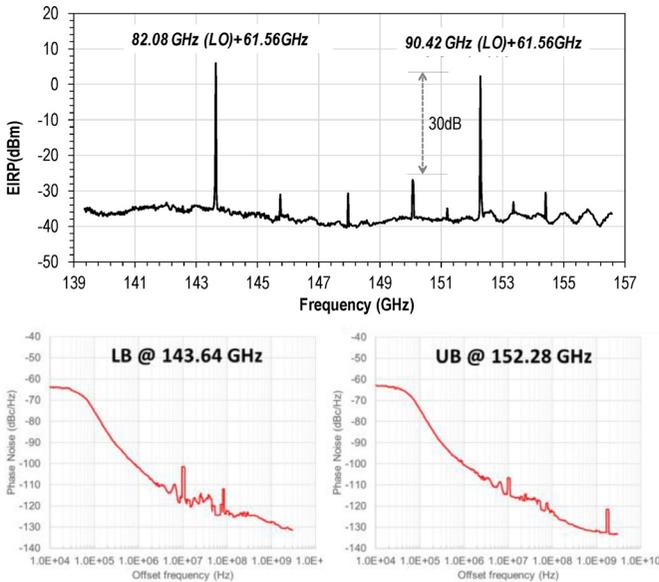


Fig. 7. LO signals spectrum and phase noise for the D-band TX and RX circuits.

features enable multi-channel operation with modulations schemes up to 64-QAM over individual channel BW of 2.16 GHz.

IV. POINT-TO-POINT LINKS EXPERIMENTS

Two point-to-point links experiments are presented in this section, the first involving the IF to D-band modules presented in Section 3.2 and the second one involving a full BB to D-band TX combining the circuits from sections 3.1 and 3.2.

Link demonstration based on D-band TX and RX modules

The TX and RX modules are inserted into a full link demonstration platform combining a MATLAB signal-processing environment that implements the digital BB (DBB) TX and RX functions and

controls an arbitrary waveform generator (AWG) and a digital sampling scope (DSO) to interface with the analog components. In this first experiment, the IF signals at the input of the D-band TX module are generated by the AWG over the whole IF BW and up-converted to V-band using a commercial mixer and LO generator, as shown in Figure 8. The IF output signals of the D-band RX module are directly sampled by the DSO. The full TX-RX point-to-point link setup is shown in Figure 8. The TX module is equipped with a transmit array planar lens but not the RX module. The link distance is set to 42 cm. Figure 9 shows the signal spectrum and received constellations. The maximum data-rate is 56.32 Gb/s for 16-QAM modulation with error vector magnitude (EVM) better than 13% in all channels.

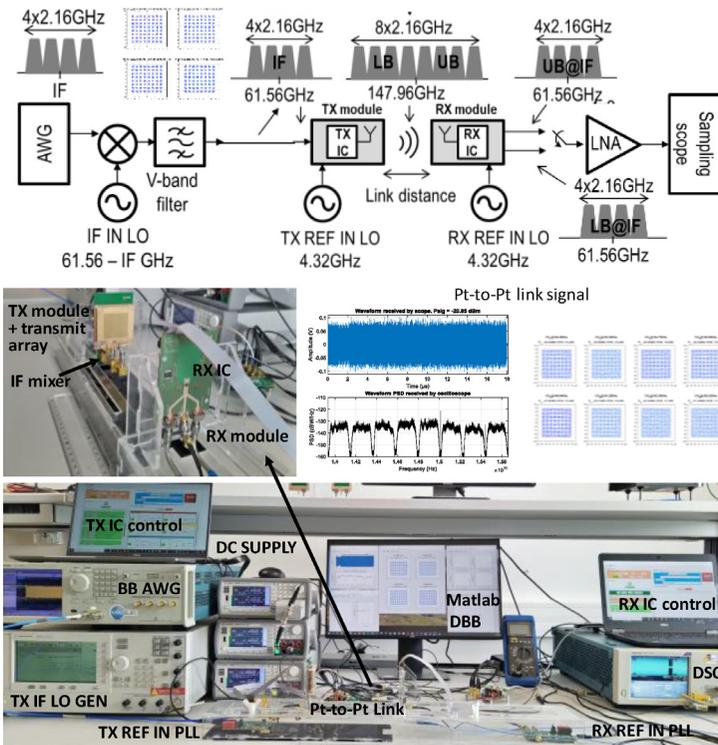


Fig. 8. Point-to-point links implemented using the D-band TX and RX modules described in Section 3.2.

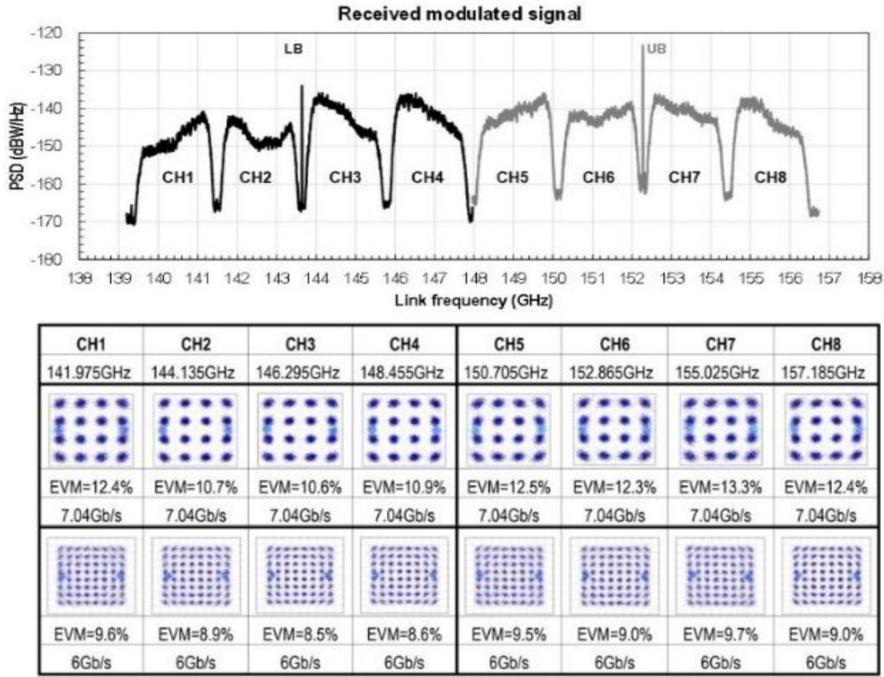


Fig. 9. D-band point-to-point link results.

Link demonstration based on BB to D-band TX

For the second experiment, the TX circuits from Sections 3.1 and 3.2 are combined in order to realize a full transmitter from multiple BB channel up to the D-band. The block diagram of the BB to

D-band TX is shown in Figure 10. The RX is implemented using a commercial D-band receiver with standard 20 dBi horn antenna. The complete link set-up is shown in Figure 11. The BB signals are generated using a multi-channel AWG and a DSO is used to sample the IF signal

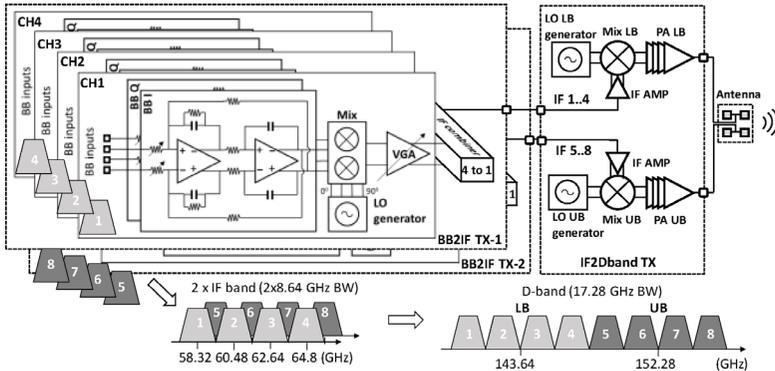


Fig. 10. BB to D-band TX block diagram.

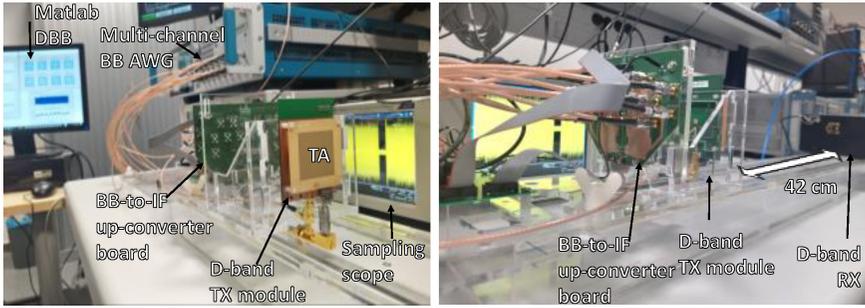


Fig. 11. BB to D-band point-to-point link set-up.

at the output of the D-band commercial receiver. This circuit has a worst case NF of 18 dB across the signal band. Table 1 shows a link budget analysis. The SNR should be 14 dB for 16-QAM modulations in order to attain a raw bit error rate (BER) of 10^{-2} that results in an acceptable packet error rate (PER) of 10^{-4} with reasonable LDPC forward-error correction codes [15]. This is achieved at a 70 cm

link distance considering the available EIRP and the RX NF numbers, with a small implementation margin.

The link shown in Figure 11 is measured for various distances. The DBB RX provides performance metrics such as signal power per channel, BER, EVM and the received constellations. The results of Figure 12 show the evolution of EVM per channel as the distance is increased from

TABLE 1
LINK BUDGET ANALYSIS

Parameter	Per channel	Full band
BW (GHz)	2.16	IF: $2 \times 4 \times 2.16$ RF 8×2.16
BB I or Q diff. peak amp. (mV @ 100 Ω)	750	
BB I or Q rms amp. (mV @ 100 Ω)	270	
BB to IF up-converter gain (dB)	-29	
IF signal power (dBm)	-30.4	-24.4 ($\times 2$)
D-band TX gain (dB)	37	
EIRP@ 1dBCP (dBm)	17.4	26.4
Back-off (dB)	10	
EIRP for IF power (dBm)	7.4	16.4
Path Loss @ 70 cm (dB)	72.7	
Rx antenna gain (dBi)	20	
Rx NF (dB)	18	
RX signal @ antenna aperture (dBm)	-45.3	-36.3
RX noise @ antenna aperture (dBm)	-62	-53
SNR	16.7	
Margin for BER 10^{-2} on 16-QAM (dB)	2.7	

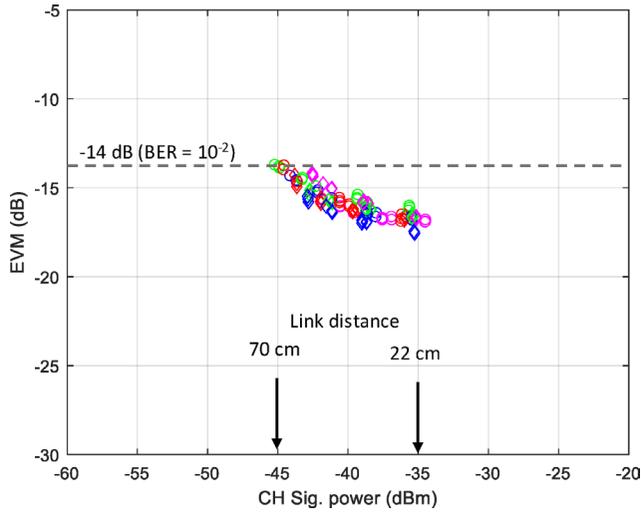


Fig. 12. EVM versus channel RX signal power for the set-up shown in Figure 11 as the TX-RX link distance is varied.

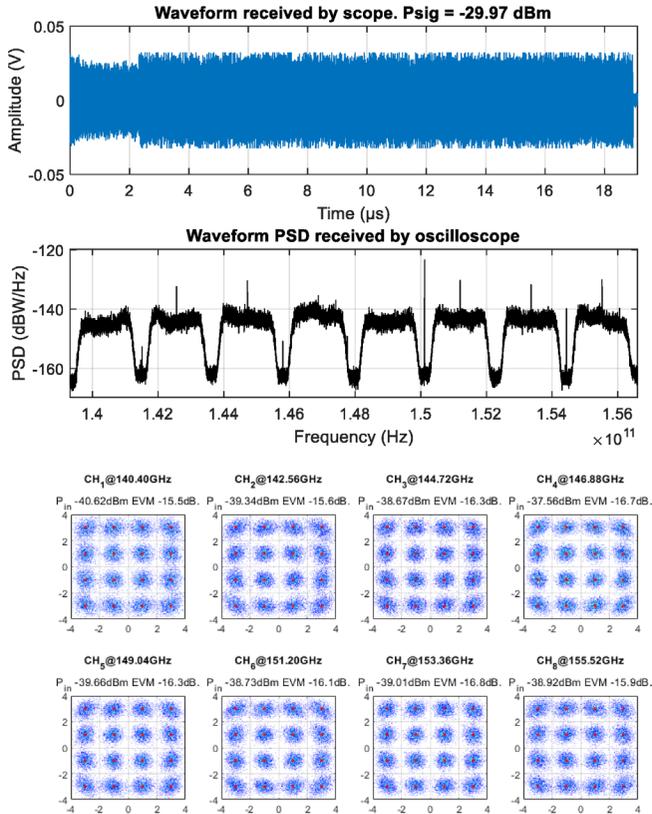


Fig. 13. RX signal waveform, spectrum and constellations for a link distance of 35 cm and 56.32 Gb/s of total data-rate.

16 to 70 cm. Note that the target EVM of -14 dB, or 20%, (for BER = 10^{-2}) is obtained for single channel power of -45 dBm, which corresponds to a link distance of 70 cm. The RX signal waveform and spectrum as well as the constellations for each channel for an intermediate distance of 35 cm are shown in Figure 13. Each channel is modulated with a 7.04 Gb/s 16-QAM signal resulting in a total link data-rate of 56.32 Gb/s and in an energy efficiency of 27.5 pJ/bit.

V. CONCLUSION

In this work, a disruptive implementation of TX and RX for high-data rate wireless communications based on channel bonding architectures is presented. The most challenging issues, including multiple LO signals generation and power combining approaches have been discussed. A full BB to D-band transceiver and two different experiments of point-to-point links have been presented showing the potentialities of these type of architectures for 100 Gb/s wireless links achieving energy efficiencies in the range of a few tens of pJ/bit.

REFERENCES

- [1] M. G. L. Frecassetti, *et al.*, “D-Band Backhaul and Fronthaul Solutions for 5G Radio Access Network,” *2022 52nd European Microwave Conference (EuMC)*, Milan, Italy, 2022, pp. 772–775.
- [2] ETSI GR mWT 012 V1.1.1 (2018-11) “5G Wireless Backhaul/X-Haul,” available on-line at: https://www.etsi.org/deliver/etsi_gr/mWT/001_099/012/01.01.01_60/gr_mWT012v010101p.pdf.
- [3] Q. J. Gu, “Sub-THz/THz Interconnect, Complement to Electrical and Optical Interconnects: Addressing Fundamental Challenges Related to Communication Distances,” in *IEEE Solid-State Circuits Magazine*, vol. 12, no. 4, pp. 20-32.
- [4] K. Okada, “Maximizing Energy Efficiency in Sub-THz Radio Communication and Prospective toward 6G,” *2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, Phoenix, AZ, USA, 2022, pp. 1-4.
- [5] C. Jany, *et al.*, “A Programmable Frequency Multiplier-by-29 Architecture for Millimeter Wave Applications,” in *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1669-1679, July 2015.
- [6] A. Siligaris *et al.*, “A Multichannel Programmable High Order Frequency Multiplier for Channel Bonding and Full Duplex Transceivers at 60 GHz Band,” *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los Angeles, CA, USA, 2020, pp. 259-262.
- [7] A. Hamani *et al.*, “A D-Band Multichannel TX System-in-Package Achieving 84.48 Gb/s With 64-QAM Based on 45-nm CMOS and Low-Cost PCB Technology,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 7, pp. 3385-3395, July 2022.
- [8] J.L. Gonzalez-Jimenez, C. Dehos, N. Cassiau, *et al.* “Channel-bonding CMOS transceiver for 100 Gbps wireless point-to-point links,” in *J Wireless Com Network*, vol. 117, pp. 1-21, June 2020.
- [9] A. Siligaris, P. Courouve, G. Waltener, A. Hamani, C. Dehos and J. L. Gonzalez-Jimenez, “A 42.24 Gb/s Channel Bonding Up-Converter with integrated multi-LO generation in 45nm CMOS,” *2023 IEEE 23rd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Las Vegas, NV, USA, 2023, pp. 4-7.
- [10] A. Hamani *et al.*, “A 84.48-Gb/s 64-QAM CMOS D-Band Channel-Bonding Tx Front-End With Integrated Multi-LO Frequency Generation,” in *IEEE Solid-State Circuits Letters*, vol. 3, pp. 346-349, 2020
- [11] J.L. Gonzalez-Jimenez, *et al.*, “A D-Band High-Gain Antenna Mod-

ule Combining an In-Package Active Feed and a Flat Discrete Lens,” *2022 52nd European Microwave Conference (EuMC)*, Milan, Italy, 2022, pp. 784-787.

- [12] J.L. Gonzalez-Jimenez, *et al.*, “A 57.6Gb/s Wireless Link Based on 26.4dBm EIRP D-Band Transmitter Module and a Channel Bonding Chipset on CMOS 45nm,” *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Diego, CA, USA, 2023, pp. 1-4.
- [13] F. Foglia Manzillo, *et al.*, “A 28dBm-EIRP Low-Profile D-Band Transmitting Module with a Folded Transmitarray Antenna,” *2023 IEEE/MTT-S International Microwave Symposium (IMS)*, San Diego, CA, USA, 2023, pp. 1-4.
- [14] A. Hamani *et al.*, “A 56.32 Gb/s 16-QAM D-band Wireless Link using RX-TX Systems- in-Package with Integrated Multi-LO Generators in 45nm RFSOI,” *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, USA, 2022, pp. 75-78.
- [15] J. Rosseel, V. Mannoni, V. Savin and I. Fijalkow, “Error Structure Aware Parallel BP-RNN Decoders for Short LDPC Codes,” *2021 11th International Symposium on Topics in Coding (ISTC)*, Montreal, QC, Canada, 2021, pp. 1-5.



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Alexandre Siligaris was born in Greece, in 1977. He received his M.Sc. and Ph.D. degrees from the Science and Technology University of Lille, Villeneuve-d’Ascq, France, in 2001 and 2004, respectively. During his Ph.D. studies, he was involved in transistor characterization and modeling for high-frequency applications. From 2004 to 2005, he was an associate professor with the Science and Technology University of Lille. In 2006, he joined CEA-Leti, Grenoble, France. His work focuses on high-frequency modeling and high-frequency circuit design in CMOS and BiCMOS advanced technologies.



Abdelaziz Hamani (Member, IEEE) received his B.Sc. degree in electronics engineering, M.Sc. degree in telecommunication systems, and Ph.D. degree in telecommunications and signal processing from the Science and Technology University of Algiers, Alger

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Cédric Dehos joined CEA Leti, Grenoble, France, in 2003 after graduation from ESIEE Paris (Dipl.-Ing. and M.Sc.) in Telecommunication and Signal Processing. Since then he has been involved in system level design of complex RF and digital base band circuits including RF behavioral modeling, architecture design and specification, system simulation and base band signal processing. His main topics of interest included ultra-wide band systems, digital compensation of RF imperfections, and antenna beamforming. Since 2006, he has been involved in various mm-w developments in CMOS or BICMOS technologies, including 24/79GHz Short Range Radar, 60GHz Wireless HD and WiGig. In 2011, he led Leti mm-w designs and began moving the developments towards 5G small cells, promoting the use of mm-w bands for 5G, and towards short-range chip-to-chip communications and contactless connectors. More recently, he proposed an architecture for channel aggregation in the D-band, targeting >100 Gbps wireless communication. He has been involved in many collaborative projects funded by the European Commission, as well as in many industrial bilateral projects with transfer of technology. He is also active in the promotion of mm-w wireless technologies for particle physics with CERN.



Fabrice Chaix was born in France in 1974. He received his M.Sc. degree in microelectronics from the Science University of Grenoble, Grenoble, France, in 2000. In 2001, he joined CIRIEL, Grenoble, France, where he worked on various research projects as an Analog Circuit Designer. In 2004, he joined EA-SII-IC, Grenoble, France, where he was involved with high-speed ADC circuits in designing CMOS advanced technologies. In 2008, he joined CEA-LETH, Grenoble, France, where he is involved with analog and millimeter-wave circuit design in CMOS advanced technologies.



Pierre Courouve received his M.Sc. degree from the Ecole Supérieure d'Ingénieurs de Nice Sophia-Antipolis, Nice France in 2005. He was consultant with ST Microelectronics for 7 years as Analog IC

Design engineer, working on high-speed op-amp for standard purposes or rad-hard applications on SOI bipolar technology (1 or 0.25 μm). He joined Maxim Integrated, Gières, France, for 2 years as MTS Analog Engineer involved in many IPs in Power Management IC sub-systems for major international suppliers. Since 2014, he has been with CEA-LETH, Grenoble, France, and works in RF Architecture and IC Design Lab on RF-ID solutions and technology transfer for industrial partners thanks to his power management expertise. He is the author of 2 patents on new architecture improving data rate up to 27.12 Mb/s on HF passive tags. He skills-up in RF field through low power wide area transceiver projects and on IoT topics designing ASICs in either bulk or advanced FD-SOI technology stack. He focuses his research on narrow band filters based on N-path architectures suitable on such integrated solutions. Recently, he has followed up on industrial transfer for a narrow band transceiver for satellite LPWAN communications and UWB SoC for localization.



Guillaume Robe received his M.Sc. degree from Institut Polytechnique de Grenoble, Grenoble France in 2020. He worked for 2 years as a consultant for the CEA-LETH as an Analog IC designer, working on the power management of an UWB SoC. In 2022 he joined the CEA-LETH and works in the RF Architecture and Design Lab. His works focus on power management and analog circuit design.



Jean Baptiste David was born in 1973 and received his M.Sc. in 1997. After various experiences in industrial companies and startups, he joined CEA-Leti in 2002. He worked on passive components modeling and passive filters design on BAW and SAW technologies. He is also involved in RF-mmW passive component modeling and electromagnetic simulation. His research interest includes mm-w circuit design for frequency synthesis, including VCOs, ILOs among others.



Francesco Foglia Manzillo (Member, IEEE) received his M.Sc. degree (cum) in electronics engineering from the University of Naples Federico II, Naples, Italy, in 2012, and his Ph.D. degree in signal processing and telecommunications from the University of Rennes 1, Rennes, France, in

2017. He spent two research stays at Delft University of Technology, The Netherlands, in 2012, at the University of Michigan, USA in 2016. Since July 2017, he has been with CEA-Leti, Grenoble, France. His research interests include the analysis, synthesis, and design of antenna arrays, quasi-periodic structures, beamforming systems, and the integration of millimeter-wave radio systems. Dr. Foglia Manzillo was a co-recipient of the Best Innovation Award at the 39th ESA Antenna Workshop in 2018 and co-authored a paper awarded with the EuMC Young Engineer Prize at EuMW 2022.



Antonio Clemente (Senior Member, IEEE) received his B.Sc. and M.Sc. degrees in telecommunication engineering and remote sensing systems from the University of Siena, Siena, Italy, in 2006 and 2009, respectively, and his Ph.D. degree in signal processing

and telecommunications and the “Habilitation à Diriger des Recherches” degree from the University of Rennes 1, Rennes, France, in 2012 and 2021, respectively. His Ph.D. project was realized at the CEA-Leti, Grenoble, France. From October 2008 to May 2009, he realized his master thesis project at the Technical University of Denmark (DTU), Lyngby, Denmark, where he was involved in spherical near-field antenna measurements. In 2012, he joined the Research and Development Laboratory, Satimo Industries, Villebon-sur-Yvette, France. From 2016 to 2018, he was the Technical Coordinator of the H2020 joint Europe and South Korea 5G-CHAMPION Project. Since 2013, he has been a Research Scientist with CEA-Leti. He has authored or coauthored more than 137 articles in international

journals and conferences and received 20 patents. He has been involved in more than 28 research projects at the national and European levels. His current research interests include fixed-beam and electronically reconfigurable transmit array antennas, millimeter-wave, and sub-terahertz antenna-in-package (AiP), antenna arrays, periodic or quasiperiodic structures, near-field focused systems, antenna theory and fundamental limitations, synthesis and modeling, and near- and far-field antenna measurements. Dr. Clemente received the Young Scientist Award (First Prize) during the 15th International Symposium of Antenna Technology and Applied Electromagnetics (ANTEM 2012) and the Best Antenna Design and Applications Paper Award during the 13th European Conference on Antennas and Propagation (EuCAP 2019). He was a co-recipient of the EuMC Young Engineer Prize at EuMC 2021, the Best Paper Award at JNM 2015 (19emes Journées Nationales Microondes), and the 2019 ETRI Journal Best Paper Award. In 2019, he was a Finalist for the “Microwave Prize” at the European Microwave Conference (EuMC 2019). He is currently an Associate Editor of the journal *Frontiers in Communications and Networks*, and serves as a reviewer for the numerous IEEE and IET journals in the field of microwave, antennas, and propagation.



Nicolas Cassiau received his M.Sc. degree in Signal Processing in 2001 from Polytech’Nantes, France. Since then he has been a research engineer and project manager at CEA-Leti in Grenoble, France. His fields of interest are digital wireless communications and algorithms design. He is, or has been,

working in particular on physical layer design and assessment for 4G and 5G, RF impairments modeling and sub-terahertz communications. He has been involved in several European projects, including mmMAGIC (millimeter wave communications), 5GNOW (waveform design) and more recently 5G-ALLSTAR. He has authored or co-authored over 35 papers and holds several patents in the above-mentioned fields.