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CMOS FD-SOI Technologies Ruggedness for Millimeter Wave Power Amplifier Design

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Abstract— This paper studies the reliability that CMOS FD-SOI can achieved for mmWave Power Amplifier (PA) applications. The technology opportunities and constraints are also shown. To demonstrate the capability of such technology, a highly rugged power-amplifier for the Ka band radio (26.5-40GHz) applications implemented in a CMOS 22FDX process is presented. By using design techniques together with an optimized supply voltage reduction, the power amplifier achieves an excellent reliability even under the worst mismatch condition (VSWR) of 7:1. These results validate the capability of the technology for highly reliable power amplifier for mmWave 5G applications.

Keywords—FD-SOI, reliability, 22nm, mmWave power amplifier, Ka band, SOI, FDX, ruggedness, HCI, TDDB

I. INTRODUCTION

Integrated RF CMOS Power Amplifier is somewhat recent. The main challenge was to achieve good performances with devices dedicated to digital. This has been possible thanks to the increase of f_T/f_{MAX} together with the gate length reduction. The evolution towards deep nanometer CMOS technologies has facilitated the design of highly integrated systems. Today, CMOS PA design has been demonstrated up to mmWave frequencies and most connectivity products integrate the PA in the transceiver. Nevertheless, the counter part is the coming up of reliably issues [2]. To ensure this reliability, specific design approach must be considered. This paper proposes a study of CMOS FD-SOI technologies ruggedness for mmWave Power Amplifier Design. The purpose is to validate how reliability can be improved with specific design techniques. The first part describes the CMOS FD-SOI technology in the reliability context. The second part proposes a Ka band PA design as a test vehicle for ruggedness studies. The last part presents the measurement results and the conclusion.

II. DEVICE TECHNOLOGY

A. CMOS FD-SOI Device Technology

Device reliability must be considered in an RF/mmW circuit that performs in large signal such as VCO, Mixer and of course Power Amplifier. Most of them use n-FET because of their superior f_T/f_{MAX} performances. For such device, the main reliability challenges to consider are the breakdown voltages (BV), hot carrier injection (HCI), time dependent dielectric breakdown (TDDB) and circuit ruggedness to voltage standing wave ratio (VSWR). The BVDS of a transistor represents the V_{ds} limit where device reach hard breakdown (current drops abruptly) because of the PN junction conduction. After breakdown, the device is no longer useful or burnt. The BVON (soft breakdown) is defined as V_{ds} level which results in I_{ds} current density of 1uA/um at $V_{gs}=0V$. If BVON is reached, the device performances are not guaranteed and can be out of

specifications [1]. The following table shows simulated breakdown voltages for 22FDX technology SG and EG transistors.

| FET (nominal Vdd) | L (nm) | BVON NMOS ($V_{G=0}$) $\Leftrightarrow V_{dg_MAX}$ | BVDS NMOS ($V_{G=0}$) $\Leftrightarrow V_{dg_MAX}$ | BVDS NMOS ($V_{G=VDD}$) $\Leftrightarrow V_{gs_MAX}$ |
|-------------------|--------|---|---|---|
| SLVT (0.8) | 20 | 2,5 | 3.25 | 3 |
| EGSLVT (1.8) | 150 | 4,2 | 4.6 | 4.15 |

Table 1: Simulated maximum voltage rating for 22FDX technology RF n-FETs at 25°C

HCI degradation in FET device characteristics occurs when the drain to source bias exposure is high over time. As the transistor channel is starting at low V_{ds} the electric field is equally divided over the length of the channel by the existence of an inverted channel. When the drain-source voltage is increased the channel begins to pinch off, restraining the electric field to the region between the channel edge and the drain diffusion. This causes an increasing of the magnitude of the electric field and channel carriers to accelerate through the pinched off region reaching a velocity that is greater than the thermally limited diffusion drift velocity. If a channel “hot carrier” strikes a crystal atom near the drain region, it may produce an electron-hole pair. In that case the transistor transconductance slowly degrades. This mechanism is usually monitored by the degradation of the I_{dsat} over the time. In this work, a degradation of a maximum of 10% has been chosen as a reference point. Therefore, to cover a given lifetime for a specific power amplifier, the DC and RF voltage must be studied. RF lifetime must be evaluated considering the application, the mission profile and the modulation scheme used. HCI effects limit the voltages that may be used with CMOS devices, and are most severe at shorter channel lengths. The HCI device degradations are correlated to the substrate current for n-FETs. The correlation exists since hot carriers are driven by the maximum channel electric field, which occurs at the drain end of the channel. In CMOS PD-SOI the body thickness (~60nm) is too high to have a full control of the depletion layer. For an FD-SOI technology, because the SOI thickness is <10nm, the channel is fully depleted allowing a full control of the I_{off} current of the transistor. It means that the HCI degradation is reduced in FD-SOI in comparison to bulk or PD-SOI [3]. Hot carrier degradation can be simulated with the appropriate software such as Cadence Spectre or RelXpert.

For TDDB, caution must be taken on the maximum gate voltage which is equivalent to electric field strength across the gate oxide. Each electric stress consumes oxide life time. It means that this degradation is cumulative. Advanced CMOS node (<65nm) have a gate oxide thinner and a lower operating voltage. Hence, for soft TDDB, the initial rupture in the oxide does not disrupt significantly the functionality of

the transistor. Therefore, in order to determine process fabricating the device parameters are monitored after the oxide breakdown, and the failure time is determined by the time it takes for the transistor performance to degrade to a certain level. For hard TDDB, there is a direct percolation path in the oxide leading to catastrophic failure of the device. For both TDDB mechanisms, the time to failure is highly accelerated by voltage and temperature. When an RF swing is applied to the transistor, the TDDB reliability check can be predicted by performing a time domain voltage simulation on transistor nodes (V_{dg} , V_{gs} and V_{gb}) at the most extreme dynamic operating point (i.e. saturated output power in a power amplifier). This should confirm that the voltage waveform exposure of the gate do not exceed the maximum allowed voltage [1]. This type of simulations have been done on this work and are presented in part III.

B. Mission Profile

The mission profile analysis must be the first step in the reliability analysis as it gives the power amplifier lifetime requirement. In consumer cellular/connectivity, a typical lifetime is 10 years. Another aspect of the mission profile is the modulation scheme used. High data rate communication requires complex modulation such as OFDM (orthogonal frequency division multiplexing). For instance, the signal waveforms used in 5G PPP mmW standard has a very large (~9.6 dB) peak-to-average spikes. An OFDM 64QAM modulation signal is shown in Figure 1. In a practical use, the PA typically operates at a 6 to 8 dB back-off from the max output power.

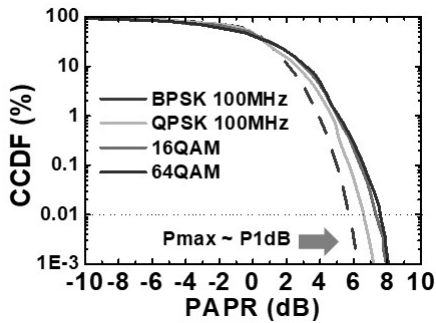


Fig 1 : CCDF of a power amplifier for various modulation profiles

Most of the PA operating time is spent at ~8-9dB back-off or even less while power peaks up to P1dB (or even beyond) represent only a very short cumulated time. For instance, considering a 10 years lifetime (always ON for simplicity purposes), the amplifier will spend approximately 4.7 years at back-off (Peak to Average power ratio or PAPR = 0dB), 100 hours at P1dB/max-1dB and 13 hours at P_{max} (or P1dB for linearity purposes). As an example, the following table shows simulated worst-case peak voltages (V_{ds} or V_{dg}) considering 10 years and 0.05 years breakdown voltages for 22FDX technology SG and EG transistors.

| FET (nominal Vdd) | L (nm) | Vp for HCI 10y | Vp for HCI 0,05y | Vp for TDDB 10y | Vp for TDDB 0,05y |
|-------------------|--------|----------------|------------------|-----------------|-------------------|
| SLVT (0.8) | 20 | 1,25 | 1,3 | 1,41 | 1,76 |
| EGSLVT (1.8) | 150 | 2,81 | 2,92 | 2,90 | 4.13 |

Table 2: Simulated maximum reliability figures-of-merit for 22FDX technology RF n-FETs at 25°C

III. KA BAND POWER AMPLIFIER DESIGN FOR RELIABILITY

A Ka-band power amplifier has been chosen as test vehicle for reliability evaluation. The circuit has been designed in CMOS 22FDX from GlobalFoundries. One of the main weaknesses of standard CMOS for power amplifier design purpose is the limited voltage levels capability [3]. One approach to overcome such a limitation is based on stacked FETs (also known as balanced cascode configuration). With proper biasing and loading, uniform voltage distributions can be obtained across the transistors. Therefore, with n-transistors, it becomes possible to sustain n-time V_{max} , where V_{max} is the maximum voltage of a single device. In addition, multiple device gate thickness (thin or thick) can be mixed in the stack configuration so that ideally balanced between performances and reliability [2]. In FD-SOI technology, since the diode between well and substrate no longer exists, the topology is only limited by the loss introduced by each successive stage and the phase delay in each transistor [3]. Therefore, the topmost device of the stack sees a drain-sub swing that is equal to the n-times increased output swing of the stacked FETs. In that case, the number of devices that can be stacked is first limited by the breakdown of the buried oxide (BOX) below each device. This voltage is >6V in FD-SOI (28, 22nm). Based on this latest property, in this work we present a two stages, PA based on the stack topology to improved hot carrier injection (HCI) performances and circuit ruggedness to VSWR. In addition, the last stage used two parallel power cells that are power combined in order to divide the maximum power seen by each of them and thus improve the robustness. The following figure presents the synoptic of the PA and the detail schematic of each power cell.

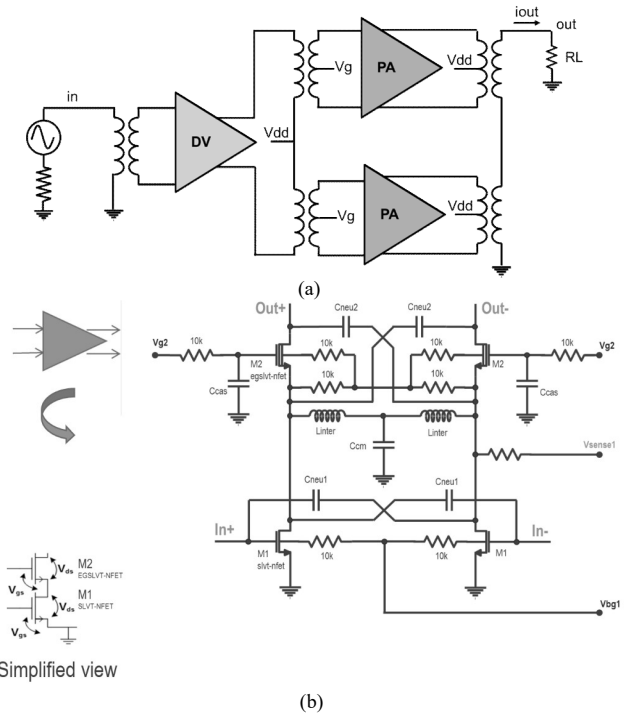


Fig 2 : Power amplifier synoptic (a) ; schematic of cells DV & PA (b)

In any power amplifier in linear class (A, AB or B), the drain to source RF voltage swing of the output stage is $2xV_{supply}$. Therefore, any devices biased at nominal technology voltage is exposed to reliability issues in large signal operation, making them sensitive to HCI and TDDB.

To design a PA conform for manufacturing, this aspect must be taken into account when RF performances are benchmarked. To solve that issue, after simulations, a power supply derated by 20 % has been chosen to secure ageing and reliability. Therefore, for the stack topology shown in Fig 2, the supply voltage is set at $0.8 \times (1.8+0.8) = 2.08V$. Common source and common gate transistors are stabilized thanks to the neutralization capacitance C_{neu1} and C_{neu2} respectively.

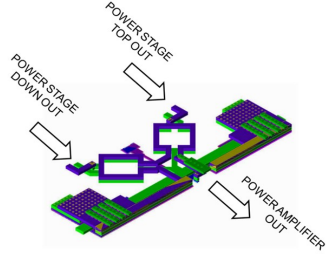


Fig 3 : 3D view of the output combiner-transformers of the PA

The first matching network (the one at input) uses balun from the design kit. The others networks require specific custom networks. The interstage and output matching networks are made with two 1:1 transformers connected in serial. This configuration allows the power matching between stages and the power combining transformation. The Fig 3 shows the designed output combiner.

The ageing has been evaluated by monitoring two phenomena: TDDB and HCI. As stated previously, the chosen failure criteria is a drop of 10% of the nominal drain current of the transistor (I_{dsat}). TDDB and HCI maximum values have been first determinate with Cadence Spectre ageing simulation considering the topology of the circuit (common-source, common-gate...) and the geometry/type of each transistor (L gate, number of fingers, thin or thick oxide). Then, an ageing mask has been defined for each transistor that compose the cascode cell. In the following figure, M1 is the thin oxide transistor (common source, slvtlp, $V_{ddnom}=0.8V$) and M2 is the thick oxide transistor (common-gate, egslvtlp, $V_{ddnom}=1.8V$). Both the driver cell and the power have been analyzed. As expected, the power cell shows the most extreme antiparallel shapes plotted in following figure (the smallest antiparallel represent the driver). Finally, two use cases have been chosen, one considering 10 years lifetime at mean output power (see Fig 1) and one at maximum output power (OCP1) during 0.05 years (Fig 4). We can see that based on simulation, the circuit should be able to work with less than 10% degradation I_{dsat} over 10 years. The second criteria followed for this design is the robustness over VSWR degradation.

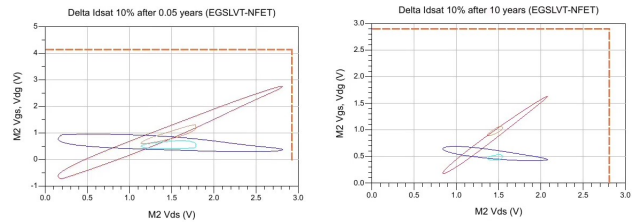
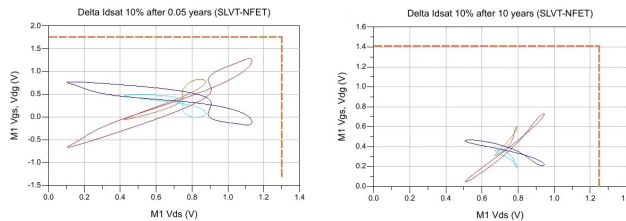


Fig 4 : 35-GHz anti-parallel waveforms of V_{gs} , V_{gd} and V_{ds} of the cascode pair transistors (M1 & M2) at P_{rms} (10 years) and P_{max} (0.05 years)

The Fig 5 shows anti-parallel waveforms of V_{gs} , V_{gd} and V_{ds} of the cascode pair transistors for a VSWR of 4:1 over 360° at maximum output power. In that case, the maximum absolute voltage value is checked (see Table 1 & Table 2 for chosen values). It can be seen that in any case the circuit voltages do not exceed the maximum voltage rating.

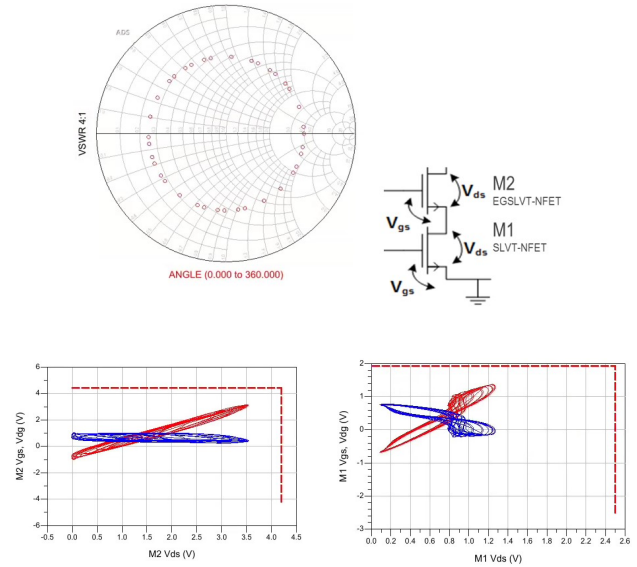


Fig 5 : 35-GHz anti-parallel waveforms of V_{gs} , V_{gd} and V_{ds} of the cascode pair transistors for a VSWR of 4:1 over 360° at maximum output power

IV. MEASUREMENT RESULTS

The PA is fabricated in 45RFSOI process and occupies a $0.7 \times 0.25 \text{ mm}^2$ core area.

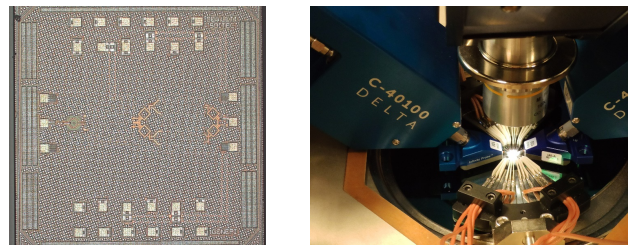


Fig 6 : Die micrograph of the fabricated PA chip in CMOS 22FDX process and on wafer probing setup

Small signal measurement are performed with a vector network analyzer (R&S ZVA67). Dedicated coplanar probes are used for 20-50 GHz measurement. The DC measured current of the driver and power stage are 35 mA and 40 mA respectively. The simulated and measured S-parameters are presented Fig 4.

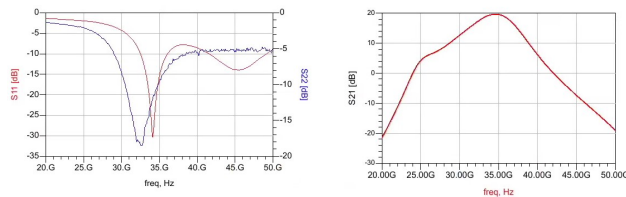


Fig 7 : S parameters vs. frequency

The power amplifier achieved 20dB gain with 5GHz bandwidth-3dB. The maximum output power is 17dBm at 35GHz (Fig 8). The measured amplitude and phase distortion are less than 1dB and 5° up to 16dBm respectively. The maximum PAE is 10%.

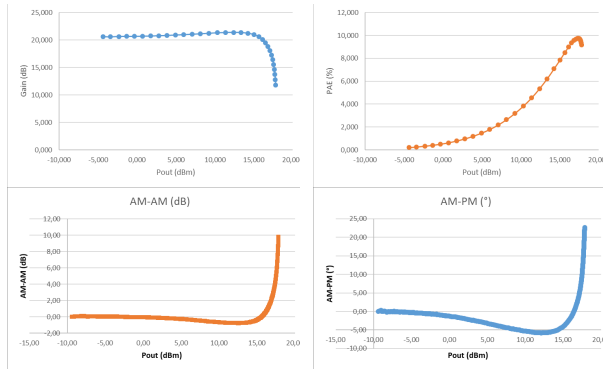


Fig 8 : One tone, large signal measurement at 35GHz

RF power amplifiers have a nominal output impedance of 50Ω and in an ideal world would be used with 50Ω load impedance. This ideal use case results in maximum power transfer from the PA to the load (i.e. all the power is absorbed in the load and none is reflected back). Unfortunately, in the real world, PA are used with load impedances that are around 50Ω. Not only is load mismatch common in most applications, but this load varying with frequency. A reliable PA must be capable to sustain extreme mismatches without compromising performance or lifetime. VSWR is the voltage ratio between the source (PA) output impedance and the load impedance at a given frequency. If the PA is driving an ideal 50Ω load impedance then the VSWR is 1:1 and there is no mismatch.

The robustness over VSWR degradation has been evaluated thanks to the use of a specific load pull probe station. Two tests have been performed. A soft stress of <30min loading presented in Fig 9, and a hard test corresponding to a longer 60min stress in Fig 10. The targeted robustness level was defined for a VSWR from 2:1 to 4:1 over 360° at maximum output power. No breakdown is observed even after 1h of 7:1 VSWR, which shows a very good robustness against load impedance variation. At maximum output power, after 1h of stress, a degradation of 0.35dB for the gain and 0.5% for the PAE is measured and almost no degradation at P_{rms} . At the same time, the I_{dsat} drift is measured at 8% and can be explained by HCI degradation,

which occurs when the drain to source bias exposure is high over time. Almost no current degradation is observed on the driver current, as this stage is well isolated from output load variation because of the power cell stage between.

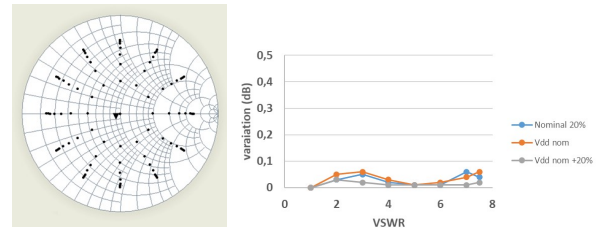


Fig 9 : 35GHz VSWR robustness measurement from 2:1 to 7.5:1 over 360° at maximum output power and Vdd +/-20%

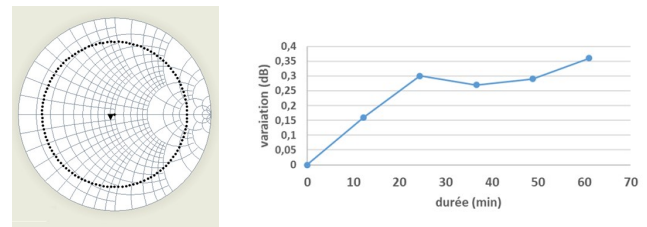


Fig 10 : 35GHz ageing degradation (HCI) measurement at 7:1 VSWR over 360° at maximum output power during 60 min

CONCLUSION

With very good RF capabilities, recent FD-SOI nodes show a great potential for a complete integration from digital to mmWave. Nevertheless, ageing and reliability must be considering. In this paper, a highly rugged Ka band power amplifier with an output power of 17dBm is presented. A very good reliability results were achieved thanks to stacking device technique together with power combining and supply voltage derating, offering high output power while securing n-FETs from breakdown. These results validate the capability of the technology for highly reliable power amplifier for mmWave 5G applications.

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