CMOS-compatible manufacturability of sub-15 nm Si/SiO_2/Si nanopillars containing single Si nanodots for single electron transistor applications

Johannes von Borany, Hans-Juergen Engelmann, Karl-Heinz Heinig, E. Amat, Gregor Hlawacek, Fabian Klüpfel, René Hübner, Wolfhard Möller, Marie-Line Pourteau, Guido Rademaker, et al.

Semiconductor Science and Technology

CMOS-compatible manufacturability of sub-15 nm Si/SiO_2/Si nanopillars containing single Si nanodots for single electron transistor applications

To cite this article before publication: Johannes von Borany *et al* 2023 *Semicond. Sci. Technol.* in press https://doi.org/10.1088/1361-6641/acbe5d

IOP Publishing Journal Title
Semicond. Sci. Technol. **XX** (XXXX) XXXXXX https://doi.org/XXXX/XXXX

CMOS-compatible manufacturability of sub-15 nm Si/SiO_2/Si nanopillars containing single Si nanodots for single electron transistor applications

J. von Borany[1], H.-J. Engelmann[1], K.-H. Heinig[1], E. Amat[2], G. Hlawacek[1], F. Klüpfel[4], R. Hübner[1], W. Möller[1], M.-L. Pourteau[3], G. Rademaker[3], M. Rommel[4], L. Baier[4], P. Pichler[4], F. Perez-Murano[2], and R. Tiron[3]

[1] Helmholtz-Zentrum Dresden-Rossendorf (HZDR), D-01328 Dresden, Germany
[2] Institute of Microelectronics of Barcelona (IMB-CNM, CSIC), E-08193 Bellaterra, Spain
[3] Université Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France
[4] Fraunhofer Institute for Integrated Systems and Device Technology (IISB), D-91058 Erlangen, Germany

E-mail: j.v.borany@hzdr.de

Received xxxxxx
Accepted for publication xxxxxx
Published xxxxxx

Abstract

This study addresses the complementary metal-oxide-semiconductor (CMOS)-compatible fabrication of vertically stacked Si/SiO_2/Si nanopillars with embedded Si nanodots as key functional elements of a quantum-dot-based, gate-all-around single-electron transistor (SET) operating at room temperature.

The main geometrical parameters of the nanopillars and nanodots were deduced from SET device simulations using the nextnano++ program package. The basic concept for single silicon nanodot formation within a confined oxide volume was deduced from Monte-Carlo simulations of ion-beam mixing and SiO_x phase separation. A process flow was developed and experimentally implemented by combining bottom-up (Si nanodot self-assembly) and top-down (ion-beam mixing, electron-beam lithography, reactive ion etching) technologies, fully satisfying process requirements of future 3D device architectures. The theoretically predicted self-assembly of a single Si nanodot via phase separation within a confined SiO_x disc of < 500 nm^3 volume was experimentally validated.

This work describes in detail the optimization of conditions required for nanopillar/ nanodot formation, such as the oxide thickness, energy and fluence of ion-beam mixing, thermal budget for phase separation and parameters of reactive ion beam etching. Low-temperature plasma oxidation was used to further reduce nanopillar diameter and for gate oxide fabrication whilst preserving the pre-existing nanodots. The influence of critical dimension variability on the SET functionality and options to reduce such deviations are discussed.

We finally demonstrate the reliable formation of Si quantum dots with diameters of less than 3 nm in the oxide layer of a stacked Si/SiO_2/Si nanopillar of 10 nm diameter, with tunnelling distances of about 1 nm between the Si nanodot and the neighboured Si regions forming drain and source of the single-electron transistor.

Keywords: CMOS, single-electron transistor, nanostructure fabrication, nanopillars, Silicon nanodot, self-organization, ion-beam mixing, phase separation

1. Introduction

Driven by the tremendous broadening of mobile and "Internet-of-Things" applications, the development of low-power logic and memory circuits remains a main task for the next generation of energy-efficient electronic devices [1],[2]. Structures based on spintronics [3], two-dimensional (2D) materials [4] and tunnelling field-effect transistors made of compound semiconductors [5],[6] are among the favoured approaches for future low-power circuits. With respect to classical Si-based complementary metal-oxide-semiconductor (CMOS) transistor technology, down-scaling of device dimensions is the key for further power reduction [7],[8]. Presently, lateral fin field-effect-transistors (FinFET) in the sub-8 nm node represent state-of-the-art technology, whereas stacked FinFET, ribbon or vertical nanowire transistor architectures enable real 3D-integration in the foreseeable future [9]. In 2013, Larrieu *et al*. [10] presented a silicon vertical nanowire (NW) transistor with gate-all-around (GAA) configuration fabricated in standard CMOS technology. These transistors with NW diameters of 20 – 80 nm offer excellent parameters with an "on/off" ratio > 10^5 and a drain-source current of 10 – 100 nA [11],[12].

Another device type with extremely low energy dissipation is the dot-based single-electron transistor (SET) [13]. In this device, electrons tunnel from the drain to the source region via a quantum dot (QD). The blocking/non-blocking states of SET are controlled by the potential of the QD which can be tuned by a third electrode (gate) capacitively coupled to this dot [14]. Typically, SETs work only at cryogenic temperatures (< 100 K) [15]-[17]. However, for many SET applications room-temperature (RT) operation is mandatory which requires a QD size of only a few nanometers to fulfill the Coulomb blockade condition [14]. SET structures operating at RT has already been realized, mainly based on lateral Si nanowires [18]-[20] or metallic nanodots [21][21]. Numerous SET applications were proposed making use of its high charge sensitivity and low power consumption, see review papers [22],[23] and references therein. Examples are electrometers, DC current or temperature standards, microwave or IR sensors, non-volatile memories or programmable logic circuits.

SETs are often considered as "beyond-CMOS" devices, particularly when metallic or III-V semiconductor QDs are used. The novel SET device architecture considered in this work promises RT operation, CMOS-compatible fabrication and high-density integration. This concept is based on a Si nanodot (ND) embedded in the oxide of a vertically stacked $Si/SiO_2/Si$ nanopillar (NP). The capability for CMOS-compatible, monolithic integration of FETs and SETs is essential because SETs have intrinsic drawbacks, such as low gain, high output impedance or the disability to drive loads [23],[24]. Fortunately, SET and FET performances are complementary. Whereas SETs exhibit ultra-low power consumption, FETs offer advantages such as high speed, driving force, voltage gain and variable input impedance that compensate exactly for the SET limitations. As an example for an integrated SET/FET logic device, logic functionality can be completely realized by the SET network, and only a limited number of FETs are required to drive the power-demanding components of the integrated circuit [25].

It has been proposed by Mahapatra and Ionescu [26] that hybrid SET/FET circuits with the FET operating at sub-threshold regime provide a way to preserve low power consumption. By on-chip SET/FET integration one can boost the Coulomb Blockade oscillation phenomenon of SET and the high drive current of FET. Thus, high performance and low energy dissipation are expected for such SET/FET-CMOS architectures. They are able to address functionalities such as neuromorphic or multiple valued logic circuits which are very difficult to implement by classical FET-CMOS circuits alone [26]. Another application field is sensing, either as a single charge sensor for semiconductor-based quantum computing or as biosensor systems [27].

In this study, we describe a CMOS-compatible fabrication process to realize stacked sub-15 nm $Si/SiO_2/Si$ NPs with embedded Si nanodots (NDs) as key building blocks for SET fabrication. The envisaged SETs have a vertical transistor topology with gate-all-around (GAA) electrode, similar to vertical nanowire FETs, what entails for high-density and monolithic FET/SET integration capability. The process flow combines top-down technologies, such as NP fabrication by electron-beam lithography and reactive ion etching, with the bottom-up approach of Si ND self-assembly. Single (or a few) ND(s) in an oxide with small tunnelling distances to adjacent source/ drain electrodes form by the phase separation of a strongly confined, metastable Si-rich oxide (SiO_x □ SiO_2 + Si) and Ostwald ripening during subsequent annealing. The SiO_x ($x < 2$) is produced by ion-beam mixing of Si into the oxide from the two Si/SiO_2 interfaces, whereas the spatial confinement required for single Si ND formation is defined by the small oxide volume within the NP.

The paper is organized as follows: at first, physical process and device simulations are presented ion order to derive the required dimensions for the NP/ND as well as the basic parameters for ion-beam mixing. Then, the technology for NP/ND fabrication is described in detail, and the realized structures with nanometer dimensions are characterized using state-of-the-art electron and ion microscopy. It is shown that the applied technology is able to realize stacked $Si/SiO_2/Si$ NPs at diameters close to 10 nm with embedded single Si NDs of ≤ 3 nm size, what it will be suitable for SET operation at RT. For structures of only a few nanometers, variability of critical dimensions represents a relevant device reliability aspect [29]. Thus, the impact of tunnelling distance differences or the variation of ND size and its position in the oxide disc on the performance of SETs is finally discussed in a separate section.

The integration of the NP/ND structures into the complex technology of SET/FET circuit fabrication is published in a separate paper [30]. Overall, the technologies introduced in

both publications offer a unique path for the manufacturability of RT operating SETs and integrated SET/FET circuits.

2. Basic considerations and device simulations

Figure 1 shows the basic scheme of a GAA nanopillar SET. The QD, realized by the silicon ND, is separated by two symmetric tunnel junctions from the adjacent drain/source regions. The tunnelling current I_D is a function of the drain-source voltage V_D and the widths of the tunnelling barriers, while the "on/off" state of the transistor is controlled by the potential V_G of the outer circular gate electrode surrounding the ND region at the NP rim. The silicon ND size and tunnelling distances must be sufficiently small to drive a controllable and stable electron current at low voltages V_D and V_G.

To enable RT operation of the SET, the Coulomb blockade [14] condition must be fulfilled, which means that the silicon ND electrostatic energy E_C considerably exceeds the thermal energy kT to suppress the influence of thermal fluctuations. The electrostatic energy of the dot is calculated as

$$E_C = \frac{e^2}{2C_D} = \frac{e^2}{4\pi\varepsilon_0\varepsilon_{Si}d_{ND}} \qquad (1)$$

where C_D and d_{ND} denote the self-capacitance and diameter of the spherical Si ND, respectively; ε_0 is the permittivity, $\varepsilon_{Si} = 11.8$ (Si dielectric number); e, k are the elementary charge and Boltzmann constant, respectively. According to equation (1), a ND diameter of $d_{ND} \leq 3.5$ nm is required to realize a barrier exceeding the common precondition $E_c > 10{\cdot}kT \approx 0.3\ eV$ for RT operation of a quantum device.

Based on the nextnano++ program package [31], a simulation framework was developed to calculate the current-voltage *(I-V)* characteristics of such a stacked NP SET (as shown in figure 2) and to derive the main geometrical constraints as targeted values for NP/ND fabrication [32].

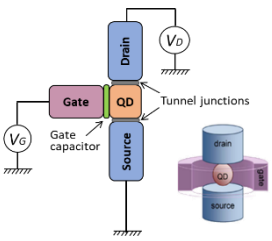

Figure 1. Schema of QD-based SET. The lower right inset illustrates a vertical, GAA SET configuration where the single Si QD is located in the centre of a SiO_2 disc sandwiched between drain/source regions in the pillar. V_G, V_D denotes the gate-source and drain-source voltages, respectively.

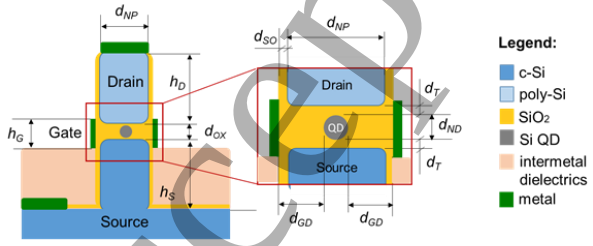

Figure 2. NP/ND as key functional components of the SET with their main geometrical parameters. Legend: $h_{D,S,G}$: height of drain, source or gate; d_{OX}: oxide thickness; d_{NP}: NP diameter; d_{ND}: diameter of the ND, d_T: thickness of tunnelling barrier(s); d_{GD}: gate-dot distance, d_{SO}: thickness of the oxide separating the gate to drain and source, respectively.

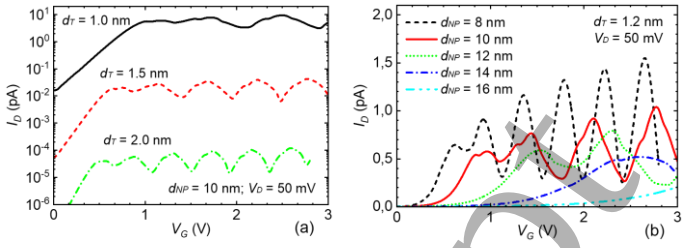

Figure 3. (a) Drain-source current $I_D = f(V_G)$ of the SET operating at RT as a function of the thickness of the tunnelling oxides, and (b) the pillar diameter for a circular Si ND of 3.2 nm size. Other parameters are indexed in the graphs.

Two results of these simulations are illustrated in figures 3(a) and 3(b) which show the dependencies of the drain-source current I_D on the tunnel oxide thickness d_T and the NP diameter d_{NP}, respectively. The current oscillations are a direct consequence of the Coulomb blockade for an increasing number of charges in the Si ND.

From these simulations it became clear that

- Tunnelling thicknesses close to 1 nm ($d_T \leq 1.2$ nm) on both sides are necessary to achieve a tunnelling current I_D of at least a few pA.
- The diameter of the NP should be $d_{NP} \leq 12$ nm to enable a tunnelling current I_D of about 1 pA at a reasonable gate-source voltage V_G.

Under these conditions, a thickness of $d_{ox} \leq 5.5$ nm was targeted for the oxide sandwiched between the Si source and drain electrodes. The outer oxide isolates the pillar from the gate electrode, its thickness should be 3 nm $\leq d_{SO} \leq 5$ nm to avoid gate-drain and gate-source short circuits for gate voltages V_G up to 3 V.

Moreover, the Si ND represents a quantum dot that is characterized by energy-level-splitting in the conductance band. The discretization of the energy levels is determined by

$$\Delta E_{Q,n} = \frac{\hbar^2\pi^2n^2}{2m^*d_{ND}^2} \qquad (2)$$

where $n \geq 1$ is the ordering number of the discrete level, m^* the Si effective carrier mass, T the temperature; $\hbar = h/2\pi$ the reduced Planck constant. To maintain the equidistant Coulomb oscillations as shown in figure 3, it is favourable that the energy difference between the ground state and the first level exceeds the value of the Coulomb blockade, that is

$$\Delta E_{Q,2} - \Delta E_{Q,1} > E_C > 10kT \qquad (3)$$

For Si NDs of approximately 3 nm in diameter (and even more for smaller ones), this condition is fulfilled as the bandgap widening for such QDs exceeds 0.5 eV [33].

In order to address the SET limitations, mainly the low current level (see figure 3(a)), its co-integration with a FET is favorable. The *I-V* characteristics of a hybrid SET/FET circuit (see figure 4(a)) proposed by ref. [26] was simulated for a ND-SET/vNW-based FET configuration using BSIM-CMG models [34].

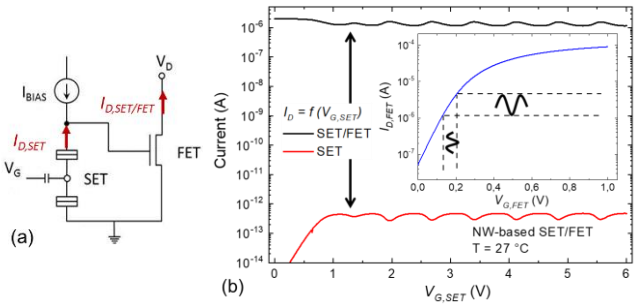

Figure 4. (a) Schematic of the hybrid SET-FET circuit; (b) I_{DS} currents of the SET and the vNP-based hybrid SET-FET circuit. The inset illustrates the sub-threshold operation of the FET and the amplification of the Coulomb oscillations. For details, see ref. [35].

As shown in figure 4(b), the SET current is significantly amplified by six orders of magnitude by the FET operating at sub-threshold level.

The simulation tools and models also allow to study the influence of variations of critical dimensions, such as tunnelling distances, the ND size or its lateral position, on the device characteristics. Results of such simulations were published in refs. [35],[35]; some aspects with respect to experimentally observed deviations to targeted values are separately discussed in section 5.5 of this paper.

3. Simulation of Si ND formation in a confined oxide volume

The formation of Si nanoclusters in Si rich oxides by thermally stimulated phase separation and Ostwald ripening has been demonstrated in numerous studies, for example [37]-[40] and references therein, a recent review paper [41] or summarized in chapters 9-13 of the textbook "Silicon Nanocrystals" [42] edited by Pavesi and Turan. The new aspect addressed in this work is to realize a single, self-assembled Si ND or only very few ones in the oxide of a vertically stacked $Si/SiO_2/Si$ pillar for SET applications. The basic approach to achieve this goal is to limit the volume of phase separation to a few hundreds of cubic nanometers, which corresponds well with the targeted volume of the oxide disc within the NP, as derived in the previous section.

Several techniques, including reactive magnetron sputtering, chemical vapor deposition and SiO evaporation, can be used to fabricate thin Si-rich oxide layers as matrices for subsequent phase separation. Here, we apply the method of ion-beam mixing at Si/SiO_2 interfaces [43],[44] to enrich the initial stoichiometric SiO_2 with Si. The excess Si content and its profile could be easily controlled by varying the irradiation fluence. Mixing of the $Si/SiO_2/Si$ stack is carried out by using chemically neutral Si ions at sufficiently high energy so that the ion penetration depth significantly exceeds the stack thickness.

For the synthesis of Si NDs within the oxide of a NP, two basic scenarios were considered. One option is to perform ion-beam mixing and subsequent annealing in pre-structured NPs. However, recent experiments revealed that RT ion irradiation at the required fluence deteriorates the stacked NPs by amorphization, leading to substantial NP shape changes during ion irradiation due to viscous flow of silicon [45]. This effect can be suppressed by performing ion irradiation at elevated temperatures (> 400 °C), which preserves the crystalline morphology of the Si regions in the stacked NP. We discarded this option because most implantation tools in standard wafer process lines do not allow ion irradiation at temperatures above 400 °C. Consequently, we chose to apply ion-beam mixing to a planar layer stack prior to electron-beam patterning and pillar etching. In this case, the volume of the mixed oxide disc is determined by the pillar dimensions after etching. Phase separation and dot formation are accomplished during subsequent annealing at temperatures up to 1100°C which is viable owing to the high thermal and mechanical stability of the pillars.

The modelling of this process sequence is accomplished in two steps, with dynamic collisional computer simulations of ion-induced atomic mixing using TRIDYN [46],[47] and subsequent kinetic Monte Carlo (kMC) simulations of the phase separation and ND formation. The accumulation of Si in the oxide interlayer during ion-beam mixing is illustrated in figure 5 which shows the depth profiles of excess Si in the oxide that develops under 50 keV Si^+ irradiation. The Si excess atomic fraction is defined as [48]

$$q_{Si}^{exc} = \frac{n_{tot}(x)}{2n_{Si}^0} \cdot (3q_{Si}(x) - 1) \qquad (4)$$

where $n_{tot}(x)$, n_{Si}, q_{Si} denote the total (Si+O) atomic density, atomic density of crystalline Si (= 5×10^{22} at/cm³), and Si atomic fraction, respectively. For SiO_2, SiO and pure Si, q_{Si}^{exc} amount to 0, 0.43 and 1, respectively. The profiles demonstrate significant ion-induced atomic mixing in the regions of both interfaces. The almost symmetric excess Si profiles in the oxide indicate a similar mixing efficiency at both interfaces, which is assured by the choice of the ion energy. In addition, there is a minor shift in the profile towards the surface which increases with increasing fluence. This is attributed to the deposition of implanted Si ions behind the oxide interlayer. (Note that the depth scales of figure 5 have already been corrected for surface erosion due to sputtering.)

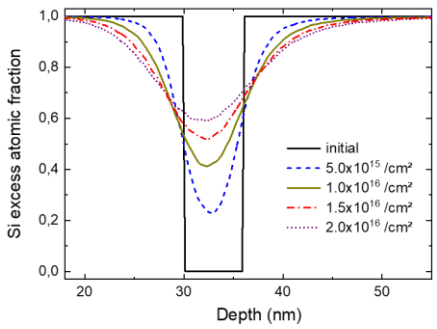

Figure 5. Si excess depth profiles in a planar 30 nm Si / 6 nm SiO_2 / Si stack irradiated with 50 keV Si^+ ions at different fluences, as obtained from TRIDYN computer simulation. The depth scale is individually corrected for the sputter loss of the outer Si layer, which is around 1 nm/10^{16} ions/cm². For the definition of the Si excess atomic fraction, see equation (4)

The excess Si in the oxide continuously increases with the irradiation fluence, converting the initial SiO_2 into an SiO_x layer with a depth-dependent x value. As concluded from the subsequent kMC simulations, a stoichiometry of $x \approx 1$ at the centre of the oxide layer optimizes the formation of well-separated Si NDs. This is achieved for a fluence of ~ 1×10^{16} /cm² which is a reasonable value with respect to the sputter loss of the upper Si layer (~ 1 nm/10^{16} ions·cm^{-2}) as well as the irradiation time (a few minutes). The maximum excess Si close to the oxide center is beneficial for phase separation and Si ND formation. However, a recent study by Prüfer *et al*. [49] showed that TRIDYN overestimates the interface broadening of the mixed Si profile, in particular for higher implantation fluence. This deviation is attributed to the neglect of chemical driving forces in connection with thermal-spike-induced diffusion during ion irradiation, which tends to reconstitute the Si/SiO_2 interfaces. Accordingly, it is proposed to increase the fluences of the TRIDYN simulations by a scaling factor of ~ 1.5 in the fluence range of interest [49]. Thus, an irradiation fluence of ~ 1.5×10^{16} /cm² appears to be appropriate for our purposes.

The excess Si depth profiles in the oxide (figure 5) were used as inputs for 3D kinetic Monte-Carlo simulations of phase separation and Si ND formation [50],[51]. Figure 6 shows a set of kinetic Monte Carlo (kMC) simulations of Si ND formation after thermally driven $SiO_x \rightarrow Si + SiO_2$ phase separation for stacked NPs of different diameters. It is evident that the number of precipitated Si NDs successively decreases towards lower pillar diameters. A single Si ND is formed for a strongly confined SiO_x volume of approximately 500 nm³. For an oxide layer of 6 nm thickness, this volume corresponds to a NP diameter of about 10 nm.

The vertical ND self-alignment almost at the oxide center results from the symmetrical mixing effect at the upper and lower Si/SiO_2 interfaces. The final Si NDs form with a size of 2 – 3 nm which agrees well with the preconditions for quantum confinement and RT operation of the SET, as set out in section 2. The very low diffusion coefficient of Si or SiO in the oxide enables small tunnelling distances and a sufficiently large thermal budget process window for the stable existence of Si NDs (see sections 5.1 and 5.5). The kMC simulations also revealed the recovery of smooth Si/SiO_2 interfaces and a remarkable rounding of Si/SiO_2 rims. The latter effect improves the electrostatic control of the ND and increases the drain-gate or source-gate breakdown stability.

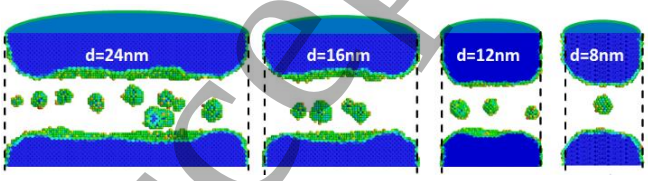

Figure 6. Set of kMC simulations of SiO_x phase separation and SiND formation in cylindrical $Si/SiO_x/Si$ nanopillars of different diameters. The Si NDs projected in the front plane represent their number in the full oxide disc. The color of the Si atoms represents its energy (blue: complete bonding in a diamond lattice, green:partly coordinated, red: dissolved as monomer in SiO_2). The oxide is transparent.

4. Experimental

4.1 Process flow of NP/ND fabrication

Industrial, silicon wafer-level processes were employed on a front-end 200-mm CMOS line to ensure a high throughput and reproducibility of NP fabrication. The basic process flow is illustrated in figure 7 and mainly consists of the preparation of the planar layer stack, ion-beam mixing for SiO_x formation, electron-beam lithography (EBL) for sub-100 nm patterning, multistep reactive ion-beam etching (RIE) using a hard mask for pillar fabrication and thermal processing for SiO_x phase separation and Si ND formation. The final plasma oxidation step was used for NP shrinkage and gate oxide growth.

For the experiments described here, mainly low-resistivity, n-type bulk-Si material was used. In parallel SOI wafers with 200-nm top-Si and 400-nm buried oxide (BOX) necessary for the fabrication of integrated SET/FET devices were processed, too. The thickness of the thermal oxide was varied between 5 nm and 8 nm to optimize the Si ND size and tunnelling distances. As the top layer, undoped amorphous Si of 30 nm thickness was deposited by low-pressure chemical vapor deposition (LPCVD), and subsequently doped by low-energy phosphorous implantation. For ion-beam mixing, RT irradiations were performed using 50 keV Si^+ ions at a fluence of 1.5×10^{16} /cm² (i.e. with parameters as described in section 3) and at an angle of incidence of 7° with respect to the surface normal. For the subsequent dry RIE step the SOC/SiARC acted as a hard mask. Isotropic resist trimming was additionally applied before etching to reduce the NP diameter. Details of this lithography/etching scheme were recently published by Pourteau *et al.* [52]. The subsequent annealing step was performed using a rapid thermal processing (RTP) tool. A two-step sequence at 800 °C for 10 s followed by 1050 °C for 60 s or 120 s was applied. The intermediate annealing step at 800 °C was included to transform the amorphous top Si cap into poly-crystalline Si and to recrystallize the amorphous zone in the bulk Si caused by ion-beam mixing.

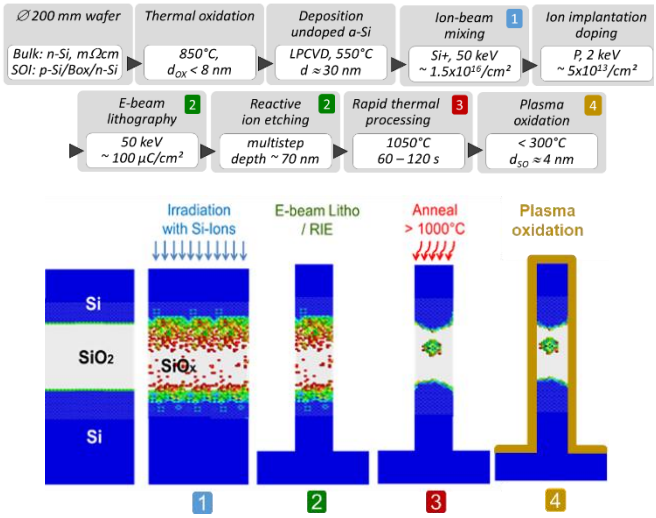

Figure 7. Processing scheme to fabricate stacked $Si/SiO_2/Si$ NPs with Si NDs embedded in the oxide. The key steps are sketched at the bottom.

Generally, the heating rate was fixed at 25 K/s, whereas the temperature profile during cooling followed an exponential decay as the wafers were not actively cooled. The necessity and details of the final plasma oxidation step are described in section 5.3.

To enable a systematic study of ND/NP fabrication and the reliability of lithography and etching steps, NPs of various size and with different distances were arranged in pillar arrays of 5 × 5 µm² size each. Stand-alone NPs – so called isolated pillars (IP) – were processed in parallel. The nominal NP diameter (denoted as critical dimension (CD)) was varied between 30 nm and 100 nm, whereas inter-pillar pitch distances between 60 nm and 1 µm (i.e. from 2x CD to 10x CD) were chosen. Several hundreds of such pillar arrays are regularly distributed across a wafer, enabling conclusions about the scalability of the technology and statistical variation of the CDs. More information regarding the lithography wafer layout is provided in the supplemental material S1 of this paper.

4.2 Structural characterization

Various state-of-the-art electron and ion microscopy techniques have been applied to the visualization and chemical analysis of nanostructures. In particular, structural characterization of the NPs and Si ND formation studies was carried out using an image-*Cs*-corrected Titan 80-300 transmission electron microscope equipped with a Gatan Imaging Filter (GIF) Tridiem 863. While the NP dimensions can routinely be obtained using bright-field transmission electron microscopy (TEM), the detection of single Si NDs of 2 – 3 nm diameter inside an amorphous SiO_2 matrix is challenging, because it requires likewise sufficient contrast (i.e. signal-to-noise ratio) and sub-nm resolution. Bright-field and annular dark-field TEM do not meet these two requirements, and high-resolution TEM can only map Si nanocrystals oriented in a low-index zone axis. Energy-filtered TEM (EFTEM), using the specific plasmon loss of Si or SiO_2, was found to be the most appropriate method to enable a distinct contrast between Si and SiO_2 and to image randomly oriented Si NDs in a SiO_2 matrix [53]. EFTEM micrographs were recorded at energy loss windows of (17 ± 3) eV and (24 ± 2) eV corresponding to the Si and SiO_2 plasmon losses, respectively. Most TEM images were obtained from cross-sectional specimens prepared by focused ion-beam thinning.

For imaging of the entire NP array (or parts of it), scanning electron microscopy (SEM) or helium ion microscopy (HIM) under tilted incidence conditions (typically 45° – 60°) were applied. For SEM either a Helios NanoLab 1200HP or an NVision 40 were used, whereas HIM images were recorded with 25 keV helium ions in an ORION NanoFab instrument.

5. Results and discussion

5.1 Ion-beam mixing and SiO_x phase separation

As derived in section 2, high-dose Si^+ ion irradiation with a fluence of 1.5×10^{16} /cm² is required to transform the initial SiO_2 layer within the stack into SiO_x ($x \approx 1$). This fluence leads to the amorphization of the Si bulk below the oxide up to a depth of about 120 nm. Generally, the amorphization is uncritical as the substrate fully recrystallizes by epitaxial regrowth during subsequent RTP. When using SOI wafers, the top Si thickness must be larger than the amorphization depth to maintain a mono-crystalline seeding layer above the BOX for solid phase epitaxial regrowth.

An important issue is the influence of ion-beam mixing on the quality of SiO_2/Si interfaces. Figure 8(a-c) depicts a sequence of EFTEM micrographs showing the Si/oxide interfaces before and after irradiation and after annealing, respectively. As expected from the TRIDYN simulations (see figure 5), ion irradiation leads to blurring of the Si/oxide interfaces and an Si accumulation in the oxide from both sides. This is caused by the continuous mixing of Si into the oxide and oxygen into the adjacent Si regions. The subsequent annealing step (T > 1000 °C) provokes Si and SiO diffusion as well as phase separation, leading to Si ND formation and the recovery of Si/SiO_2 interfaces [54],[55]. The relative Si depth profiles derived from line-scans of the Si-plasmon-loss-filtered TEM micrographs are shown in figure 8(d). They clearly reveal the mixing effect: the Si content in the oxide after mixing is significantly increased, and the still existing Si excess after annealing is caused by the presence of Si NDs which is indicated by the slight profile bump in the center of the oxide. NDs are also seen as bright spots in figure 8(c).The strong recovery of the Si profile after annealing indicates that most of the excess Si condensates at Si/SiO_2 interfaces during thermal treatment. The almost identical profile slopes of the as-deposited and annealed samples in figure 7(d) confirm the reconstitution of sharp interfaces after annealing.

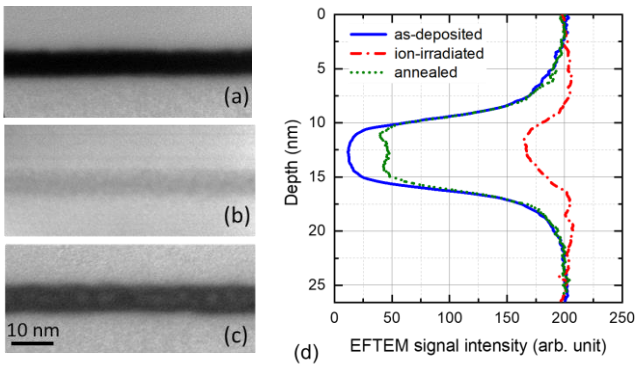

Figure 8. Sequence of Si-plasmon-loss-filtered TEM micrographs, showing the Si/SiO_2 interface regions of an 30 nm a-Si / 7 nm SiO_2 / bulk c-Si stack before (a) and after (b) ion irradiation as well as after annealing at 1050 °C for 60 s (c). Graph (d) displays normalized Si depth profiles as extracted from grey-scale values of EFTEM images (a) - (c) laterally averaged for regions of 15 nm width each. Note that this investigation has been carried out at a layer stack without NP patterning.

The parameters for the annealing step, required for phase separation and Si ND growth were investigated in detail by Xu *et al.* [56] defining a thermal budget parameter *TB*

$$TB = D_0 \int \exp\left(-\frac{E_a}{kT(t)}\right) dt \;\cong\; D_0 t \cdot exp\left(-\frac{E_a}{kT}\right) \qquad (5)$$

where D_0 and E_a denote the diffusion coefficient and activation energy of the relevant SiO diffusion in SiO_2, respectively (D_0 = 4x10^4 cm²/s and E_a = 6.2 eV) [54]. In the case of a negligible thermal budget during heating/cooling this equation has a simple exponential form, as shown on the right side of equation (5). Zhou *et al.* [56] determined a suitable process window of *TB* = (0.7 – 2.1)×10^{-17} cm² for the generation of Si NDs with a size of 2 – 3 nm. Although this study was performed for an unpatterned 2D layer stack, this *TB* value should also be a reasonable choice for the case of phase separation within the stacked NP considered here. The reason is the distinctly smaller distance of diffusing excess Si (or SiO) for condensation at both Si/SiO_2 interfaces compared to the outer pillar rim. For the excess Si fraction close to the rim the situation might be different, but this finally only favours the formation of NDs in the NP center which is a beneficial effect for single Si ND formation. Consequently, for the experiments described in this paper, RTP was usually carried out at 1050 °C and with times of 60 s or 120 s corresponding to *TB* = 0.6×10^{-17} cm² or 1.1×10^{-17} cm², respectively.

A critical issue is the right choice of the annealing ambient. After annealing in pure nitrogen (grade 6.0) at 1050 °C, pitting at the pillar walls and pillar cap as well as at the bottom Si substrate bottom besides the NPs was observed (figure 9). These defects were not present directly after the NP etching before annealing. As a result of detailed investigations, excluding other reasons such as thermally activated etching by halogen residuals from RIE, these defects are most probably caused by the formation of volatile SiO(g) from traces of humidity or oxygen in the annealing environment [57]. Options to circumvent this artifact are to use either a diluted mixed N_2/O_2 atmosphere (oxygen content 1-2 vol.%) to favour sacrificial SiO_2 layer formation or to protect the NP by a thin SiO_2 film deposited before the RTP anneal, e.g. by low-temperature plasma-enhanced atomic-layer-deposition. In the latter case, post-annealing can be carried out in pure N_2 atmosphere.

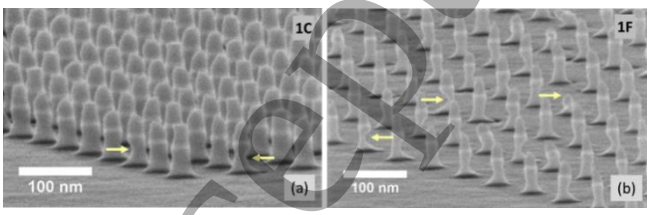

Figure 9. HIM micrographs of pillar arrays 1C (a) and 1F (b) after annealing at 1050 °C, 60 s in pure N_2. NP dimension and pitch within the arrays are as follows: 1C: 30 nm / 90 nm: 1F: 30 nm / 210 nm. Critical features are marked by yellow arrows.

[a] See supplemental material S2 for detailed information.

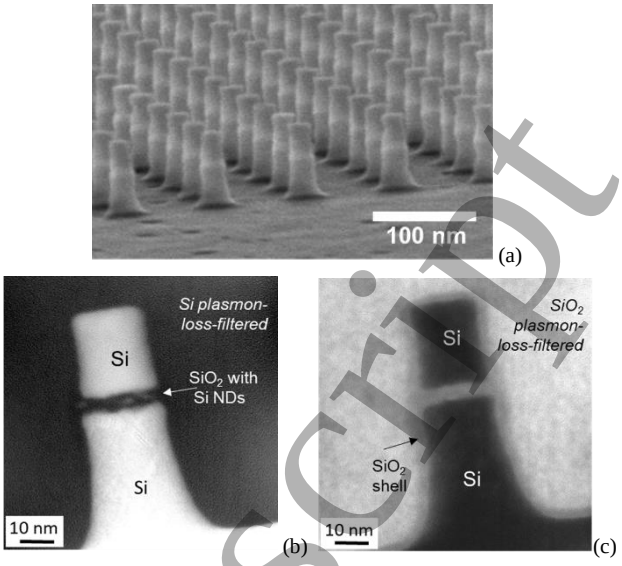

Figure 10. NPs after annealing in an N_2/O_2 = 99/1 vol.% atmosphere at 1050 °C for 60 s: (a) HIM image of an array with CD = 30 nm and a pitch of 90 nm × 90 nm, and (b-c) EFTEM images of a single identical NP with Si-plasmon-loss (b) and SiO_2-plasmon-loss (c) filtering. The formation of several Si NDs in the oxide is confirmed in (b).

Both methods were successfully applied, yielding almost defect-free NP arrays, as shown in figure 10 for the case of annealing in N_2/O_2 mixed ambient. The oxide grown around the pillar with a thickness of of (3 ± 1) nm (see figure 10(c)) is acceptable for further processing. The use of N_2/1%O_2 annealing is not detrimental to the formation of Si NDs in the center of the oxide, as proven by EFTEM imaging (see figure 10(b)).

A second advantage of using mixed N_2/O_2 is the prevention of silicon-oxynitride formation at the outer Si NP rim which was confirmed by analytical TEM[a] after annealing at 1050°C in pure N_2. The $Si_xO_yN_z$ films can only be removed by plasma or RIE dry etching with limited selectivity for other materials which is a critical issue for subsequent SET gate oxide formation and drain metallization.

5.2 NP morphology control

The device simulations in section 2 show that SET operation requires a final NP diameter of < 12 nm. Therefore, NP arrays of various dimensions were investigated to determine the limits of the lithography/etching/annealing processes applied for the fabrication of defect-free NPs. Pillar arrays with CD = 30 nm and 60 – 300 nm pitch were of particular interest to elucidate pillar topology and the Si ND formation within the smallest NPs.

A first observation revealed that the NP diameter after RIE became a function of the NP pitch, as shown in figure 11(a). Note that resist trimming generally led to NP diameters smaller than the EBL designed CD values [52]. Starting from an NP diameter of about 28 nm, obtained for an array pitch of 60 nm, it shrinks with increasing pitch down to a diameter of

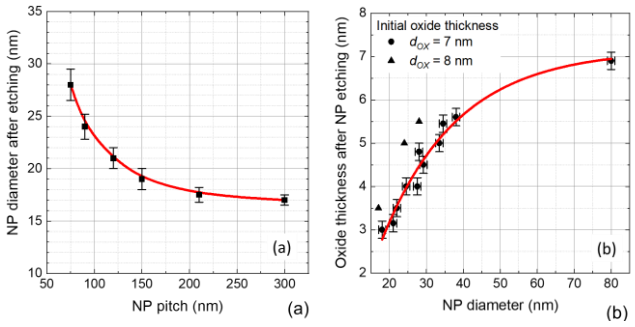

Figure 11. (a) NP diameter for pillars of array 1 (CD30) after RIE etching and subsequent RTA (1050 °C, 60 s, N_2/O_2 = 99/1 vol.%), (b) reduction of the intermediate oxide thickness for stacked $Si/SiO_2/Si$ pillars of various diameters and ~ 80 nm total height.

17 nm. Above 200 nm pitch, the shrinkage saturation represents the situation of stand-alone pillars. This shrinkage effect was caused by the simplified lithographic workflow at which electron-beam proximity correction was not applied before exposure of negative EBL resist. This results in overexposed patterns at small pitch values due to locally scattered electrons. As a second effect, a reduction in the oxide layer thickness for decreasing NP diameters was observed (figure 11(b)). The thickness reduction can be explained by the charging of the NP cap during the final phase of pillar etching, leaving the upper Si-cap electrically isolated. This charging leads to local breakdowns and SiO emanation at the rim of the oxide [58]. The easiest option to compensate for this oxide shrinkage is to increase the initial oxide thickness within the stack. Another technical option is the isolation of the entire wafer during RIE.

The investigations described so far show that sub-30 nm NPs can be realized by direct EBL and RIE etching. However, the yield of defect-free pillars rapidly decreased to < 50% for stand-alone NPs less than 20 nm in diameter. Main artifacts are the removal of the top Si cap, NP bending, or a strong trapezoidal shape of the stacked pillars.

5.3 NP shrinkage technology

As a consequence of the yield drop of sub-20 nm diameter NPs after RIE, an additional process step is necessary to shrink the NP size from ~ 20 nm to the targeted diameter of < 12 nm. A common technique for reducing the size of Si nanostructures is sacrificial oxidation [59],[60]. Usually by thermal oxidation, the surface of the Si nanostructure is oxidized with consumes a Si layer of $d_{Si} = 0.44 \cdot d_{ox}$ thickness by conversion into SiO_2. This oxide layer can be selectively removed by HF, resulting in a reduction of the initial nanostructure dimension. Accordingly, the NP diameter reduction was tested using rapid thermal oxidation at temperatures between 850 °C and 1050 °C. However, a closer look at NPs with an initial diameter of < 20 nm by EFTEM showed the dissolution of the existing Si NDs during this treatment, which is attributed to Si ND oxidation[b]. This can be avoided using the microwave-based plasma oxidation technique operating at temperatures

[b] See supplemental material S3 for detailed information

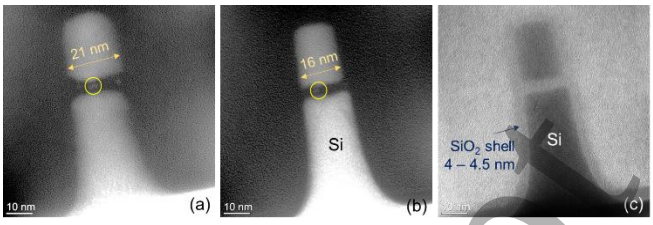

Figure 12. Si-plasmon-loss-filtered EFTEM images before (a) and after (b) a single plasma oxidation (He/O_2 = 85/15vol%, 35 Pa, 2 W/cm²) for 90 s (250°C max.). The initial 20-nm NP diameter reduces to 16 nm. The EFTEM image after plasma processing (b) confirms the existence of a Si ND (marked by a circle). (c) SiO_2-plasmon-loss-filtered EFTEM image of the pillar shown in (b) confirming the uniform formation of an ~ 4.2 nm oxide around the NP.

< 400 °C [61],[62]. Plasma oxidation provides oxides of up to ~ 8 nm in thickness and high electrical quality [63],[64] at reasonable oxidation times of some minutes. In collaboration with the company HQ Dielectrics GmbH (HQ-D), experiments were performed with the HQ-D Hyperion^{LT} tool [65] (suitable for processing up to □ 300-mm wafers) to qualify the plasma process for the oxidation of NPs. Oxidation was performed in a microwave plasma (2.45 GHz) using O_2/He gas ratio of 85/15 vol.%, a working pressure of about 35 Pa and a power density of 2 W/cm^2.

Figure 12 shows the uniform oxidation of NPs and the preservation of the Si NDs after plasma oxidation. Remarkably, the thickness of the intermediate oxide layer in the $Si/SiO_2/Si$ sandwich did not change. Limiting the processing temperature to < 350 °C and staying within the linear oxidation regime, an oxide layer up to 6 nm thickness around the NP can be realized. This corresponds to an NP diameter shrinkage of approximately 5 nm per oxidation cycle. As the procedure can be repeated after removing the oxide by an HF dip, NPs with a final diameter of < 12 nm can be obtained by single or multiple plasma oxidation, depending on the initial NP diameter. The use of plama oxidation provides another advantage: the same technology can be used to grow the gate oxide required for a gate-all-around SET (see figures 2 and 7). A breakdown field > 10 MV/cm was measured at planar MOS structures for a gate oxide of 3 nm thickness produced by plasma oxidation.

5.4 Towards a single Si nanodot

Figure 13 depicts a sequence of EFTEM images of isolated NPs with diameters varying between 35 nm and 18 nm, which were fabricated from the same layer stack of Si (30 nm)/SiO_2 (6 nm)/Si under identical ion-beam mixing, pillar etching and annealing conditions. The corresponding NP/ND features are summarized in table I.

The number of Si NDs decreases with decreasing NP diameter, which is in close agreement with kMC simulations (see figure 6). In most pillars Si precipitates could be detected, except for a final oxide thickness of ≤ 3 nm. In this case the oxide thickness is too small to generate a Si ND of 2 – 3 nm as it immediately dissolves by de-wetting if touching the Si/SiO_2 interface.

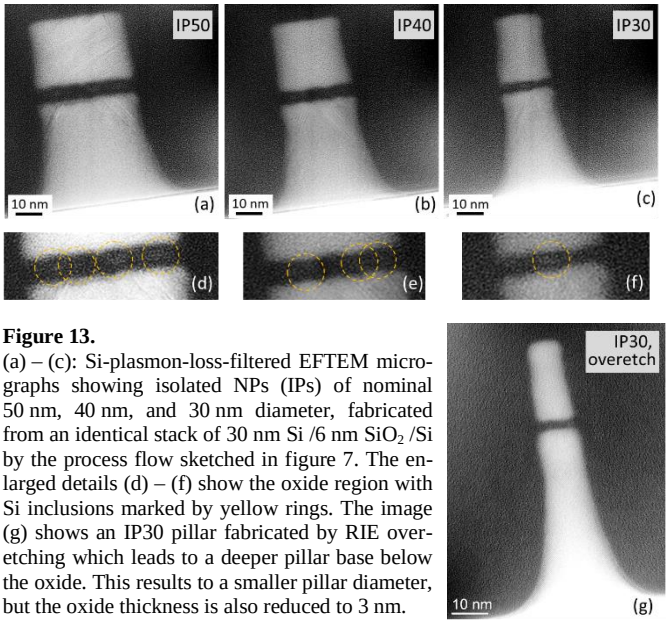

Figure 13.
(a) – (c): Si-plasmon-loss-filtered EFTEM micrographs showing isolated NPs (IPs) of nominal 50 nm, 40 nm, and 30 nm diameter, fabricated from an identical stack of 30 nm Si /6 nm SiO_2 /Si by the process flow sketched in figure 7. The enlarged details (d) – (f) show the oxide region with Si inclusions marked by yellow rings. The image (g) shows an IP30 pillar fabricated by RIE overetching which leads to a deeper pillar base below the oxide. This results to a smaller pillar diameter, but the oxide thickness is also reduced to 3 nm.

Table I: Values for the effective NP diameter d_{NP}, the oxide thickness d_{ox} and number of NDs in the pillars of figure 13 including also the cases IP45 and IP35 not shown there.

Parameter	Unit	IP50	IP45	IP40	IP35	IP30	IP30,oe
d_{NP}	nm	37,0	33,0	27,5	21,7	18,6	10,5
d_{ox}	nm	5,6	5,4	4,8	4,2	3,8	3,0
# ND (min)		3 - 4	3	3	2	1 -2	0
figure 11		**(a),(d)**		**(b),(e)**		**(d),(f)**	**(g)**

Considering all aspects described before, we successfully produced stacked $Si/SiO_2/Si$ NPs < 12 nm in diameter with a single Si ND embedded in the oxide. This is illustrated in figure 14, which shows the EFTEM image of a NP of (11 ± 1) nm diameter with a single Si ND in the center of the 3.7 nm thin SiO_2 disc formed by the self-organization and self-alignment mechanisms discussed in section 3. The ND has a diameter of 2.5 nm, the tunelling widths are ≤ 1.2 nm which suggests the ability for SET operation at RT.

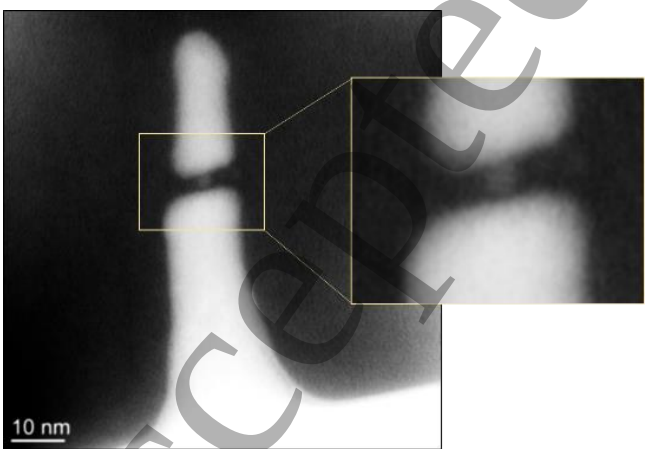

Figure 14. EFTEM (Si-plasmon-loss-filtered) image of a NP of about 11 nm in diameter with a single Si ND embedded in the centre of the thin 3.7 nm thin oxide. The enlarged detail on the right confirms a size of the almost spherical Si ND of 2.5 nm and tunnelling distances to neighboured Si regions of about 1 nm.

The widening of the oxide layer at the pillar rim is in agreement with the targeted layout and predictions by kMC simulations (see figure 6), which is advantegeous for the reduction of the electrical field strength at the gate region. The results provide a proof of the manufacturability of vertically stacked NPs with embedded Si NDs and reveal that the tunnelling distances close to 1 nm can be achieved.

5.5 Impact of NP/ND parameter variations

The NP/ND manufacturing process at sub-20 nm level decribed in previous sections as well as the statistical nature of SiO_x phase separation and Si ND formation results in some variations of the number of Si NDs as well as their size and lateral position in the oxide. Because of the strong geometrical constraints in the NP, these variations are generally small. It is outside the scope of this paper to discuss this matter here (for details see refs. [35],[35]), but let us briefly consider four experimentally observed situations, their consequences for SET or SET/FET operation and possibilities to balance such variations.

i. The tunnelling transmission coefficient exponentially depends on the tunnelling distance. Thus, the most critical parameter is a very thin tunnel distance d_T of about 1 nm to achieve SET currents in the pA range (see figure 3). A variation of 10% in the tunnelling thickness will change the SET current by one order of magnitude [35]. For the hybride SET/FET circuit such a variation modifies the FET drain-source current by 20% [35],[35]. Any asymmetry of the upper/lower tunnelling distances will also considerably lower the SET current, as shown in figure 15(a). How one can reduce and unify tunnelling distances? The very low diffusion coefficient of Si or SiO in SiO_2 ($D \approx 10^{-21}$ cm²/s @ 1050 °C, see [54],[66]) implies a low diffusional screening length which is essential to enable tunnelling distances of about 1 nm or even slightly below (see figure 14). Thus, a reduction of the oxide thickness one can expect a stronger localization of Si NDs with respect to both Si/SiO_2 interfaces and the unification of tunnelling distances.

ii. Simulations reveal that the ND shape (spherical, elliptical or elongated) has only a minor influence on the SET current as shown in figure 15(b). Flattened NDs, which is the most observed variation in the ND shape due the the vertical confinement, requires lower V_G voltages. The SET current is almost constant as long as the tunnelling distance remains small enough and as long the conditions of equations *(1)* and *(3)* are still fulfilled.

iii. Furthermore, the lateral position of a single Si ND may deviate from the oxide center. This increases the gate-dot capacitance C_{GD} and slightly lowers V_G which is beneficial for SET operation.

iv. It is also possible that more than one (typically 2 – 3) NDs forms, particularly for larger NPs of > 15 nm diameter.

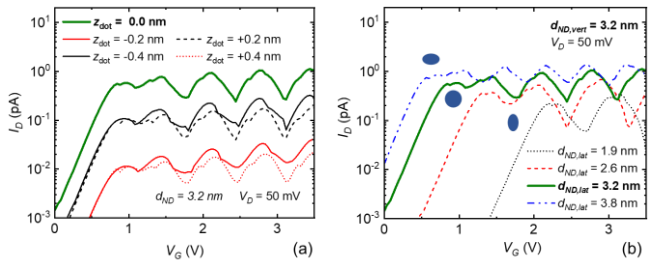

Figure 15. Influence of vertically asymmetric ND position (a) or a laterally shaped ND on the SET current (b). Fixed parameters are d_{OX} = 5.6 nm, d_{NC} = 10 nm; d_{ND} = 3.2 nm and V_D = 50 mn.

Within a small ensemble of NDs the tunnelling distances will not exactly be identical which has a strong impact on the SET current. Consequently, a self-selection of a specific ND characterized by the lowest tunnel barrier will happen. Moreover, there is also a technological way to favour a single, centered Si ND. It has been experimentally shown (see supplemental material S3) that annealing in a strongly diluted N_2/O_2 ambient dissolves Si NDs close to the rim of the NP while preserving near-centered NDs. Optimization of the oxygen content in the annealing ambient and the thermal budget will favour the formation of single NDs in cases that the NP dimension exceeds the 10 nm diameter level.

In addition to process developments mentioned before, there is also another option as both, SET and FET devices present a vertical topology with high integration capability. This will entail the the possibility to implement SET arrays connected in parallel that will accont for a suppression of the variability impact [67]. However, further efforts are necessary to reduce the variations in order to achieve a higher technology readiness level.

6. Summary and further work

This paper describes the CMOS-compatible fabrication of $Si/SiO_2/Si$ NPs with embedded Si NDs suitable as key functional elements for a quantum-dot-based, gate-all-around SET. Remarkably, all process steps were carried out using industrial equipment on □ 200-mm bulk Si or SOI wafers, which confirms the manufacturability of the NP/ND structures in a complex wafer flow at a large wafer level.

To realize the ND/NP structures, a novel process flow that combines bottom-up and top-down technologies has been developed. Geometrical constraints and technological process parameters have been derived partly from predictive physical processess and device simulations, partly by using our experimental experience related to the formation of near-interface Si NDs. Finally, the reliable formation of Si NDs < 3 nm in the oxide of a stacked $Si/SiO_2/Si$ NP ≤ 12 nm in diameter with tunnelling distances of approximately 1 nm between the Si ND and the adjacent Si regions could be demonstrated. The impact of critical dimension variations on the SET properties has been analyzed by device simulations. Well defined, symmetric and ultra-thin tunnelling distances (~ 1 nm) have the strongest influence on the SET current. Deviations in the shape of the NDs or their lateral position in the pillar are of less importance. Layout and technological options were discussed to suppress deviations for further improvements.

The work gained at physico-chemical understanding of the self-organization and patterning of nanostructures. This involves processes like ion-beam mixing, phase separation, reactive ion etching or plasma oxidation which might be helpful for future processing in nanoelectronics in general. In particular, the experimental verification of the predicted self-assembly of single Si NDs by phase separation within a confined SiO_x volume of < 500 nm³ and the ability to locate such self-assembled quantum dots within a direct tunnelling distance to a Si electrode is highly relevant for nanoelectronics.

This study limits on the fabrication and structural characterization of NPs/NDs as key functional elements for the SET. In the Ions4SET project [68] further work was carried out to fabricate and electrically characterize NPs with Si NDs and single SETs [69]. Moreover, the entire integration schema for a hybrid SET/FET device was elaborated and tested [30]. An important issue was to verify that the NPs/NDs could withstand the thermal, mechanical and chemical stresses of a complex SET/FET fabrication flow. These investigations reveal that the NPs/NDs maintained their stability during the entire process, if they are embedded in sacrificial Si_3N_4 dielectrics and if the thermal budget during FET processing is limited to 900 °C/3 h, which are acceptable preconditions for state-of-the-art transistor technology.

Acknowledgements

This work received funding from the European Union's Horizon 2020 Research and Innovation Program under grant agreement N° 688072 (project acronym: Ions4SET), which is gratefully acknowledged. The authors thank the Ions4SET Industry Endorsement Board for their continuous support during the project. In particular, the valuable inputs of K.-H. Stegemann (XFAB Dresden GmbH) was very helpful in developing the process flow for ND/NP fabrication and in solving several critical issues related to the processing of nanostructures. The authors thank W. Lerch and J. Niess from HQ Dielectrics GmbH (HQ-D) for providing and performing plasma oxidation at the HQD Hyperion^{LT} tool and their work to qualify this technique for the shrinkage of NPs. Numerous test preparations and extensive analytical work were carried out at the Ion Beam Center (IBC) of HZDR which is gratefully acknowledged.

Data availability statement

The data that support the findings of this study are included in the article, the supplemental material or will be available upon reasonable request from the authors.

Declarations

The authors declare no conflicts of interest. We certify that the paper is an original work, approved by all co-authors, and not

published elsewhere. The study is in agreement with the "DFG rules for good scientific practice" which complies ethics in science.

Supplemental material

Supplemental material is available to provide more information concerning the following items:

S1: Electron-beam lithography layout of pillar arrays and isolated pillars

S2: Si oxynitride formation during high-temperature annealing in pure nitrogen

S3: Aspects of nanopillar shrinkage by thermal oxidation

References

[1] Yuan J S, Lin L, Qutaiba A and Taheri S 2017; Ultra-low-power design and hardware security using emerging technologies for Internet of Things; *Electron.* **6**, 67

[2] Pradhan K P 2022; An introduction to nanoscale CMOS technology transistors: a future perspective; in Semiconductor devices and technologies for future ultra-low-power electronics, edited by Nirmal D, Aijan J and Fay P J; CRC Press 2022,chapter 1,1-28; ISBN 978 1 003 20098 7

[3] Lin X, Yang W, Zhao W; Two-dimensional spintronics for low-power electronics; *Nature Electron.* **2** 274-83

[4] Das S *et al.* 2021; Transistors based on two-dimensional materials for future integrated circuits; *Nature Electron.* **4** 786-99

[5] Ionescu A M and Riel H 2011; Tunnel field-effect transistors as energy-efficient electronic switches; *Nature* **479** 329-37

[6] Nazir G, Rehman Aand Park S J 2020; Energy-efficient tunnelling field-effect transistors for low-power device applications: challenges and opportunities; *ACS Appl. Mater. & Interf.* **12** 47127-63

[7] Zhao X, Lu W, and Del J A 2018; Shrinking the vertical nanowire MOSFET; *www.compoundsemiconductor.net* 52-56 https://mtlsites.mit.edu/users/alamo/pdf/2018/RJ-194%20paper.pdf

[8] Lepedus M 2018; Transistors options beyond 3 nm; Semiconductor Engineering https://semiengineering.com/transistor-options-beyond-3nm

[9] IRDS International Roadmap for Devices and Systems 2020, IEEE 2020 and references therein https://irds.ieee.org/images/files/pdf/2020/2020IRDS_ES.pdf

[10] Larrieu G and Han X L 2013;Vertical nonowire array-based field effect transistors for ultimate scaling; *Nanoscale* **5** 2437-41

[11] Guerfi Y and Larrieu G 2016; Vertical silicon nanowire field-effect transistor with nanoscale gate-all-around; *Nanoscale Res. Lett.* **11** 210

[12] Larrieu G, Guerfi Y, Han X L and Clement N 2017; Sub-15 nm gate-all-around field effect transistors on vertical silicon nanowires; *Solid State Electron.* **130** 9-14

[13] Patel R, Agrawal Y and Parekh R 2021; Single-electron transistor: review in perspective of theory, modelling, design and fabrication; *Microsystem Techn.* **27** 1863-75

[14] Washuber C 1997; About single-electron devices and circuits; Dissertation TU Vienna 01/1997 https://www.iue.tuwien.ac.at/phd/wasshuber

[15] Maeda K *et al.* 2012; Logic operations of chemically assembled single-electron transistor; *ACS Nano* **6** 2798-803

[16] Ihara S, Andreev A, Williams D A, Kodera T and Oda S 2015; Quantum dots in single electron transistors with ultra-thin silicon-on-isolator structures; *Appl. Phys. Lett.* **107** 013102

[17] Stuyck N D *et al.* 2020; An integrated silicon MOS single-electron-transistor charge sensor for spin-based quantum information processing; *IEEE Electr. Dev. Lett.* **41** 1253-56

[18] Zhuang L, Guo L and Chou S Y 1998; Silicon single-electron quantum-dot transistor switch operating at room temperature; *Appl. Phys. Lett.* **71** 1205-07

[19] Shin S J *et al*. 2010; Si-based ultra-small multi-switching single-electron transistor operating at room temperature; *Appl. Phys. Lett.* **97** 103101

[20] Tanahashi Y, Suzuki R, Saraya T and Hiramoto T 2014; Peak position control of Coulomb blockade oscillations in silicon single-electron transistors with floating gate operating at room temperature; *Jap. J. Appl. Phys.* **53** 04EJ08

[21] Zharinov V S, Picot T, Scheerder J E, Janssens E and Van de Vondel J 2020; Room temperature single electron transistor based on a size-selected aluminium cluster; *Nanoscale* **12** 1164-70

[22] Krishnan R 2014; Single electron transistors; *Intern. J. of Scient. and Engin. Res.* **5** 42-48

[23] Rai C, Khursheed A and Haque F Z 2019; Review on single electron transistor (SET): emerging device in nanotechnology; *Austin J. Nanomed. Nanotechnol.* **7** ID:1055, 1-11

[24] Kumr A and Dubey D 2013; Single electron transistor: applications and limitations; *Adv. in Electronic and Electric Engin.* **3** 57-62

[25] Uchida K, Koga J, Ohba R and Toriumi A 2003; Programmable single-electron transistor logic for future low-power intelligent LSI: proposal and room-temperature operation; *IEEE Trans. on Electr. Dev.* **50** 1623-30

[26] Mahapatra S and Ionescu A M 2006; Hybrid CMOS single-electron-transistor device and circuit design. *Artech House.* https://dl.acm.org/citation.cfm?id=1204065

[27] Nakajima A. 2016; Application of single-electron transistor to biomolecule and ion sensors; *Applied Sciences* **6** 94.

[28] Tan Y T, Kamiya T, Durrani Z A K, and Ahmed H 2003; Room temperature nanocrystalline silicon single-electron transistors. *Journal of Appl. Phys.* **94** 633–37

[29] Jehl X *et.al.* 2011; Mass production of silicon MOS-SETs: can we live with nano-devices' variability? *Procedia Computer Science* **7** 266–68

[30] del Moral A *et al.*; CMOS compatible manufacturing of a hybrid SET-FET circuit; submitted for publication in *Journal of Semiconductor Science and Technology* (2022).

[31] Program package: https://www.nextnano.de

[32] Kluepfel J F and Pichler P 2017; 3D simulation of silicon-based single-electron transistors; 2017 Intern. Conf. on Simulation of Semiconductor Processes and Devices (SISPAD), JSAD, pp. 77-80, 2017.

[33] Cho E C *et al.* 2007; Silicon quantum dots in a dielectric matrix for all-silicon tandem solar cell; *Adv. in Optoelectr.* Art-ID: 69578

[34] Aydavosi N, Venugopalan S, Chauhan Y S, Duarte J P, Jandhyala S, Niknejad A M, and Hu, C C 2013; BSIM-SPICE models enable FinFET and UTB IC designs; *IEEE Access* **1** 201–15.

[35] Amat E, Kluepfel F, Bausells J, and Perez-Murano F. 2019; Influence of quantum dot characteristics on the performance of hybrid SET-FET Circuits. *IEEE Trans. on Electr. Devices* **66** 1–7

[36] Amat E, del Moral A, Bausells J, Perez-Murano F, and Kluepfel F 2018; Quantum dot location relevance into SET-FET circuits based on FinFET devices, *2018 Conference on Design of Circuits and Integrated Systems (DCIS)*, pp. 1-5, doi: 10.1109/DCIS.2018.8681478.

[37] Mueller T, Heinig K H, Moeller W 2002; Size and location control of Si nanocrystals at ion beam synthesis in thin SiO_2 films; *Appl. Phys. Lett.* **81** 3049-51

[38] Mueller T, Heinig K H, Moeller W 2002; Nanocrystal formation in Si implanted thin SiO_2 layers under the influence of an absorbing interface; *Mater. Science and Engin. B* **101** 49

[39] Roentzsch L, Heinig K H, Schmidt B and Muecklich A 2006; Experimental evidence of Si MC delta-layer formation in buried und thin SiO films; *Nucl. Instr. and Meth. in Phys. Res. B* **242** 149

[40] Bulyarskiy S Y 2021; A kinetic model of silicon nanocrystal formation; *Silicon* **13** 3321-27

[41] Mangolini L 2013; Synthesis, properties, and applications of silicon nanocrystals; *J. Vac. Science & Techn. B* **31** 020801

[42] Pavesi L and Turan R (Editors) 2010; Silicon nanocrystals: fundamentals, synthesis and applications; Wiley 2010; ISBN: 978-3-527-62996-1

[43] Heinig K H, Mueller T, Schmidt B, Strobel and Moeller W 2003; Interfaces under ion irradiation: growth and taming of nanostructures; *Appl. Phys. A* **77** 17-25

[44] Schmidt B, Heinig K H, Roentzsch L, Mueller T, Stegemann K H and Votintsseva 2006; Ion irradiation through Si/SiO_2 interfaces: non-conventional fabrication of Si nanocrystals for memory applications; *Nucl. Instr. Meth. in Phys. Res. B* **242** 146-48

[45] Xu X *et al.* 2020; Morphology modification of Si nanopillars under ion irradiation at elevated temperature: plastic deformation and controlled thinning to 10 nm; *Semicond. Science and Techn.* **35** 015021 (2020).

[46] Moeller W and Eckstein W 1984; Tridyn – A TRIM simulation code including dynamic composition changes; *Nucl. Instr. Meth. in Phys. Res.* **2** 814-18

[47] The actual version of the code and the user guide is available via HZDR under the following link: https://www.hzdr.de/db/Cms?pOid=21578&pNid=0

[48] Pruefer T 2020; Formation of Si nanocrystals for single-electron transistors by ion-beam mixing and self-organization; Dissertation, TU Dresden https://nbn-resolving.org/urn:nbn:de:bsz:14-qucosa2-709797

[49] Pruefer T, Moeller W, Heinig K H, Wolf D, Engelmann H J, Xu X and von Borany J 2019; Computer modeling of a single-layer nanocluster formation in a thin SiO_2 layer buried in Si by ion mixing and thermal phase decomposition; *J. Appl. Phys.* **125** 225708

[50] Strobel M, Reiss S, Heinig K H and Moeller W 1997; Computer simulation of precipitate coarsening: A unified treatment of diffusion and reaction controlled Ostwald ripening; *Radiation Effects and Defects in Solids* **41** 99-111

[51] Strobel M, Heinig K H and Moeller W 2001, Three-dimensional domain growth on the size scale of the capillary length: effective growth exponent and comparative atomistic and mean-field simulations; *Phys. Rev. B* **64** 245422

[52] Pourteau M L *et al.* 2020; Sub-20 nm multilayer nanopillar patterning for hybrid SET/CMOS integration; *Micro- and Nano-Engin.* **9** 10074

[53] Iacona F, Bongiorno C, Spinella C, Boninelli S and Priolo F 2004; Formation and evolution of luminescent Si nanoclusters produced by thermal anneling of SiO_x films; *J.Appl. Phys.* **95** 3723-32

[54] Uematsu M, Kageshima H and Takahashi Y 2004; Modeling of Si self-diffusion in SiO_2: effect of the Si/SiO_2 interface including time-dependent diffusivity; *Appl. Phys. Lett.* **84** 876-78

[55] Mueller T *et al.* 2004; Multi-dot floating-gates for nonvolatile semiconductor memories: Their ion beam synthesis and morphology; *Appl. Phys. Lett.* **85** 2373

[56] Xu X *et al.* 2018; Site-controlled formation of single Si nanocrystals in a buried SiO_2 matrix using ion beam mixing; *Beilstein J. Nanotechn.* **9** 2883-91

[57] Sodoh K and Naito M 2010; Interfacial reaction of Si islands on SiO_2 during high temperature annealing; *J. Appl. Phys.* **108** 083520

[58] Heinig KH and Engelmann HJ; Private communication, contact via k.h.heinig@hzdr.de

[59] Shir D, Liu B Z, Mohammad A M, Lew K K and Mohney S E 2006; Oxidation of silicon nanowires; *J. Vac. Science & Techn. B* **24** 1333

[60] Yang B, Buddharaju K D, Teo S, Singh N, Lo G Q and Kwong D L 2008; Vertical silicon-nanowire formation and gate-all-around MOSFET, *IEEE Electr. Device Lett.* **29** 791

[61] Taylor S, Zhang J F and Ecclestone W 1993; A review of the plasma oxidation of silicon and its applications, *Semicond. Sci. Technol.* **8** 1426-33

[62] Lerch W, Schick T, Sacher N, Kegel W, Niess J, Czernohorsky M and Riedel S 2016; Low-temperature microwave-based plasma oxidation of Ge and oxidation of silicon followed by plasma nitridation; *ECS Trans.* **72**, 101–14

[63] Joshi P C, Ono Y, Voutsas A and Hartzell J W 2004; Low-temperature growth of thermal quality SiO_2 thin films in high-density He/O_2 plasma generated by RF driven ICP source, *Electrochem. Solid-State Lett.* **7** G62–G64

[64] Czernohorsky M, Seidel K, Kühnel K, Niess J, Sacher N, Kegel W and Lerch W 2017; High-k metal gate stacks with ultra-thin interfacial layers formed by low temperature microwave-based plasma oxidation; *Microelectr. Engin.* **178** 262–65

[65] Detailed information is available via HQ-D homepage: https://www.hq-dielectrics.eu/products/semiconductor-manufacturing-equipments/hyperion-lt

[66] Fukatsu S *et al.* 2003; Effect of the Si/SiO_2 interface on self-diffusion of Si in semiconductor-grade SiO_2; *Appl. Phys. Lett.* **83** 3897- 99

[67] del Moral A, Amat E, Bausells J, and Perez-Murano F. 2021; Benefits of using arrays of vertical nanowire FETs in integrated circuits to mitigate variability; *Semiconductor Science and Technology* **36** 125017

[68] von Borany J (coordinator); Horizon 2020 project Ions4SET (Grant No.688072); Homepage: http://www.ions4set.eu

[69] M54 periodic report of the Ions4SET project https://cordis.europa.eu/project/id/688072/results