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CMOS compatible manufacturing of a hybrid SET-FET circuit

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Abstract

This study analyzes feasibility of complementary metal–oxide–semiconductor (CMOS)-compatible manufacturing of a hybrid single electron transistor–field effect transistor (SET-FET) circuit. The fundamental element towards an operating SET at room temperature is a vertical nanopillar (NP) with embedded Si nanodot generated by ion-beam irradiation. The integration process from NPs to contacted SETs is validated by structural characterization. Then, the monolithic fabrication of planar FETs integrated with vertical SETs is presented, and its compatibility with standard CMOS technology is demonstrated. The work includes process optimization, pillar integrity validation, electrical characterization and simulations taking into account parasitic effects. The FET fabrication process is adapted to meet the requirements of the pre-fabricated NPs. Overall, this work establishes the groundwork for the realization of a hybrid SET-FET circuit operating at room temperature.

Keywords: CMOS, MOSFET, vertical nanopillar, single electron transistor, hybrid circuit

(Some figures may appear in color only in the online journal)

1. Introduction

The current technological maturity of complementary metal–oxide–semiconductor (CMOS) devices is the result of many decades of investigations [1–3]. Device scaling has driven sustained progress in the semiconductor industry, first by reducing the dimensions of planar MOSFET and, more recently, by exploiting the benefits of novel topologies. In the most advanced nodes, three-dimensional (3D) architectures provide a significant increase in integration density, with vertically arranged devices such as nanosheets being the most suitable candidates for future generations [4, 5].

In the context of the Internet of things, ultra-low power consumption devices are required [6]. An example of an electronic

device with low power consumption is the single electron transistor (SET), which is based on defining a quantum dot (QD) between electron reservoirs (figure 1(a)). The QD can be defined either physically [7] or electrostatically [8]. Figure 1(b) shows the equivalent electrical circuit of a polarized SET. The power dissipation of SETs is several orders of magnitude lower than that of most advanced field-effect transistors (FETs) [9], mainly because of their reduced source-drain voltage and extremely low current operation [10, 11]. However, the cryogenic temperature required for its operation and the fact that they are fabricated with processes that are not scalable or compatible with the semiconductor industry limit its practical implementation.

SETs have intrinsic limitations like low output current, which prevents the control of other components of the circuit [12]. In this sense, SETs and MOSFETs are complementary:

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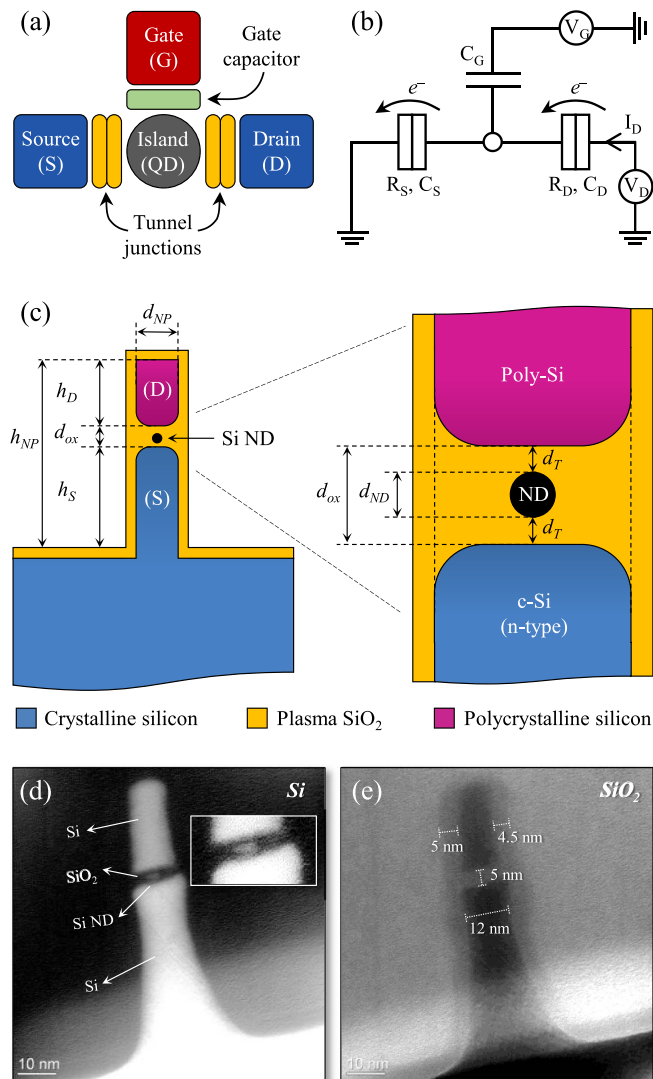


Figure 1. (a) Scheme of the different elements of a SET and (b) corresponding electrical circuit. (c) Sketch of the patterned Si/SiO₂/Si nanopillar, with detail of the inner region with the embedded Si nanodot and the corresponding dimensions in nanometers. (d) Si plasmon-loss-filtered EFTEM image of an example of nanopillar with inset of embedded single Si ND on the SiO₂ layer and (e) corresponding SiO₂ plasmon-loss-filtered image with dimensions.

SET presents advantages for implementing low-power consumption circuits, while FETs have better frequency response and higher voltage and current gain. Thus, a hybrid SET-FET circuit can compensate for SET's intrinsic drawbacks as background noise or device instability, while still keeping advantage for low-power consumption [13–15].

The attainable QD dimensions dictate the ultimate SET performance. In the past, single electron transfer was only observable at cryogenic temperatures [16–18]. However, it has been proven that SETs can operate at room temperature for QDs smaller than 5 nm [19–21]. Additionally, the need for tunneling junctions below 1.5 nm is another constraint, due to the required quantum resistance for single electron transfer.

The requirements for SETs to be CMOS compatible and to operate at room temperature pose extreme challenges in manufacturing technology, representing a roadblock for their integration into CMOS technologies in a controlled and efficient manufacturability. The technology needed to co-integrate SETs and FETs ultimately depends on the ability of new processes to address size and variation issues and to be costly affordable. For that reason, the development of novel methodologies to move forward the state-of-the-art technology is mandatory. Within this context, an innovative solution has been explored in the framework of the Ions4SET EU project [22]: a fabrication process based on ion irradiation-induced self-assembly of Si nanodots (NDs) embedded in a nanopillar (NP) (figure 1(c)). In this configuration, Si ND acts as QD, and the oxide layer in which it is confined within the NP defines the tunnel junctions.

In this work, we present a methodology to manufacture vertical SET devices compatible with CMOS technology. The work is organized as follows. First, in section 2, the process to contact a NP with embedded QD for building up a SET is presented. In section 3, the monolithic, CMOS-compatible fabrication of planar FETs co-integrated with vertical SETs is described. The FET process fabrication is adapted to fulfill the restrictions imposed by the pre-fabricated NPs, such as reduced thermal budget, addition of protective layers and modified doping procedures. Overall, the monolithic fabrication of SETs and FETs is demonstrated: at the end of the process, the pillar integrity is preserved and the FETs conserve adequate electrical characteristics.

2. Vertical SET integration

The first part of the process includes the creation of the Si/SiO₂/Si stack, silicon implantation, NP patterning, Si ND assembly, pillar size reduction and gate oxide fabrication. The details of this part of the fabrication process are presented in related publications [23–26]. The generation of the NDs occurs by the phase separation of metastable SiO_x into Si and SiO₂ within geometric constraint imposed by the thin embedded oxide in the NP. Figure 1(c) denotes the sketch of a vertical NP, with the Si/SiO₂/Si stack and the Si ND induced in the embedded oxide layer. Figures 1(d) and (e) show energy filtered transmission electron microscopy (EFTEM) images of one NP with the embedded Si QD.

Dedicated characterization techniques with nanometer resolution are crucial for a successful process monitoring. We have systematically used atomic force microscopy (AFM) in dynamic mode, scanning electron microscopy (SEM) and high-resolution transmission electron microscopy (HR-TEM). In particular, EFTEM using plasmon-losses of Si and SiO₂ has been key to characterize the NPs as it provides material selectivity with sub-10 nm resolution.

2.1. Vertical SET integration process

The SET integration requires several levels of metal and dielectric layers: a thin gate electrode aligned with the

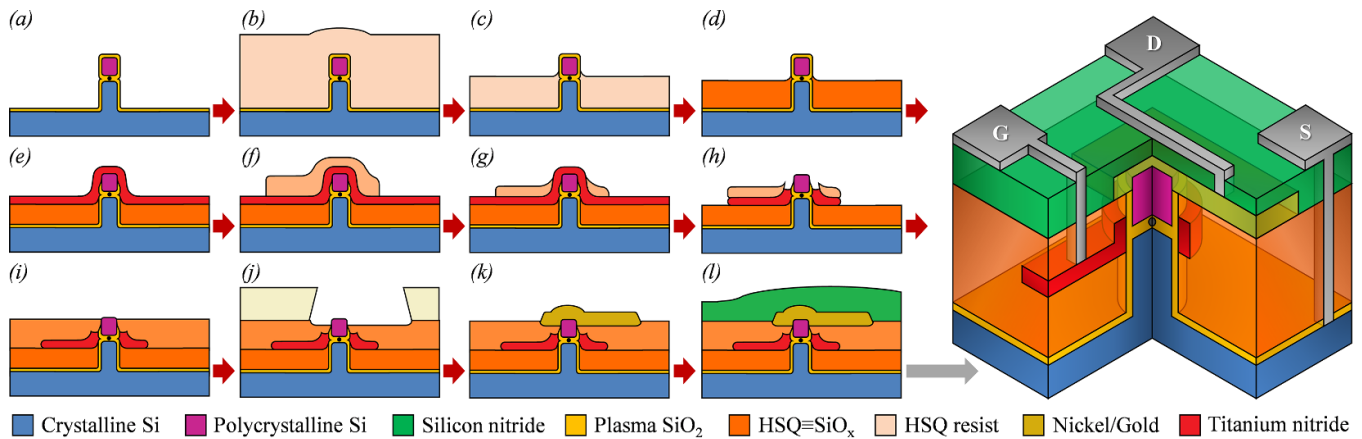


Figure 2. Sequence steps of the SET integration process flow: (a) initial pillar configuration, (b) after HSQ spin-coating, (c) HSQ etched-back and (d) HSQ annealing at 800 °C. (e) After TiN sputtering, (f) HSQ exposure, (g) HSQ mask etched-back and (h) TiN wet etching. (i) After second inter-metal layer annealing at 400 °C, (j) diluted HF for pillar-drain contact, (k) lift-off of Ni/Au metal contacts and (l) Si₃N₄ deposition by PECVD as passivation.

intermediate oxide layer, a drain electrode to contact the pillar top, and insulating layers to separate the source (silicon bulk) from the gate electrode and the gate electrode from the drain electrode. Accurate control of the thickness of the inter-metal layers is extremely important and challenging due to the small dimensions of the pillars.

Hydrogen silsesquioxane (HSQ) is chosen to create the thin insulating layers because it presents excellent gap-filling and local planarization capabilities in comparison with SiO₂ or Si₃N₄ [27]. HSQ is widely used as a negative-tone resist for electron beam lithography (EBL) [28]. Alternatively, it can be converted into a SiO_x-like material by thermal activation: through the scission of Si–H bonds, the formation of new Si–O chains is promoted [29]. In terms of dielectric characteristics, relative permeability (κ) values in the range of 2.8–5.1 have been reported [30]. The topography that arises due to the NPs precludes a good planarization; consequently, a method based on first producing a thicker HSQ layer and afterwards etching it back by means of diluted hydrofluoric acid (HF) is used [31, 32]. The final HSQ thickness accuracy is determined by the precision of the etch-rate.

Figure 2 presents the complete process sequence for SET integration. The first step is the deposition of a thick HSQ layer by spin coating, covering the pillar (figure 2(b)). Then, the HSQ is etched-back by immersion in 0.025% diluted HF down to half the pillar height (figure 2(c)). The slow etch-rate allows to accurately control the proper final thickness. Afterwards, an annealing at 800 °C converts HSQ into a SiO_x-like inter-metal layer (figure 2(d)). It has not been observed any significant etching of the plasma oxide as a consequence of the HSQ back-etching. The main reason is that the etch rate for plasma SiO₂ is lower than for SiO_x-like layer generated from HSQ, but also to the fact that, as it is observed in the drawings of figure 2, the HSQ layers wets the sides of the pillar.

Titanium nitride (TiN) is used as gate electrode material because of its electrical conductivity, well-established thin film deposition technology and CMOS compatibility [33]. A 10 nm thick TiN layer is deposited by radio frequency

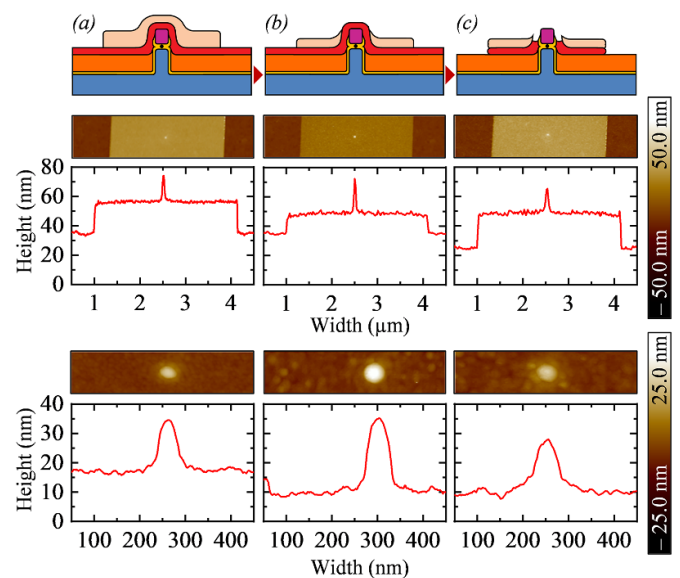


Figure 3. AFM profiles of the same pillar in the three steps of the gate definition sequence: (a) after HSQ exposure of a 20–22 nm thick mask, (b) after etch-back of the mask down to 10–12 nm and (c) after TiN wet etching.

(RF)-sputtering, resulting in a conformal covering of the pillar (figure 2(e)) [34].

The process sequence to remove the TiN from the pillar and to define the gate electrode is presented in figure 3. First, a 20–22 nm mask is defined by EBL using HSQ as a negative resist (figure 3(a)). Afterwards, this layer is etched-back down to 10–12 nm, leaving uncovered the upper part of the pillar (figure 3(b)). At this point, an ammonia-peroxide mixture wet etching is performed at room temperature, in order to remove the TiN from the unprotected areas (figure 3(c)) [35]. AFM characterization at each step of the process reveals a topography that is in agreement with the expected thickness reduction.

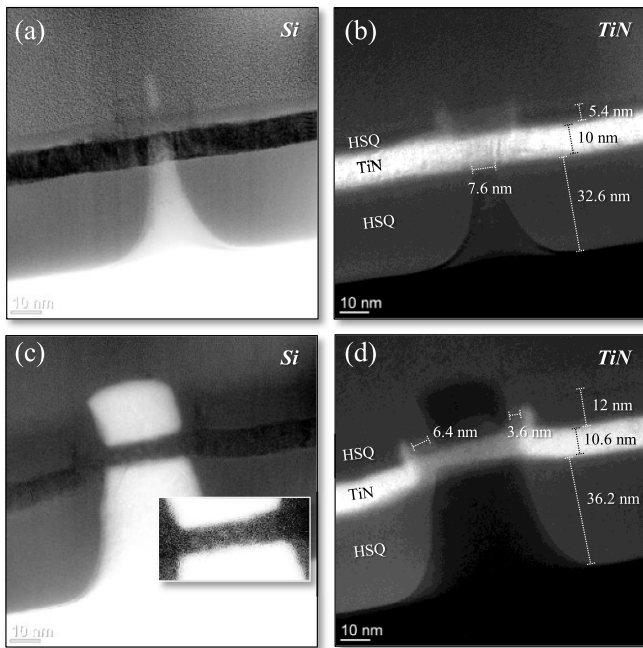


Figure 4. (a), (c) Si and (b), (d) TiN plasmon-loss-filtered EFTEM images of (top row) one example of smallest NP and (bottom row) a wider NP after gate definition and second inter-metal layer annealing at 400 °C. Inset of the embedded Si NDs in (c).

Before the realization of the pillar top contact, a second HSQ layer is deposited (figure 2(i)), followed by an etch-back process. The subsequent HSQ annealing is performed at 400 °C in order to avoid degradation of the TiN layer [36]. The level of leakage current for the two SiO_x -like layers generated from HSQ was tested; the results shows that the parasitic current is lower than the current through the pillar under the expected polarization conditions for SET operation [37].

Figure 4 shows EFTEM images of sub-10 nm (a) and sub-30 nm (b) diameter pillars at this point of the process. In both cases, the inter-metal layers are in the range of optimal thickness values: 32–36 nm for the first one, locating the gate electrode at the same height than the embedded oxide layer; and 5–12 nm for the second layer, enabling the contact to the pillar cap once the drain electrode is fabricated. The TiN material is completely removed from the pillar top, and the electrode surrounds the pillar defining the gate-all-around configuration of the SET. The material chosen as a drain electrode is nickel (Ni) in order to obtain a good ohmic contact with the n-type silicon NPs [38–40].

After the lithography step, a 0.025% diluted HF etching step is performed to remove the native oxide on the pillar top (figure 2(j)), followed by Ni deposition and lift-off (figure 2(k)). The gold (Au) metallization on top of the Ni layer is performed in order to prevent the oxidation of the surface, as the back-end-of-line processing was performed in a non-CMOS line.

Afterwards, a 25 nm silicon nitride (Si_3N_4) is deposited by plasma-enhanced chemical vapor deposition (PECVD) (figure 2(l)). As shown by the EFTEM images presented in figure 5, both gate and drain are properly defined: TiN is

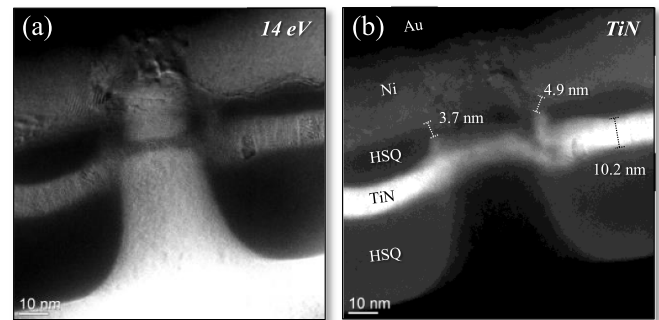


Figure 5. 14 eV (a) and TiN (b) plasmon-loss-filtered EFTEM images of one NP after Ni/Au lift-off for drain electrode definition.

effectively removed from top of the pillar, and a good Ni-NP contact is observed. In addition, both insulating layers are thick enough (3.7–4.9 nm) to separate the TiN electrode (gate) and Ni layer (drain) around the pillar.

Two main issues make very challenging to get an optimal SET performance. The first one is the limited available distance to place both gate and drain electrodes. Note that the separation between the bottom of the embedded oxide and the top of the pillar cap is barely 30 nm. Within this space, the 10 nm thick TiN gate electrode, the Ni drain electrode (which covers not only the top of the pillar, but also some part of the pillar sidewall in order to ensure a proper electrical contact), and the insulating inter-metal layer must be placed. Figure 5 shows that the proper structure can be obtained.

The second issue is related to the gate voltage needed to change the electron energy levels in the Si ND: the separation between the gate electrode and the Si ND is determined by the position of the ND in the embedded oxide and on the remaining insulator on the sides of the NP. The separation can be larger than expected (due to a larger pillar diameter or a thicker remaining insulator in the pillar sidewalls). Then, a high gate voltage needs to be applied, up to the point of inducing the electrical breakdown of the insulating layers that prevents the observation of Coulomb blockade or quantization effects.

3. CMOS compatibility

3.1. Compatibility requirements

The SET-FET circuit is based on the FET amplification of the SET drain current. Figure 6(a) shows a not-to-scale cross-sectional drawing of the contacted SET-FET, and figure 6(b) the corresponding electrical circuit. Figures 6(c) and (d) are 3D drawings of the SET and FET devices, respectively. The pads and contacting lines are made of aluminum.

The following requirements must be considered for a compatible integration:

- (a) To significantly amplify the SET current the FET should operate at sub-threshold level. So, a FET with low threshold value (200–300 mV) is needed.

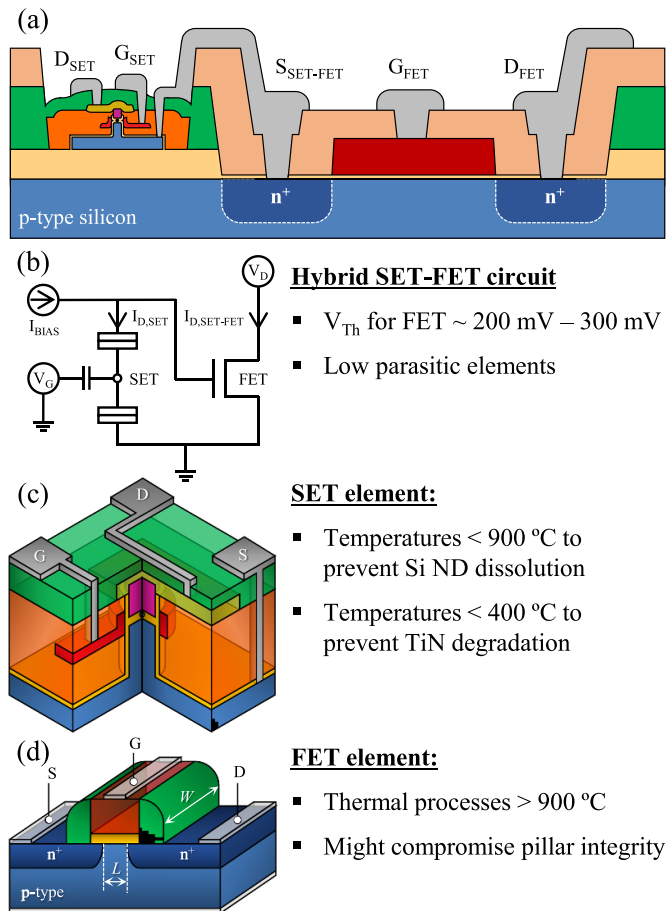


Figure 6. (a) Sketch of the hybrid SET-FET circuit, with details of the main requirements in terms of (b) circuit and each of its integrating elements: (c) vertical SET and (d) planar FET.

- (b) The thermal budget after Si NDs formation is restricted below 900 °C, as a higher temperature process might result in NDs dissolution and consequent SET inoperability.
- (c) After TiN deposition, temperatures over 400 °C must be avoided in order to prevent degradation effects on the gate electrode [36].
- (d) The Ni/Au bilayer used for drain electrode does not endure high temperature processing, and thus the SET contacting must be performed after FET fabrication.
- (e) FET-related fabrication processes may induce a mechanical stress on the pillar structures if a specific protection is not applied.

3.2. Process sequence

The overall fabrication process is based on the prior activity of combining standard CMOS circuits with nanodevices [41, 42], which has been adapted to meet compatibility requirements. The substrates are silicon on insulator (SOI) wafers, where the NPs are defined in the top-Si layer, while the FETs are fabricated in the bulk silicon. This has the advantage of facilitating the isolation between devices.

Figure 7 shows the complete process flow for the hybrid SET-FET circuit, starting from patterned NPs with embedded

Si NDs defined in the SOI layer. In-house FET manufacturing is limited to a 100 mm wafer size, whereas pillars are fabricated on 200 mm wafers. Therefore, a reshaping of the wafer must be performed. Once the pillars have been fabricated, the wafers are shaped to 100 mm diameter size and then the FET processing is carried out.

An additional concern is pillar protection during FET fabrication. The requirements for such protection include: well-known processes for deposition and etching; a safe unprotecting procedure to preserve pillar integrity; and an insulating chemical barrier action. The selected protection is a 300 nm thick Si_3N_4 layer deposited by PECVD, which is removed by immersion in phosphoric acid (H_3PO_4) [43]. Tests of the Si_3N_4 protection and removal with an intermediate annealing step have been performed to confirm that the pillars remain intact, as verified by HR-TEM characterization.

Therefore, before FET processing, the pillars are covered with a 300 nm Si_3N_4 layer (figure 7(b)). Then, this layer and the buried oxide (BOX) are locally etched (figure 7(c)) to define the active area of the FET, and the first part of the FET is fabricated: formation of a 36.5 nm thick gate oxide layer (figure 7(d)); deposition of 480 nm thick polysilicon, doping and patterning (figure 7(e)); source/drain regions definition and implantation (figure 7(f)); and deposition of a 1.3 μm tetraethyl orthosilicate (TEOS) layer as pre-metal dielectric (figure 7(g)), followed by fluidification at 850 °C for dopant activation.

Figure 8 presents a photograph of the wafer and optical images with details of the FETs fabricated near the top silicon islands where the patterned NPs are located.

At this point, pillars are deprotected by removing the Si_3N_4 in H_3PO_4 (figure 7(h)). Plasma oxidation for pillar shrinkage and SET gate oxide formation is then performed as detailed in [26] (figure 7(i)), followed by the complete SET integration as described in section 2 (figure 7(j)). The remaining steps involve contact windows etching (figure 7(k)) and metal routing (figure 7(l)) for SET-FET interconnection.

Figure 9 shows optical images of the fabrication after metal routing: for each chip, 16 FETs are fabricated near a set of 16 top-silicon islands with previously defined pillars.

3.3. Structural validation

Although AFM and SEM inspections were performed during the FET fabrication as part of the process monitoring, the ultimate validation of the pillar and Si ND integrity is performed by EFTEM analysis at the end of the complete fabrication process.

Figure 10 presents EFTEM cross-sectional micrographs of pillars of sub-30 nm and sub-50 nm diameters. The complete process sequence has been performed: wafer-reshaping, protection during the FET fabrication, optimized thermal processes, pillar unprotecting and plasma oxidation. As it can be observed, both pillars present excellent aspect, with no residues of resist or Si_3N_4 around. Furthermore, Si NDs are visible in the embedded SiO_2 layer, and a thin 4–5 nm SiO_2 layer covers the pillar completely. This result validates the

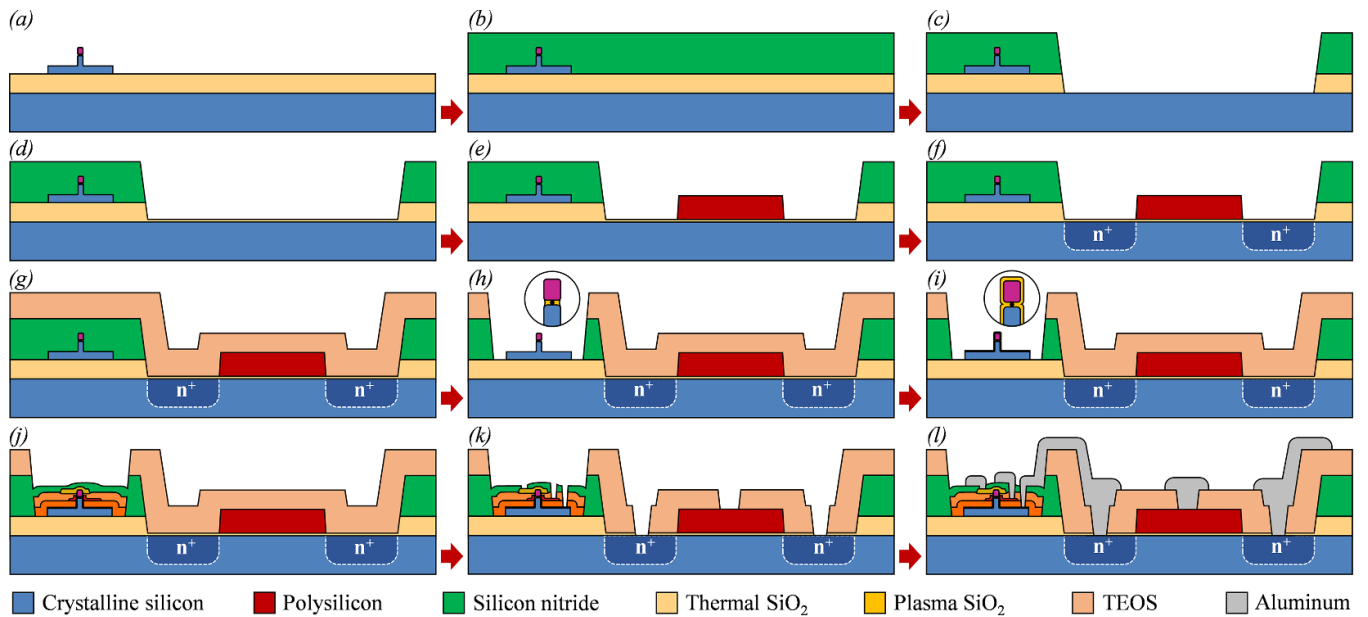


Figure 7. Sequence steps of the SET-FET integration process flow: (a) initial pillar SOI configuration; (b) 300 nm Si_3N_4 deposition by PECVD as pillar protection; (c) Si_3N_4 and BOX dry etching; (d) gate oxidation of a 36.5 nm layer; (e) 480 nm polysilicon deposition, doping and patterning; (f) phosphorus implantation in S/D regions; (g) 1.3 μm TEOS deposition as pre-metal dielectric; (h) TEOS dry etching and Si_3N_4 wet etching in H_3PO_4 ; (i) plasma oxidation for pillar size shrinkage; (j) SET integration process; (k) contact windows etching; (l) and metal routing definition for SET-FET interconnection.

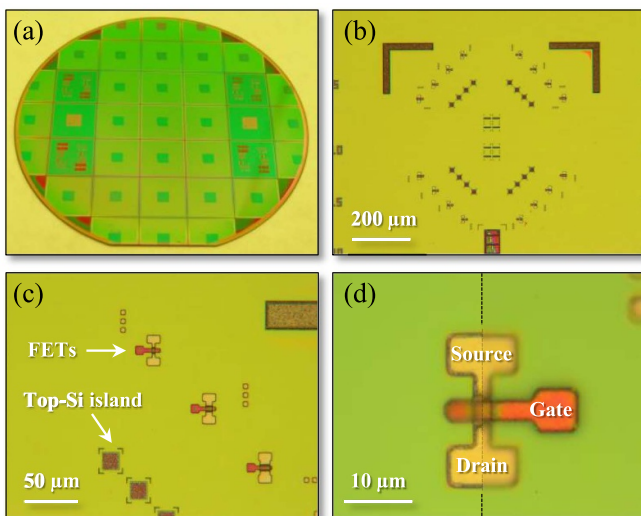


Figure 8. (a) Optical image of one of the processed wafers, with detail of (b) one example of device layout, (c) an inner region with the FETs fabricated near the top-Si islands with the patterned NPs and (d) optical images focused on the active areas (left) and the polysilicon gate (right) of the smallest FETs, with dimensions W (width) $\times L$ (length) of $3 \mu\text{m} \times 3 \mu\text{m}$.

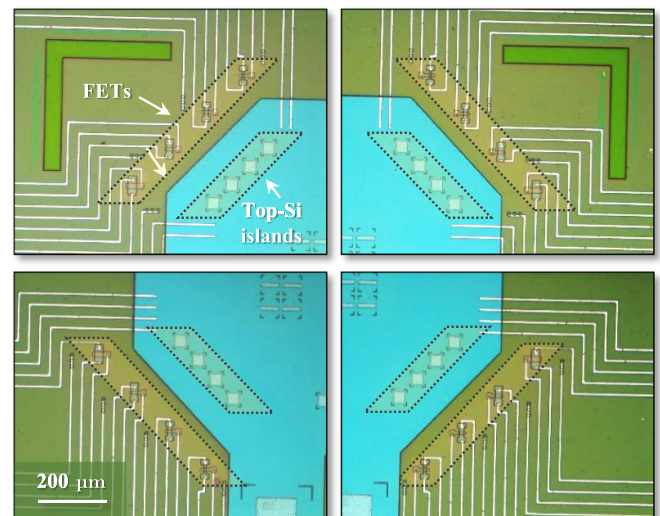


Figure 9. Optical images of one example of device after contact windows etching and metal routing definition, completing the FET fabrication.

CMOS compatibility with vertical nanostructured devices in terms of structural integrity.

3.4. Electrical measurements and simulations

After the fabrication of the FETs, their electrical characterization is performed to extract electrical parameters such as threshold voltage (V_{Th}) and subthreshold slope (SS).

The resulting parameters are used in the electrical simulation of the hybrid SET-FET circuit.

3.4.1. FET characterization. The nominal transistor width and length ($W \times L$) are $3 \mu\text{m} \times 3 \mu\text{m}$, $6 \mu\text{m} \times 3 \mu\text{m}$, $9 \mu\text{m} \times 3 \mu\text{m}$ and $12 \mu\text{m} \times 6 \mu\text{m}$, for the transistors named T1 to T4 in figure 11.

The current–voltage characteristics of the FETs are presented in figures 11(a) and (b). The main parameter affecting the operation of the SET-FET hybrid circuit is V_{Th} . $I_{\text{D}}-V_{\text{GS}}$

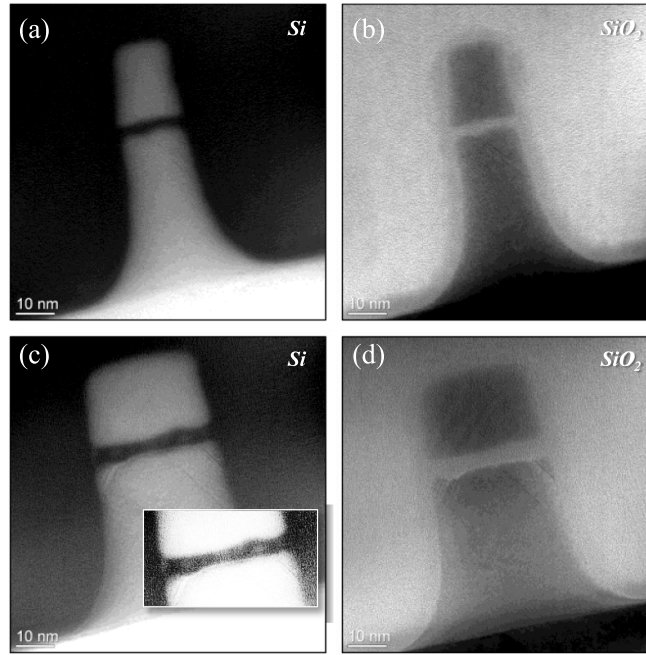


Figure 10. (a), (c) Si and (b), (d) SiO₂ plasmon-loss-filtered EFTEM images of (top row) one example of the narrowest nanopillar and (bottom row) one of the widest one, after performing the complete process sequence: wafer reshaping, protection during FET fabrication, FET fabrication at pre-optimized conditions, pillar unprotecting and plasma oxidation. Inset of the embedded Si NDs in (c).

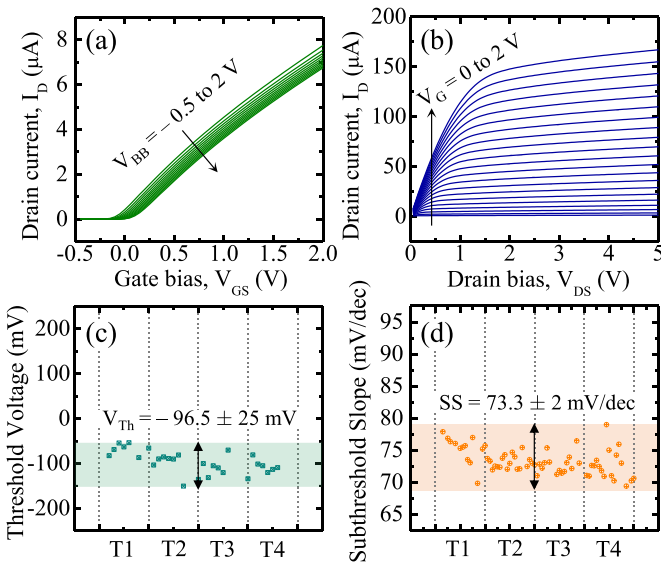


Figure 11. (a) I_D - V_{GS} characteristics of one example of T1 FET by sweeping the body bias V_{BB} from -0.5 V to $+2$ V with at $V_D = 50$ mV, and (b) I_D - V_{DS} characteristics for gate bias from 0 V to 2 V. (c) Threshold voltage V_{Th} and (d) subthreshold slope SS for all measured FETs, classified by device dimensions.

curves reveal a shift of V_{Th} towards negative bias, which can be compensated by applying a bias to the bulk (V_{BB}) (figure 11(a)). The negative values for V_{Th} are obtained because of the dopant concentration of the substrate wafer and the missing implantation for V_{Th} adjustment during the

FET process. The implantation step has been skipped to avoid damaging the pillars and modifying the silicon NDs embedded in the pillars.

In the linear regime ($V_{DS} = 50$ mV), an average V_{Th} of -96.5 ± 25 mV (figure 11(c)) and an average SS value of 73.3 ± 2 mV dec⁻¹ (figure 11(d)) have been obtained. The SS value can be compared with the theoretical one according to substrate doping and oxide charges.

In the subthreshold region, the exponential behavior of the I_D - V_{GS} characteristic curve is described as follows:

$$I_D \propto \exp \frac{V_{GS}}{(n\phi_t)}$$

Therefore, the slope is determined by $n\phi_t$, where ϕ_t is the thermal voltage, and n is a factor that depends on the dopant concentration, oxide capacitance and Fermi potential:

$$n = 1 + \frac{1}{2C_{ox}} \sqrt{\frac{2qN_A\epsilon_{Si}}{1.5\phi_F}}$$

Dopant concentration is nominally 1×10^{15} at-cm⁻³ for the processed wafer; the Fermi potential ϕ_F at room temperature for the same concentration is 0.289 V, and C_{ox} is calculated:

$$C_{ox} = \epsilon_{ox} \frac{A}{t_{ox}}$$

The resulting theoretical value for the subthreshold slope is 69 mV dec⁻¹, which is very close to the measured value of 73 mV dec⁻¹.

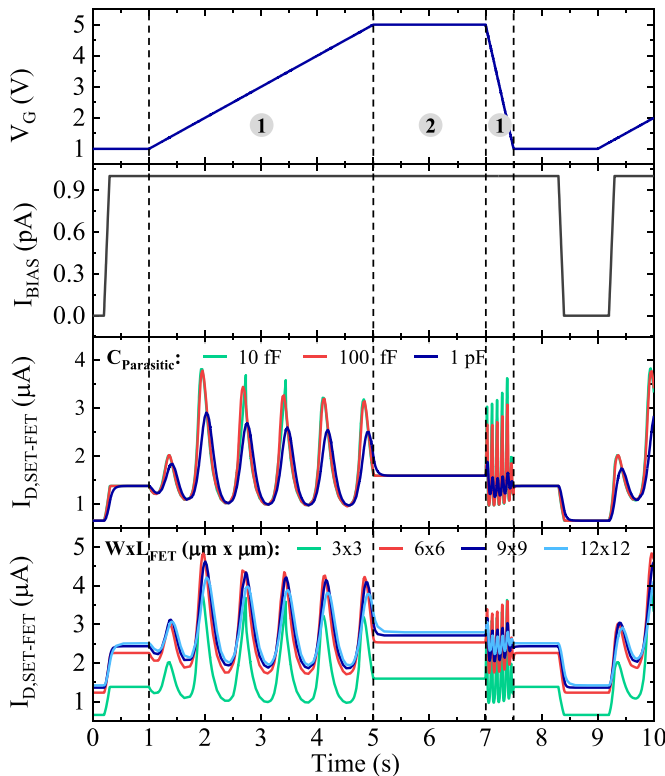


Figure 12. Simulations for different values of parasitic capacitances and resistances at different regimes and conditions in the hybrid SET-FET circuit.

3.4.2. Simulation of the hybrid SET-FET circuit with experimental parameters. In order to simulate the hybrid SET-FET circuit, a dedicated model for the vertical SET topology has been used [44]. For the FET element, a HSPICE device model of the in-house CMOS technology is used, modified according to the results of the FET characterization presented previously.

According to the simulations performed and summarized in figure 12, Coulomb blockade oscillations can be easily observed by varying the gate voltage. The effect of the parasitic capacitance introduced by the interconnections between the SET drain and the FET gate has been analyzed. It is concluded that the hybrid SET-FET circuit still works properly for parasitic capacitances up to 1 pF. Moreover, the simulations show a good amplification of the SET signal, achieving a FET drain variation of 4 μA .

4. Conclusions

The integration of vertical NPs containing self-assembled Si NDs with planar FETs has been demonstrated, as an example of compatible CMOS technology with SET fabrication.

Several innovative process approaches have been developed. For example, the use of HSQ along with an etch-back mechanism to form an inter-metal layer, providing good planarization and accurate thickness control, and its use as ultralow-thickness negative masks to pattern the TiN gate electrode at the same time that TiN is removed from the pillar cap.

Standard CMOS technology has been adapted in order to preserve the NPs and NDs integrity during FET fabrication and SET integration. Thermal processes have been modified to remain below the restricted thermal budget. An effective mechanism to protect the NPs/NDs during FET fabrication has been tested and validated. The integrity of the pillars after FET fabrication was confirmed by TEM structural analysis. Characterization of both gate and drain electrodes in contact with the pillar indicates proper contact formation.

The fabricated FETs demonstrate a low threshold voltage and good subthreshold swing performance, with values in the theoretically expected range; both characteristics are in line with the requirements imposed by the hybrid SET-FET circuit. Moreover, simulations indicate that the FET performance is adequate for the operation of the hybrid SET-FET circuit.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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