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Improved electronic properties of p- epitaxial layers grown on HPHT (100) substrates after a surface pretreatment

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Single-crystal diamond synthesis of high crystalline quality remains a challenge for power electronic devices[1]. Usually, HPHT diamond substrates will undergo a mechanical polishing step which induces plastic deformation and dislocations in the subsurface at few microns depth[2]. During Chemical Vapour Deposition (CVD) growth, these dislocations might thread into the epilayers[3] and emerge as pyramidal hillocks[4] affecting the devices electronic performance[5]. Consequently, removing this defective layer and reaching very smooth substrate surface before growth[6] is primordial to better control the crystalline quality of diamond epitaxial layers.

In this work, we investigated the effect of Ar/O_2 etching on HPHT (100) Ib Sumitomo substrates by optimizing the RF-power, the pressure and the O_2 content in regard to the etching rate and RMS roughness. This surface pretreatment provides fast etching rates up to 9 µm/h and results in smooth surfaces according to AFM measurements (RMS roughness from 3.5 to 2 nm on 40x40 μm^2 images).

Ar/O_2 etching with optimal conditions was used to lead a comparative study on two half-etched HPHT (100) substrates of different suppliers (Sumitomo Ib and New Diamond Technology IIa). Pretreatment efficiency was tested on both of them by evaluating the enhancement of crystalline quality using Raman Spectroscopy and High Resolution X-ray Diffraction.

The crystalline quality of low boron doped (10^{16} cm^{-3}) epilayers (2 µm thick) grown simultaneously on the two etched substrates was studied by Raman and Cathodoluminescence and compared with non-treated substrates. SEM voltage contrast is used to highlight the threading dislocations on non-pretreated areas and their removal after etching (Figure 1). Electronic properties were also investigated by Hall measurements and show a clear improvement in term of carrier mobility and resistivity (from 3 to 1.7 Ω.m) on pre-etched area of Ib Sumitomo substrates.

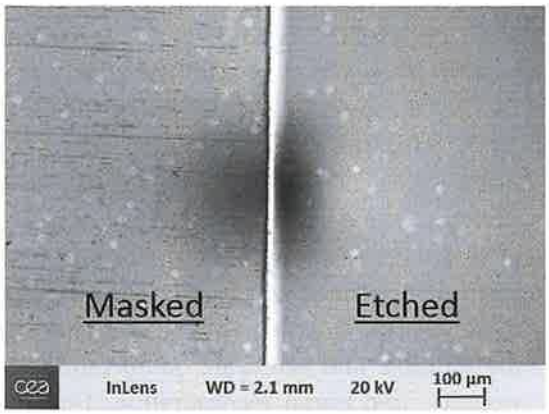

Figure 1: SEM image of half-etched Sumitomo substrate at 20 kV

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