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Crossbar Arrays based on "Wall" Phase-Change Memory (PCM) and Ovonic-Threshold Switching (OTS) Selector: a Device Integration Challenge Towards New Computing Paradigms in Embedded Applications

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Abstract

In this work, we demonstrate the integration feasibility of Crossbar arrays based on Ovonic-Threshold Switching (OTS) selector and "Wall"-based Phase-Change Memory, realized with a "Double-Patterned Self-Aligned" (DPSA) structure in the Back-End-of-Line (BEOL) of the CMOS fabrication. We fabricated devices with critical dimensions down to 60 nm×80 nm, integrating materials providing improved thermal stability (against BEOL thermal budget). Preliminary statistical electrical tests performed in 1 kb 1T1S1R arrays confirm the devices correct programming and cycling operations. These results pave the way to the integration of Crossbar arrays in embedded applications.

(Keywords: Crossbar, "Wall" PCM, OTS selector)

Introduction

Phase-Change Memory (PCM) and Ovonic-Threshold Switching (OTS) selector have been successfully co-integrated in 3D stacked Crossbar arrays definitely reaching a high maturity, until the mass production of devices targeting stand-alone Storage Class Memory applications [1]. In order to enable neuromorphic computing architecture design, for example to speed up matrix-vector multiplication operations [2], Crossbar Resistive Memory is considered a valuable solution to be implemented in future embedded architectures, in order to support recognition and prediction tasks required in autonomous systems (e.g. driving).

In this work, we demonstrate the co-integration of a PCM resistive device (1R) based on "self-aligned" (SA) Wall structure [3] with an OTS selector device (1S) by adding a "Cross" patterning (i.e. "Double-Patterned Self-Aligned" or DPSA integration) perpendicular to the first SA one. We address the issues inherent to our DPSA integration and in particular related to the bitline realization, which should reliably recover the contact over the 1S1R devices, and to the lithography strict alignment to allow device scaling down to tens of nm.

We show a good control of the effects of etching/stripping chemistry on the integrated materials by TEM/EDX analyses and finally we provide electrical results demonstrating successful programming operations in devices with a surface size down to 60 nm×80 nm.

Results and Discussions

A. PCM and OTS alloys

Our 1S1R DPSA structure is schematically represented in **Fig. 1a**. The PCM layer is integrated over a heater element (H), and it is followed by the OTS layer based on a GeSbSeN alloy [4], [5] (**Fig. 1b**). The intermixing between the two layers is hindered by an intermediate TiN electrode. We fabricated 1S1R devices integrating two different GeSbTe PCM alloys A and B, respectively with low and high Ge content. They were coupled with two OTS thicknesses (i.e. t1 and t2 with t1 < t2), leading to a total of four different PCM-OTS stacks.

B. DPSA 1S1R cell fabrication

We fabricated our 1S1R devices and arrays in the BEOL of LETI Memory Advanced Demonstrator based on 130 nm CMOS technology. **Fig. 2** summaries the key steps of the DPSA process integration described by Coventor SEMulator3D® modeling platform. A first Wall (W) SA patterning (x direction) of the PCM-OTS stack involving also the heater definition is followed by a Cross (C) perpendicular patterning (y direction). The recovery of the contact on the top electrode after Wall patterning represents the first challenge in such integration. We compared two approaches: "Dry Etch-back" (**Fig. 3a**) and "Full CMP" (**Fig. 3b**) (i.e. chemical-mechanical polishing). The first one demonstrated (in SEM analyses) a high dependency on the devices pitch, with a consequent high variability. The second one, based on the selectivity of SiO_2 polishing wrt a SiN layer used as stop layer demonstrated a good reproducibility. In order to obtain fast prototyping of scaled devices in x and y directions (targeting devices down to 50 nm), we took advantage

[1] Vistec Electron Beam GmbH, D-07743 Jena, Germany.

of Variable Shape Beam VISTEC® SB3054 lithography tool allowing alignments control thanks to modelling and die-to-die correction. Being the C/H alignment crucial for the device functionality (i.e. to obtain an active region perfectly centered into the PCM layer), we designed dedicated structures with a large Wall size and for different Cross sizes, connecting many devices in parallel for the electrical evaluation of the C/H alignment at end of fabrication. **Fig. 4a** shows the results obtained on a wafer integrating only a PCM layer (w/o OTS). The resistance increases with the decrease of the Cross size, likely related to a gradual loss of reliability on the C/H alignment. The inset reports the typical overlay (OV) obtained in a whole lot for both W/H and C/W alignments with a *mean OV+3*σ < 30 nm for both. This is affecting the alignment for a Cross size below 60 nm (a solution for a direct C/H alignment is under validation). On the contrary, we observe the expected almost linear relation between the devices virgin resistance (R_V) and the reciprocal of the Wall size (**Fig. 4b**). TEM analyses performed on a 60×60 device (i.e. Wall×Cross sizes are expressed in nm) integrating the PCM-OTS stack (**Fig. 5a**) highlight that alignment control is mandatory to target small sizes functionality. Indeed, we observe that H is not perfectly aligned with C in the device observed. EDX profiles (**Fig. 5b**) evidence a uniform distribution of the elements perpendicularly to the OTS/SiN interface. Indeed, chalcogenide materials are sensitive to halogens [6], then a step-by-step etching strategy with dedicated chemistry recipes for each step was applied during the Wall etching (i.e. starting from the top electrode: *TiN / OTS / TiN / PCM / heater*) and Cross etching (i.e. *TiN / OTS / TiN / PCM*) to prevent from OTS and PCM layers damage.

C. DPSA 1S1R electrical characterization

The firing operation (i.e. initialization step) was investigated in the four PCM-OTS stacks, showing a decreasing of the firing voltage (V_{FIRING}) when reducing the OTS thickness from t2 to t1, and when reducing the Ge content in the PCM alloy from B to A (**Fig. 6a**). As expected, V_{FIRING} does not depend on the size of the device (i.e. electric-field-dominated phenomenon) [7], as shown in the results that are equivalent for 60×60 and 300×300 devices. Device functionality was statistically verified in 1 kb arrays of transistor-selected 1S1R devices (1T1S1R). As an example, in **Fig. 6b** we report the array map of the current after the devices activation, meaning the dynamic current measured during the pulse application. Only four devices are not switching (< 0.4%). Threshold Voltage (V_{th}) versus programming current plots of **Fig. 7** show the typical SET-RESET characteristics for 1S1R devices. We compared the behavior of 60×80 and 300×300 cells, both showing a reading window of about 1.5 V, compatibly with the V_{th} of Ge-rich GeSbTe devices [8] (i.e. the 1S1R max voltage reading window is equal to the PCM V_{th} [9]), with well distinguishable SET and RESET programming current regions. Current reduction in 60×80 cells is in line with the reduced heater surface wrt 300×300. SET/RESET programming operations were performed in 1T1S1R 1 kb arrays based on 60×80 devices along 100 cycles, and the statistics of the obtained V_{th} distributions are reported in **Fig. 8**. We show almost no overlapping among SET and RESET distributions, without the use of smart programming or Program&Verify protocol.

Conclusions

A "Double-Patterned Self-Aligned" PCM-OTS structure was presented, targeting the co-integration of PCM "Wall" structure with OTS in the BEOL of the integration. The optimization of the fabrication process was discussed, presenting some of the implemented solutions. 1S1R devices, with dimensions down to 60 nm×80 nm, were realized and tested at statistical level in 1 kb 1T1S1R arrays. A reliable reading window of 1.5 V obtained with almost no SET/RESET distributions overlapping along 100 cycles.

Acknowledgments

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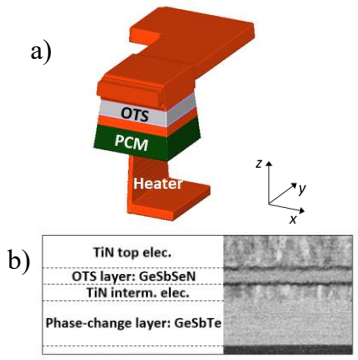

Fig. 1: a) DPSA PCM-OTS device description. b) Bright Field TEM image of the integrated stack.

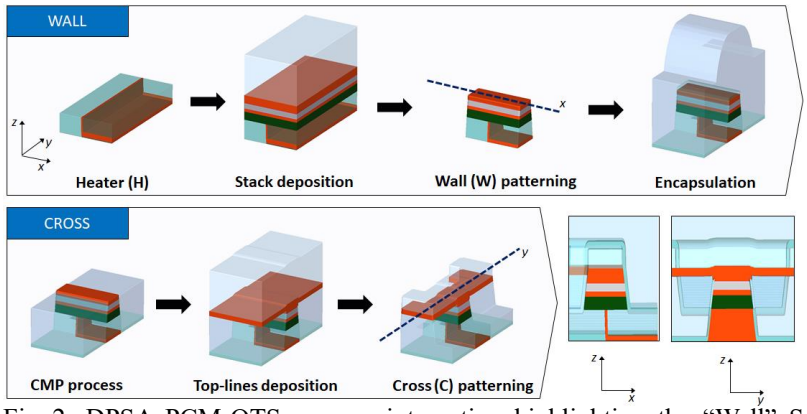

Fig. 2: DPSA PCM-OTS process integration highlighting the "Wall" SA patterning (top) and the following "Cross" patterning (bottom).

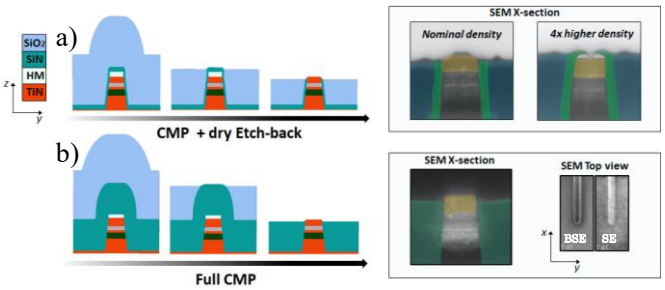

Fig. 3: Contact recovery after "Wall" patterning and encapsulation: a) "Etch-back" approach: strong dependency on the devices density. In the TEM it is compared the nominal (good) density wrt 4x (bad). b) "Full CMP" approach: good uniformity, confirmed by SEM (section + BSE and SE).

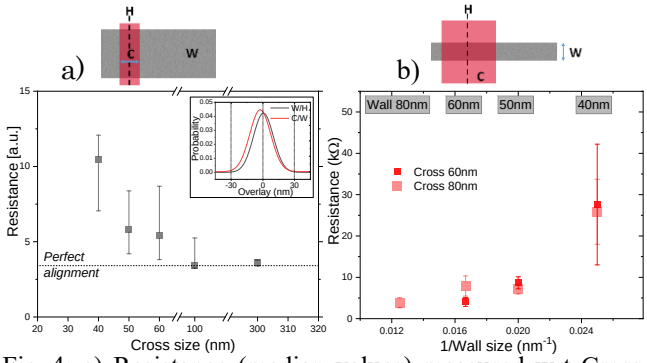

Fig. 4: a) Resistance (median values) measured wrt Cross size on dedicated test structures (PCM layer w/o OTS i.e. 1R devices) for alignment control. b) Evolution of mean R_V vs reciprocal of Wall size in 1R devices. The smallest Wall size of 40 nm shows a higher variability.

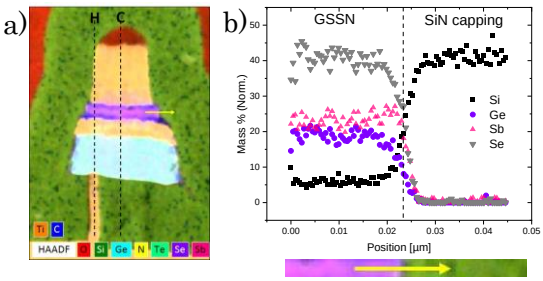

Fig. 5: a) HAADF TEM-EDX of a 60×60 device (zx plane) highlighting C/H misalignment issue. b) EDX profile performed at the OTS/SiN capping interface.

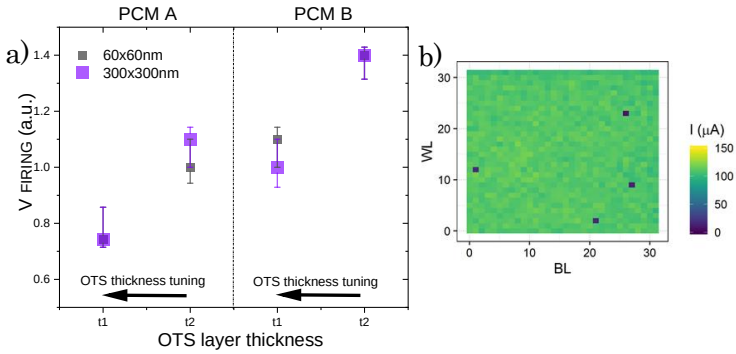

Fig. 6: a) V_{FIRING} (median values) for the different OTS thicknesses (t1 and t2) and PCM alloys (A and B). b) Reliable firing operation at 5 V in 1 kb array of 1T1S1R 50×60 devices (based on PCM alloy A and OTS thickness = t1).

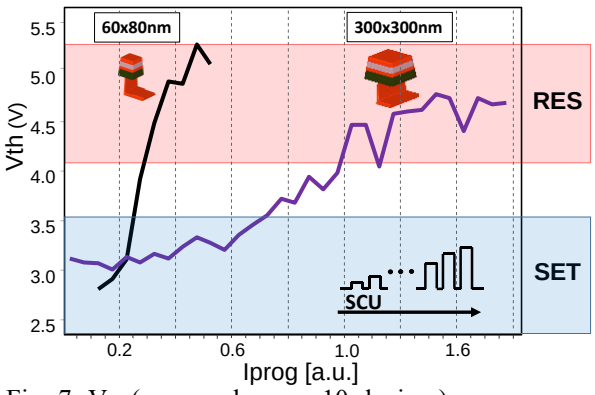

Fig. 7: V_{th} (mean values on 10 devices) vs programming current (I_{PROG}) characteristics for 300×300 and 60×80 1S1R devices (based on PCM alloy A and OTS thickness = t1).

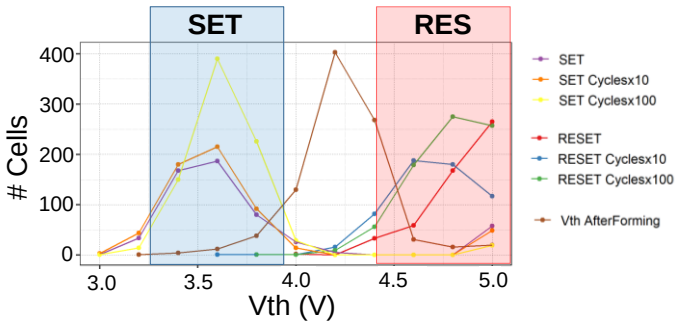

Fig. 8: SET/RESET programming in 1T1S1R 1kb arrays based on 60×80 cells. SET and RESET V_{th} distribution are reported at the starting and after 10 and 100 cycles.