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Die-to-die alignment for lithographic processing of reconstructed wafers

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Abstract— In this work, we address one of the challenges of Fan-Out Wafer Level Packaging (FO-WLP), which is chip placement error, which occurs during the process of wafer reconstruction and molding. In a typical FO-WLP process, a wafer processed on a front-end tool is diced, and the dies are repositioned on a carrier with additional space created for fan-out structures. A dedicated alignment approach, which includes measurement of individual dies to adjust the settings per exposure, would result in a dramatic improvement of the overlay performance. This process further referred to as die-to-die alignment is generally known to have negative impact on throughput for IC manufacturers.

The accuracy of die-to-die alignment on 200 mm wafers is evaluated experimentally in collaboration between Kulicke & Soffa and CEA LETI. The wafer layout consists of dies of different sizes (120 chips of 4 mm x 4 mm and 70 of 10 mm x 10 mm) for which intentional misalignments have been introduced with different amounts of translation (up to +/-50 micrometers) and rotation (up to +/-10 milliradians) in order to emulate typical errors found in reconstructed wafers.

Alignment of the “back-end” layer with respect to existing patterns on the wafer was measured both at Kulicke & Soffa and at CEA LETI. Both measurements confirmed sub-micrometer accuracy of overlay between the structures on the reference wafer and the new layer exposed on LITEQ 500. Throughput inline with current industrial standards was achieved. Data analysis shows that major improvements of the throughput can be achieved by optimizing the exposure process.

Keywords: die-to-die, alignment, WLP, Fan-out, RDL, Lithography, LITEQ 500, Overlay

I. INTRODUCTION

Fan-out wafer level packaging (FO-WLP) is one of the key enablers of 2.5D and 3D packaging solutions for such applications as 5G, Antenna in Package (AIP), High Performance Computing, AI, Automotive ADAS, mobile devices and the Internet of Things (IOT) [1-4]. These demanding markets require compact, high performance devices which may require the use of advanced packaging in their IC manufacturing process.

In this work, we address one of the challenges of FO-WLP, which is the chips placement error, which occurs during the process of wafer reconstruction and molding. In a typical FO-



Fig. 1. The LITEQ 500 stepper.

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TABLE I
SPECIFICATIONS OF LITEQ 500

Item	Standard Features	Comments
Imaging	Qualified at 2 μm L/S, DoF > 16 μm	NA 0.13 1x Lens Sub 1.5 μm resolution possible
Illumination	Intensity: > 2000 mW/cm ² Non-uniformity: < 3%	Conventional illumination with $\sigma = 0.55$
Focus Control	Field-by-field, 2 μm repeatability	Z-only, field by field focus leveling
Single Machine Overlay	Accuracy < 500 nm	Bright field pattern recognition
Wafer Handling	2x 300 mm FOUP load ports Wafer thickness range: 0.4 to 2 mm	100 to 300 mm compatible Different substrates types
Reticle Handling	Up to 3 SMIF pods containing 6 reticles each	2-gripper configuration
300 mm Wafer Throughput	> 95 wph for 400 mJ/cm ² > 70 wph for 1000 mJ/cm ²	40 fields, 2 EGA sites
Wafer Edge Exposure Wafer Edge Protection	Adjustable in 1 to 3 mm range. Accuracy ± 0.2 mm (WEE), ± 0.3 mm (WEP)	Automatic recipe-defined, no manual change required for 200 / 300 mm
Multi-pattern Exposures	Enables to image subfields using SW controller reticle masking	Chrome border 2 mm, Configuration option

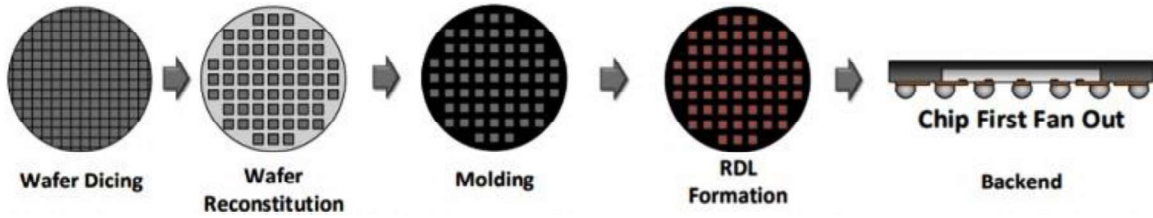


Fig. 2. Chip First Fan Out process flow

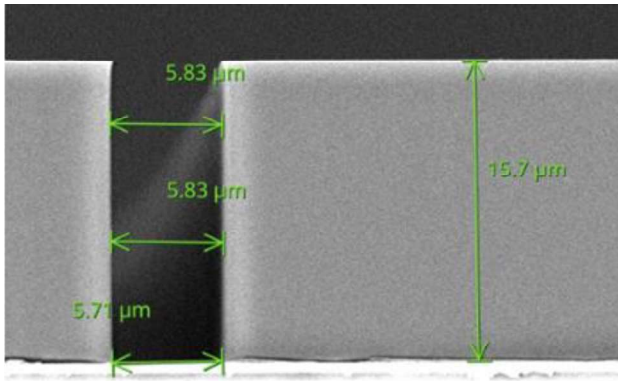


Fig. 3. Cross-section image of CY-1000 photoresist. 5 μm isolated trenches with near-vertical sidewalls on a Ti/Cu/Ti substrate exposed at 100mJ/cm². Resist showed a bias of 0.7-0.8 μm .

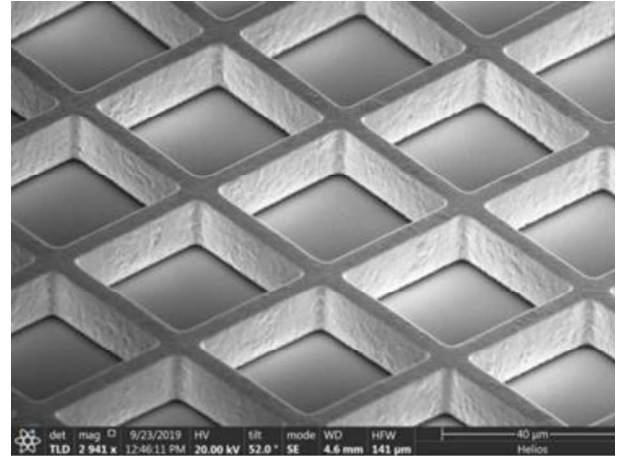


Fig. 4. Same wafer as in Fig. 2 but after copper plating and stripping CY-1000 photoresist.

WLP process, a wafer processed on a front-end tool is diced, and the dies are repositioned on a carrier with additional space created for fan-out structures. Then the wafer is reconstructed by molding, and finally, a redistribution layer is formed on top of the reconstructed wafer using several lithographic steps. Errors occur during die placement and molding, typically resulting into translations up to a few tens of micrometers and rotations up to a few milliradians with respect to the target position.

A common global alignment approach, where only a few features per wafer are measured to adjust the exposure grid,

cannot correct for these errors, thus yielding limited overlay accuracy. A dedicated alignment approach, which includes measurement of individual dies to adjust the settings per exposure, would result in a significant improvement of the overlay performance. This creates an opportunity for implementing fan-out structures with higher interconnection density. This process is further referred to as die-to-die alignment; generally known to have a major impact on throughput for manufacturers. This paper reports on the implementation of die-to-die alignment using the LITEQ 500 lithographic projection stepper from Kulicke & Soffa.

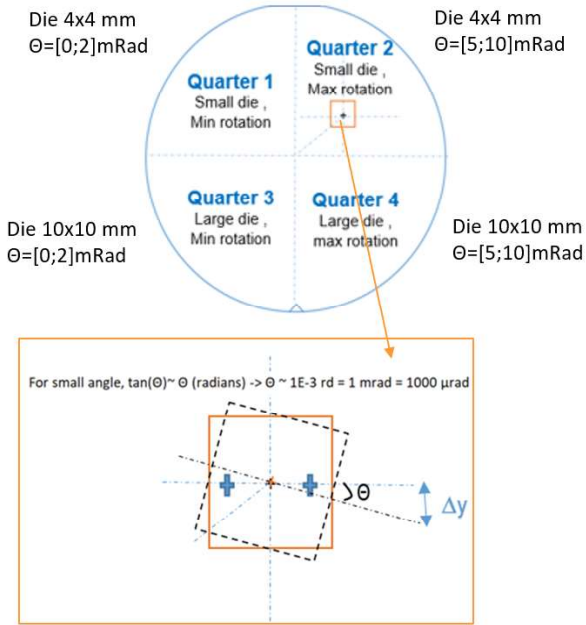


Fig. 5. Layout of the test wafer.

II. EXPERIMENTAL DETAILS

A. Kulicke & Soffa LITEQ 500 project stepper

The lithography system employed in this study was the K&S LITEQ 500 stepper (shown in Fig. 1) that supports wafer sizes from 100 to 300 mm [5]. The 355 nm laser-powered tool is developed specifically for the advanced packaging market; it offers 2 micrometer-resolution over 16 micrometers of usable depth of focus, warped wafer handling, laser-based Wafer Edge exposure and contact-free wafer edge protection. The specifications of this tool are listed in Table I.

On the LITEQ 500, pattern recognition and alignment is done optically by means of a camera. The system offers maximum flexibility as the end user is able to teach many types of patterns that fall within the field of view of the camera. X and Y positions of features on the wafer such as dies, alignment marks, etc. can be collected and reported within a few minutes.

B. Wafer preparation

In order to demonstrate LITEQ 500 capability to perform die-to-die alignment on a broad range of misalignments and die sizes, a suitable test vehicle was designed by LETI FO-WLP and process teams. The idea was to consider continuing the process of a reconstructed wafer with chips embedded in a molding material structure, by an electrical redistribution layer (RDL), as shown in the integration flow in Fig. 2.

In this type of integration, multiple die sizes and misalignment values can be present. To investigate this kind of configuration, LETI provided K&S with wafers to simulate the placement error generated during the wafer reconstitution process.

Starting from 200 mm silicon bulk wafers, a standard i-line lithography with a 1x mask aligner was carried on, followed by a silicon dry etching step to build up the layer 1 pattern, which contains the predefined pattern of offsets required for the overlay evaluation. For cost aspects, instead of functional dies, we created a typical footprint of silicon

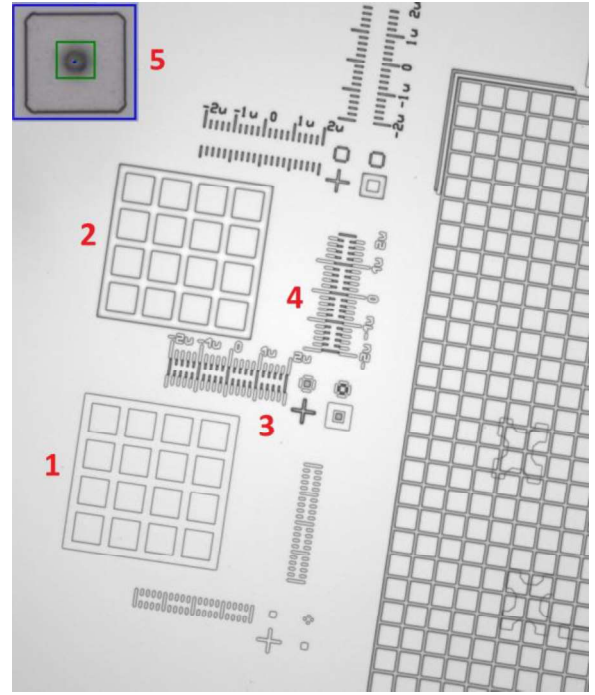


Fig. 6. Image of the etched grid mark 1, exposed grid mark 2, Vernier scales 3 and 4 and overlapping boxes for measuring overlay 5.

chips, which would have been formed following the stress molding process step, in layer 1 of the wafer.

After layer 1 patterning, a Ti/Cu or Ti/Cu/Ti PVD seed layer deposition was done on the wafers, which were then sent to K&S to perform the RDL die-to-die lithography.

At K&S, the LETI wafers were coated with a 15-micron thick layer of TOK CY-1000 chemically amplified photoresist. Fig. 3 shows the cross-section of the resist after development, and Fig. 4 shows copper structures after electroplating, which is the intended application scenario.

The test vehicle mask design consisted of 120 dies of 4 mm x 4 mm size and 70 dies of 10 mm x 10 mm size. Different amounts of translation (up to +/- 50 micrometer) and of rotation (up to +/- 10 milliradians) were applied to the individual dies to emulate typical errors found in reconstructed wafers. The wafer layout is shown in Fig. 5. Small (4 mm x 4 mm) dies are placed in the top half (Quarters 1 and 2), and large (10 mm x 10 mm) dies in the bottom half (Quarters 3 and 4). Rotation range was limited to 2 milliradians for Q1 and Q3, with large (up to 10 milliradians) rotations in Q2 and Q4.

C. Die-to-die exposure approach

In a global alignment strategy, the wafer grid is calculated using a six-parameter fit [6], which consists of x-Translation, y-Translation, Rotation, Non-Orthogonality, x-Magnification and y-Magnification. In contrast, for a single die exposure only four parameters are used for position correction, which are x-translation, y-translation, rotation, and magnification.

In the metrology step, etched global alignment marks coated with a Ti/Cu or Ti/Cu/Ti seed layer are captured using the alignment system of the LITEQ 500. Near these marks, we also visualize two etched halves of the Vernier scales, one half is for the x-direction of the die and the other for the y-direction. Global alignment marks are also present on the

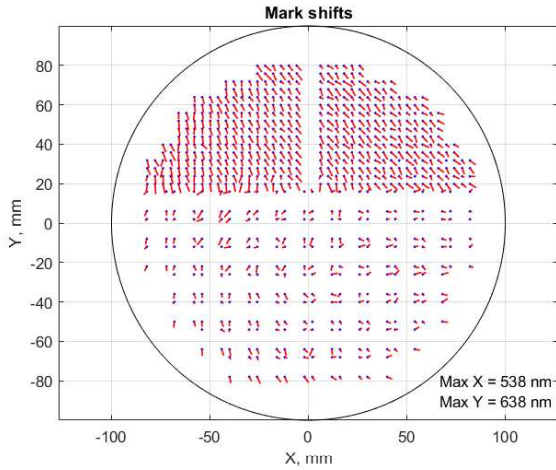


Fig. 7. Measurement data from IVS-200 tool, wafer #5; four alignment marks in corners of each die were measured.

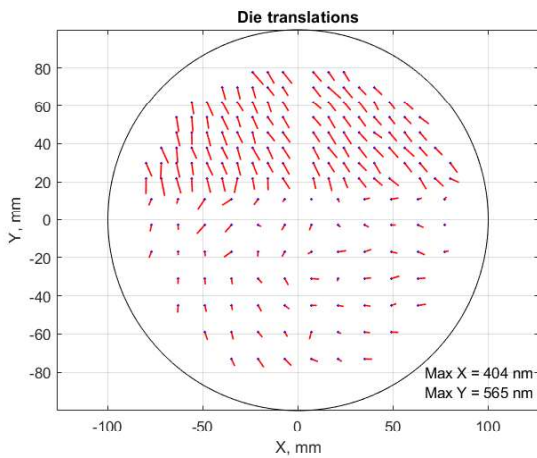


Fig. 8. Die translations obtained by decomposition of the IVS-200 measurement data using model (1), wafer #5.

reticle image, but with a finite offset. The same applies to the second halves of the aforementioned Vernier scales. This means that when the photoresist is developed, both global

alignment marks and two full Vernier scales should become visible (see Fig. 6). The etched grid mark 1 is used for alignment, while features 2 to 4 are used for internal overlay diagnostics, which are performed directly on LITEQ 500 tool. This diagnostic is already part of the tool functionality. The exact measurement procedure on the LITEQ 500 will be the subject of a subsequent publication.

For measurement with a dedicated overlay metrology tool, four $30 \mu\text{m} \times 30 \mu\text{m}$ boxes are placed in corners of each field on the test wafer. Smaller ($6 \mu\text{m} \times 6 \mu\text{m}$) boxes at the corresponding locations are included in the reticle layout. After the photoresist layer is exposed and developed, the relative shift between the large and small box can be measured with an IVS-200 tool at CEA LETI, which is automated for measuring all 760 locations on a wafer. This box-in-box pattern is shown in an insert of Fig. 6 (label 5).

III. DATA ANALYSIS AND DISCUSSION

A. ANALYSIS OF THE OVERLAY PERFORMANCE

Four wafers (numbered from #5 to #8) were processed according to the die-by-die exposure approach described above, with 120 small and 70 large dies exposed on each wafer on top of the existing pattern. Overlay errors (shifts of the box-in-box alignment marks) were measured in four corners of each die using the IVS-200 tool. The overlay signature measured on wafer #5 is shown in Fig. 7.

The measured data was further processed using the overlay decomposition model shown below [6].

$$\begin{aligned} dx &= T_x - R \cdot y + M \cdot x \\ dy &= T_y + R \cdot x + M \cdot y \end{aligned} \quad (1)$$

Here T_x and T_y are die translations in X and Y, R is the die rotation, and M is the die magnification. This model describes errors typical for the die-to-die alignment process. It does not include wafer grid errors which are only relevant in case of global alignment; thus, the decomposition is performed per die, not per wafer. Also, anamorphism (different magnification in X and Y) and non-orthogonality errors are not included, since these are mostly relevant to scanner lithographic tools.

TABLE II

OVERLAY ERRORS MEASURED ON FOUR TEST WAFERS USING IVS METROLOGY TOOL WITH RESULTS OF DECOMPOSITION USING MODEL (1).

Wafer # (K&S slot)	Mark shift X/Y, nm	Die translation X/Y, nm	Rotation 10 mm die, urad	Rotation 4 mm die, urad	Magnification 10 mm die, ppm	Magnification 4 mm die, ppm
5	638	565	19	34	28	71
6	581	520	19	29	30	54
7	501	399	17	30	34	55
8	529	410	18	41	38	62

TABLE III

DURATION ESTIMATES PER FULLY EXPOSED 200MM WAFER WITH EITHER TYPE OF DIE BASED ON 2- OR 4-MARK ALIGNMENT PER DIE.

Die size	Total number of dies	Time to process	
		2 marks per die	4 marks per die
4 x 4 mm	300	19.6 min	33.8 min
10 x 10 mm	120	8.6 min	14.2 min

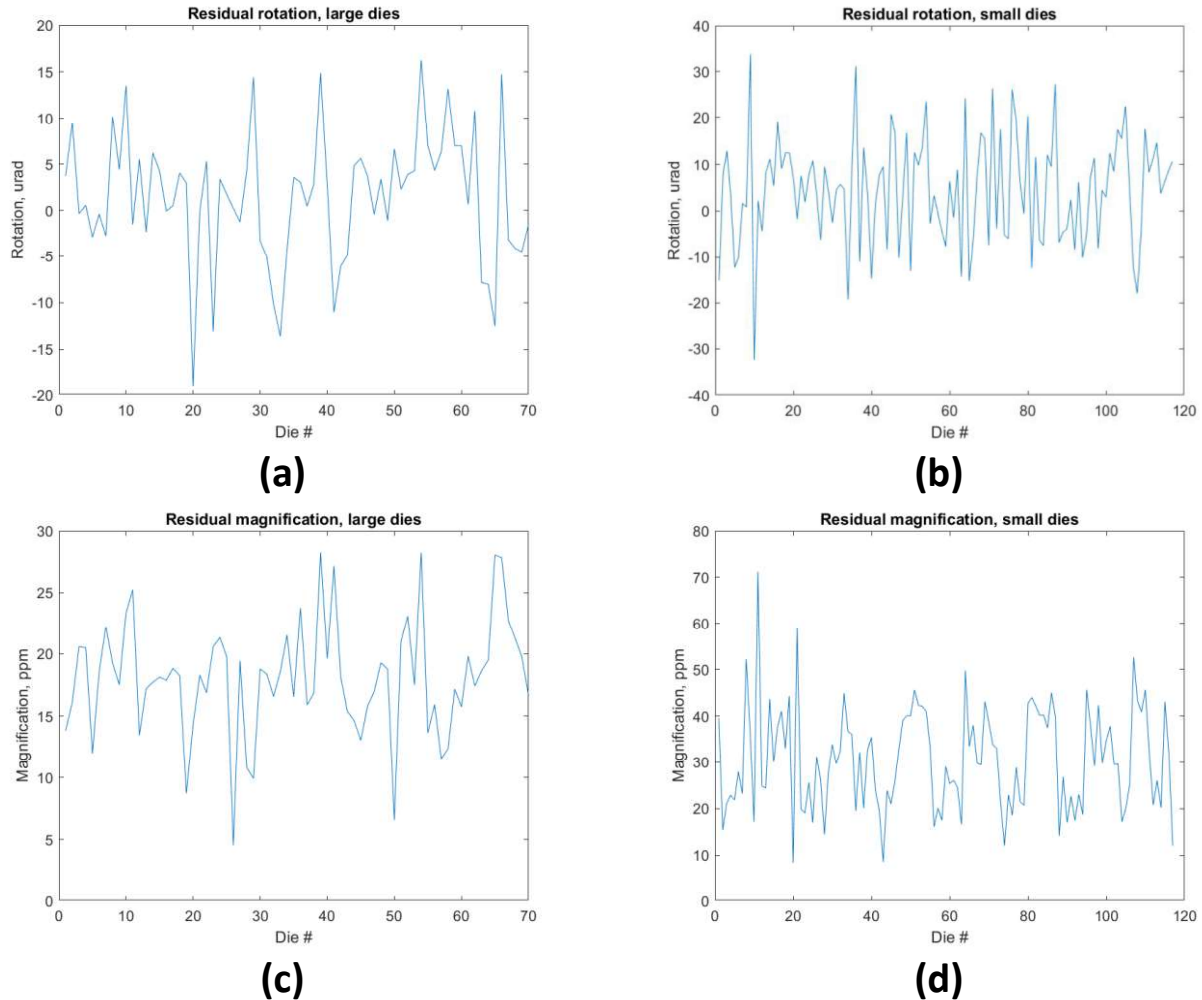


Fig. 9. Residual die rotation and magnification obtained by decomposition of the IVS-200 measurement data using model (1), wafer #5. Shown for large and small dies separately.

The results of measurement and decomposition are summarized in Table II. Wafer #5 has the largest overlay error, with mark shifts up to 638 nm (see Fig. 7) and die translations up to 565 nm (see Fig. 8). In Fig. 9, rotations and magnifications of individual dies are shown for small and large dies separately. An independent measurement on the LITEQ 500 tool based on analysis of Vernier scales confirm errors in the submicron range.

B. THROUGHPUT CONSIDERATIONS

The full wafer contained 120 small dies and 70 large dies. Each die has four alignment marks. The total time for processing the 190 dies was 23 minutes with an approach optimized for best overlay, including reticle measurement and wafer placement. This throughput is in line with current industrial standards, while the accuracy exceeds typical requirements of current FO-WLP processes. Even though with standard global alignment the test wafer could be processed in about 2 minutes, it would not be possible to achieve overlay better than 50 μm with the existing layout.

There is a potential throughput improvement of approximately 11 minutes by optimizing the alignment process. Major improvement can be achieved by measuring two marks per die instead of four; this is sufficient for fitting four die alignment parameters in (1), T_x and T_y , R and M .

We may anticipate, based on the above results, what the throughput per wafer fully processed with only 4 mm x 4 mm and only 10 mm x 10 mm dies would be. Based on our estimates, a 200 mm process LETI wafer filled could contain either 300 dies of 4 mm x 4 mm or 120 dies of 10 mm x 10 mm. Table III shows the wafer processing time for these two use cases.

IV. CONCLUSION

The results of this experiment demonstrate the capability of the LITEQ 500 tool to detect, measure and correct large offsets in die placement and rotation, providing submicron accuracy while maintaining throughput levels in line with current industrial standards. Analysis shows that major improvement of the throughput can be achieved by optimizing the alignment process. Additional experiments are planned to verify the overlay performance and demonstrate the capability of overlay diagnostics with reconstructed wafers on the LITEQ 500. Preliminary estimates indicate that an even faster throughput may be achieved when the overlay requirements are less stringent. In future work, we plan to investigate what throughput is achievable for overlay accuracy levels required in current FO-WLP processes.

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